IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 23 December 2022, accepted 8 January 2023, date of publication 12 January 2023, date of current version 19 January 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3236424

RESEARCH ARTICLE

New Zero Power Memristor Emulator Model and Its Application in Memristive Neural Computation

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ABSTRACT We present here a simple three P-type MOSFET-based grounded memristor emulator model. The model is designed to achieve zero static power dissipation and is done so by eliminating the external DC supply i.e., no DC bias. The proposed memristor emulator model has extremely low dynamic power dissipation as well which comes to around 175 nW i.e., $\sim$ 67% improvement compared to recent work. A mathematical analysis is carried out to present the relevance of this design. Simulations were done on Cadence Virtuoso 90 nm technology node and fingerprints of the proposed memristor emulator were obtained. The layout area occupied by the model is approx 1154.69 μm^2 and an external capacitor is connected to add tunability to the circuit. Furthermore, Monte Carlo and corner analysis validate the robust nature of the design. Besides, simulations have been experimentally verified using CD-4007 CMOS integrated circuit (IC) to make the design practically feasible. Furthermore, the design offers advantages such as extremely less overall power consumption and smaller chip area that could possibly pave the path for fabrication using standard CMOS technologies. At last, an application of the proposed model depicting in-memory computation through a memristor emulator crossbar array is presented in brief.

INDEX TERMS Memristor emulator, CMOS, pinched hysteresis loop (PHL), Monte Carlo, in-memory computation.

I. INTRODUCTION

The concept of memristors (resistor and memory) by Leon Chua dates back to the early 1970s [1]. These are essentially a metal-insulator-metal (MIM) structures that can be switched to a low resistance state (LRS) from a high resistance state (HRS) or vice-versa in a peculiar hysteretic manner and are hence often termed resistive RAM or RRAM. An intensive period of investigation on memristive devices was pursued in the late 1990s [2] with a wide variety of materials ranging from binary oxides to chalcogenides as well as organic compounds. However, the research was primarily triggered after Strukov [3] and his team successfully fabricated a memristor in Hewlett Packard (HP) lab that was based upon the notion of Chua. Even though there are many successfully fabricated memristors that have certain favorable properties such as low power consumption, high endurance, etc., memristors are still a fairly nascent technology to be able to promote commercialization at a larger scale. So as we await the inclusion of this nascent technology in the market, memristor emulators capable of imitating the attributes of memristive devices can play a crucial role simply because of the notable strides made by the CMOS technology.

For this reason, many designs using current mode blocks, active elements, multipliers, and other analog design architectures were explored and subsequently reported in the literature. For example, in [4], the design was implemented using four AD844, and a multiplier along with a large number of passive elements. The design in [5], incorporated three OTA (Operational Transconductance Amplifier) and 4 CCII (Second Generation Current Conveyor) blocks enjoying its operation in decremental mode. The grounded memristor configuration in [6] has a current mode block i.e. CCII and an analog multiplier along with one resistor and one capacitor. Ranjan et al. simulated CCTA (Current Conveyor Transconductance Amplifier) [7] and DVCCTA (Differential

The associate editor coordinating the review of this manuscript and approving it for publication was Baker Mohammad.

Voltage Current Conveyor Transconductance Amplifier) [8] based emulators. The design in [9] and [10] adopted a similar current mode block i.e., VDTA (Voltage Differencing Transconductance Amplifiers) to implement memristor emulators with 50 MHz as the maximum operating frequency for both works. Prasad and his team modeled a resistor-less memristor emulator [11] using a single CFTA (Current Follower Transconductance Amplifier) block. Kanyal et al. [12] investigated a high-frequency memristor emulator with the help of OTA, operating up to 8 MHz. The circuit in [13] presented a floating memristor emulator comprising of single CCTA and a single CCII current mode block with 5 MHz as the maximum frequency of operation. In [14] a design has been proposed that contains one CCII and one OTA as an active component with a single resistor and a capacitor as a passive element. This circuit has 26.3 MHz as the upper limit operating frequency. In [15], a 120 MHz memristor based on DZ-VDTA (Dual Z Output Voltage Dependent Transconductance Amplifier) has been proposed with a high transistor count. Similarly, a DVCCTA-based memristor emulator in [16] operates up to 12.8 MHz with a static power consumption of 8.74 mW. Notably, such designs had a complex circuit architecture, high power consumption, greater transistor count, and a fairly large number of passive elements. As a result, many scholars have also proposed MOS-only implementation of emulator circuits. For example, in [17] Yesil et al. presented seven MOSFET-grounded memristor emulator with operating frequencies as high as 50 MHz. Similarly, a design [18] that had only three MOS was implemented with a maximum operating frequency of 100 kHz. The work in [19] constitutes a memristor emulator with four transistors operating up to 100 MHz. Also, a new passive floating/grounder memristor emulator has been reported in [20] while Ghosh et al. in [21] presented the work with three N-type MOS having a power consumption of 2.6 μW. Meanwhile, some other works of literature containing memristor emulator circuits are reported in [22], [23], and [24].

The proposed design is a new grounded memristor emulator circuit that is devoid of any active blocks or analog multiplier circuits. It uses only three P-type MOSFETs and a capacitor and operates without any DC bias hence zero power consumption. Even the dynamic power consumption of the circuit is also very low. The capacitor voltage is used to control the conductivity of the PMOS transistors M2 and M3, necessary for implementing memristive behavior and also ensures tunability to the circuit. The rest of the paper is summarized in the following manner: Section II deals with the schematic diagram and mathematical modeling of the proposed emulator. In Section III, the simulation as well as the experimental results are described. In Section IV, a comparison table of the proposed design has been presented. Section V discusses an application perspective of the presented model using a brief memristor emulator crossbar array to demonstrate in-memory computation. Finally, the brief is concluded in Section VI.

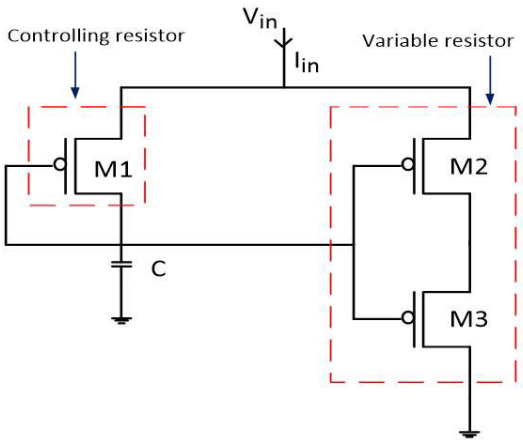


FIGURE 1. Proposed memristor model.

II. MEMRISTOR EMULATOR

The design architecture of the memristor emulator herein is a grounded topology consisting of two major parts, one is the controller circuit and another is a controlled/variable resistor. As shown in Fig.1, the proposed memristor emulator design consists of three PMOS (M1, M2, and M3). M1 along with the external capacitor, C, acts as a controller circuit. M2 and M3 act as controlled/ variable resistors. A part of the alternating current flowing through M1 controls the capacitor voltage which in turn drives the gate of M2 and M3. Thus, M1 acts as a controlling resistor whereas M2 and M3 serve as variable resistors leading to the non-linear behavior of the circuit. The connection is in such a way that M1 will always lie in the saturation region and M2 and M3 will always be in the linear region. The PMOS has been utilized in design by keeping in mind its characteristics of less threshold variation and low noise.

Next, considering the mathematical analysis, the drain current equation through the capacitor C can be written as

$$C\frac{\mathrm{d}V_c\left(t\right)}{\mathrm{d}t} = K_{p1}\left(V_{in}\left(t\right) - V_c\left(t\right) - \left|V_{tp}\right|\right)^2 \tag{1}$$

where V_{in} is the applied sinusoidal input voltage, V_c represents the capacitor voltage, V_{tp} is the threshold voltage of PMOS, $K_{p1} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{M1}$ is the process transconductance parameter of M1 transistor in which μ_p and C_{ox} are the mobility and gate oxide capacitance respectively. Expanding and rearranging (1), we get

$$\Rightarrow C\frac{\mathrm{d}V_c(t)}{\mathrm{d}t} = K_{p1}(V_{in}^2(t + 2V_c(t)|V_{tp}| + |V_{tp}|^2 + V_c^2(t) - 2V_{in}(t)|V_{tp}| - 2V_{in}(t)V_c) \tag{2}$$

Neglecting the terms in the above equation ($V_{in}^2\left(t\right)$, $2V_{in}\left(t\right)\left|V_{tp}\right|$ and $\left|V_{tp}\right|^2$) as these are very small in values,

we get an approximation as

$$\Rightarrow C\frac{\mathrm{d}V_c(t)}{\mathrm{d}t} \approx K_{p1}(2V_c(t)|V_{tp}| + V_c^2(t) - 2V_{in}(t)V_c) \quad (3)$$

$$\Rightarrow C\frac{\mathrm{d}V_c\,(t)}{\mathrm{d}t} \approx K_{p1}V_c^2\,(t)\left[-2\frac{V_{in}\,(t)}{V_c\,(t)} + 2\frac{|V_{tp}|}{V_c\,(t)} + 1\right] \quad (4)$$

$$\Rightarrow \frac{1}{V_c^2\,(t)}\frac{\mathrm{d}V_c\,(t)}{\mathrm{d}t} - \frac{2K_{p1}}{C}\frac{1}{V_c\,(t)}\left(-V_{in}\,(t) + |V_{tp}|\right) \approx \frac{K_{p1}}{C} \quad (5)$$

Substituing $V_c^{-1}\,(t) = z$ in (5) and assuming $V_{tp} \approx 0$,further simplication yeilds

$$+\frac{\mathrm{d}z\,(t)}{\mathrm{d}t} - \frac{2K_{p1}}{C}\,(V_{in}\,(t))\,z \approx \frac{-K_{p1}}{C} \quad (6)$$

where (6) closely resembles a linear first-order differential equation in z, whose solution can be obtained as

$$z \approx Be^{-\int \frac{2K_{p1}}{C}V_{in}(t)dt} \quad (7)$$

(B) here denotes the constant of integration and on replacing z by $V_c^{-1}\,(t)$, the capacitor voltage in its final form can be written as

$$V_c\,(t) \approx \frac{1}{B} + \frac{2K_{p1}}{BC}\phi\,(t) \quad (8)$$

where $\phi\,(t) \approx \int(V_{in}\,(t)\,dt$ is the flux (also called as the state variable) and is dependent on the capacitor voltage V_c.

Now, considering the transistors M2 and M3, the conductance seen at M2 can be written as

$$\frac{\alpha I_{in}\,(t)}{V_{in}\,(t)} = K_p\left(V_{GS_2} - V_{tp2}\right) \quad (9)$$

It can be noted that identical current flows through M2 and M3 as they are in series, hence the current equation from (9) can be represented as

$$\alpha I_{in}\,(t) = K_p\left(V_{GS_2} - V_{tp2}\right)V_{in}\,(t) \quad (10)$$

The source voltage of M2 is connected to sinusoidal AC input whose DC value is zero and the gate voltage equals the capacitor voltage (V_c), hence (10) modifies to

$$\frac{I_{in}\,(t)}{V_{in}\,(t)} \approx \frac{K_p}{\alpha}\left(\frac{1}{B} + \frac{2K_{p1}}{BC}\phi\,(t)\right) \quad (11)$$

The memductance equation in its final form can be eventually written as

$$\Rightarrow W\,(\phi\,(t)) \approx \frac{K_p}{\alpha}\left(\frac{1}{B} + \frac{2K_{p1}}{BC}\phi\,(t)\right) \quad (12)$$

where $K_p = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)$ is the process transconductance parameter of M2 transistor and $'\alpha'$signifies that some part of the input current flows through M1 alone and the remaining current flows through M2 and M3 transistors hence $0 < \alpha < 1$.

An in-depth insight suggests that the first term inside the bracket on the right-hand side of (12) contains the initial state of the memristor and is time-invariant whereas the second term inside the bracket denotes the linear time-variant part. It becomes apparent from (12) that the memductance is a function of its state variable $'\phi'$ which is the time integral of voltage in general and hence is a deciding factor for the state of the memristor. Also, as the memductance here is a function of the state variable $'\phi'$ or flux, it is essentially a flux-controlled memristor emulator.

Now, to analyze the effect of frequency on the hysteresis nature of the proposed memristor emulator, a sinusoidal input voltage of the form $A_m\sin(2\pi\,\mathrm{ft})$ is applied where A_m and 'f' are the signal amplitude and frequency respectively. By substituting this input voltage in (12) and using $\phi\,(t) \approx \int(V_{in}\,(t)\,dt$, we get

$$W\,(\phi\,(t)) = \frac{K_pK_{p1}A_m}{\pi\alpha fBC}\cos\,(2\pi ft) \quad (13)$$

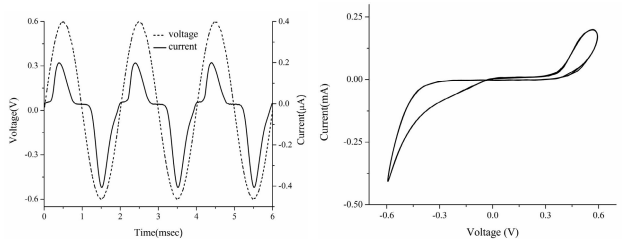
From (13) it is evident that, as the frequency approaches infinity, the memductance is dominated by the linear time-invariant part and the hysteresis nature is eventually lost thereby the circuit behaves as a simple resistor.

III. SIMULATION AND EXPERIMENTAL RESULTS

A substantial investigation of the emulator model in this work has been done through simulation as well as experimentation. The simulation setup comprises of spectre circuit simulator under 90 nm technology node in Cadence Virtuoso Tool. The settings for the circuit simulations were created in Analog Design Environment (ADE) window under moderate accuracy default settings having 27°C as the operating temperature. The first result is reflected in Fig. 2 which represents the workability of the proposed memristor emulator. Table 1 contains the aspect ratios of the three MOS transistors used in the proposed model. The unsymmetrical behavior of the proposed memristor circuit can be attributed to parasitic effects in the design [25], [26]. A multiple cycle transient analysis at 5 kHz having sinusoidal input of amplitude 600 mV has been shown in Fig. 2(a) whereas Fig. 2(b) contains the multiple cycle hysteresis curve in the voltage-current (V-I) plane which doesn't present any significant changes in the value of current unlike that of the work by Gupta et. al. in [27]. The hysteresis in Fig. 2(b) is simply because the maxima and minima of the current and voltage plots with respect to time occur at different values of the time. Unlike the usual symmetric bow-tie curve representing a memristive behavior, the hysteresis in the proposed work is unsymmetric which is still able to clearly distinguish the high and low resistance states. Moreover, these states can be altered depending on the applied voltage of suitable polarity. The hysteresis nature tends to diminish with increasing frequency which is one of the fingerprints of the memristor hysteresis loop and so is the case with the proposed model. Furthermore, the hysteresis nature of the proposed design to a great extent replicates the memristive switching as seen in some of the perovskites-based materials like that presented in [28]. Fig. 3(a) shows the nature of PHL at different signal frequencies and it can be said that the low and the high resistance states of the memristors are well-defined and distinguishable. An independent validation for the proposed

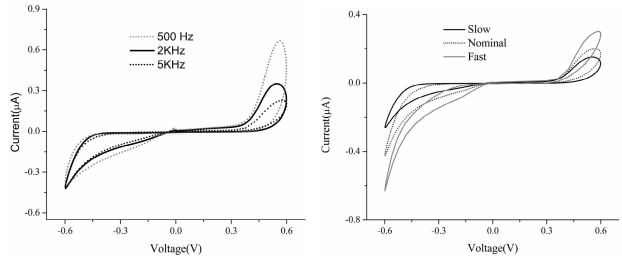
TABLE 1. Aspect ratios of the MOSFET used in the design.

MOSFET	Aspect ratio (W/L) (in μm)
M1	11/27
M2	60/4.5
M3	10.5/28



(a) (b)

FIGURE 2. (a) Transient curve (b) V-I plot.

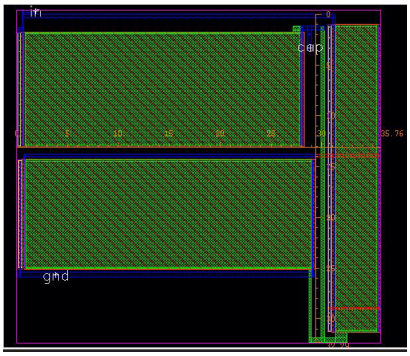


(a) (b)

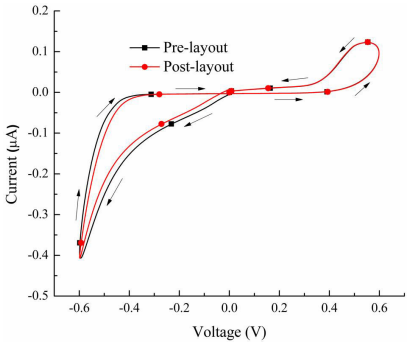
FIGURE 3. (a) Nature of PHL (.5,2,5) kHz (b) Memristor behavior at different process corners.

model is carried out by calculating the R_{OFF}/R_{ON} ratio i.e. ratio of the high resistance state value to the low resistance state value. This ratio turns out to be approx. 59 which incidentally corroborates with the findings of the TiO_2 model as in [3]. Also, the pinching of the curve has slightly deviated from the origin as seen in Fig. 3(a). However, there exist minute deviations primarily because of the drifting issues. The drift is attributed to the shift in the operating point of the MOSFETs used in this design from its usual region of operation thereby causing the hysteresis to pinch slightly away from the origin or (0,0). Moreover, the PHL area has a tendency to shrink at higher frequencies thereby signifying that the non-linearity is lost. In Fig. 3(b), the process corner analysis for nominal, slow, and fast cases has been included in order to show the robustness of the design. The deviation seen on either side of the nominal case is quite prominent and it turns out that the maximum current is achieved for the fast case while the current is lowest for the slow case.

The CMOS layout of the proposed work is shown in Fig. 4(a) and has been laid out occupying a die footprint of ≈ 1154.69 μm^2 in area. The layout of the memristor model is devoid of the capacitor and is connected externally in order to provide flexibility in tuning the capacitance value depending on the requirement. Fig. 4(b) represents a comparison between post-layout and pre-layout simulation. It is worth noting that pinched hysteresis is required for memristor behavior as stated in the work [29]. However, in the



(a)



(b)

FIGURE 4. (a) Layout for memristor structure (b) Pre-layout vs Post-layout results.

pre- and post-layout curves owing to certain non-idealities and parasitic effects involved in the layout causes the two curves to intersect at different points near the origin for the negative going pulse but these shifts or deviations are so insignificant that they do not violate the other fingerprints of the memristor.

To probe further, the input noise has been studied as shown in Fig. 5(a) and its value at 5 kHz has been found as 0.6 μV/sqrt(Hz) which is negligible when compared to the actual signal strength at the input. Further investigation is carried out for the dynamic power consumption by all the MOSFETs used in the design and the graph has been plotted in Fig. 5(b). The dynamic power as seen from the graph clearly points towards the fact that the maximum power consumed is ≈175 nW which is considerably low.

The scope of the investigation proceeds by showing the memory nature of the proposed memristor model. The behavior of the memristor is of an incremental nature as is evident from Fig. 6. Once the memristor has been programmed, the present programmed state is retained even when the supply is removed (an essential criterion for its non-volatile nature). For justifying the non-volatility criterion, we have fed an input pulse of 1 V amplitude with an ON time of 15 μs and a period of 50 μs. It is observed that during the first cycle of the ON time, the memristance value increases from its initial value to 250 Ω, stays at that programmed value during the OFF period between the duration of 15 μs to 50 μs. When the next electrical stimulation arrives, it again increases to a value of 500 Ω and continues in an identical fashion thereafter. Thus, it can be inferred that the previously

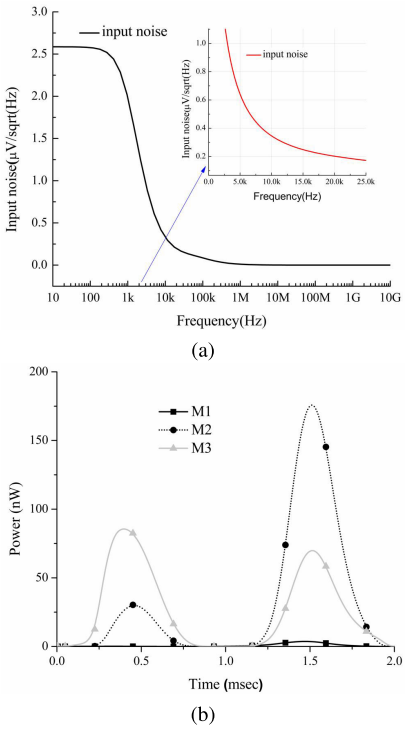


FIGURE 5. (a) Input noise for the memristor emulator (b) Dynamic power dissipation.

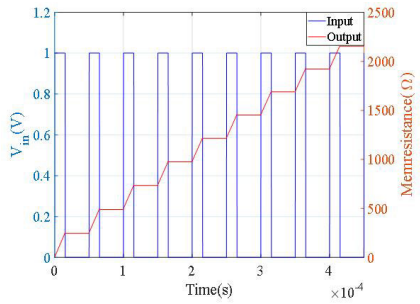


FIGURE 6. Nonvolatile nature (incremental mode).

programmed value is maintained in the absence of stimuli thereby acting as a non-volatile memory.

Statistical results from the Monte-Carlo (considering process and mismatch variations during the fabrication) analysis of the proposed memristor emulator at 5 kHz frequency and approx. 200 nA output is depicted in Fig. 7. The histogram plot provides a standard deviation of $\approx$ 1.95 nA from the actual value of the current obtained through the transient plot of Fig 2(a). Lastly, we introduce a setup that tests the proposed emulator with off-the-shelf components using CD4007 MOS IC. The schematic of the circuit emulating the memristor is shown in Fig. 8 which contains two CD4007 ICs. Two PMOS (M1 and M3) has been utilized from the first CD4007 IC whereas one PMOS (M2) is taken from the second CD4007 IC. Pin 1 of the first CD4007 which serves as the source of M3 is grounded. Pin 13 of both the ICs has been shorted which serves as the source of M1 and M2 through which the sinusoidal input is fed. Pin 2 of the first

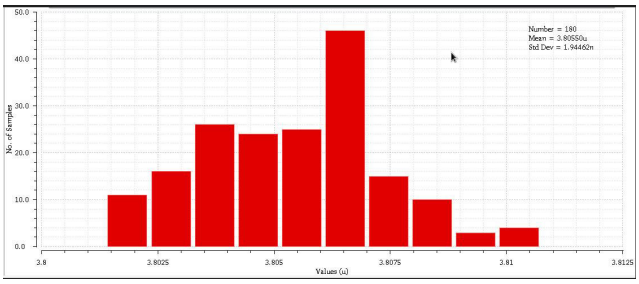


FIGURE 7. Histogram plot for Monte Carlo simulation (180 runs).

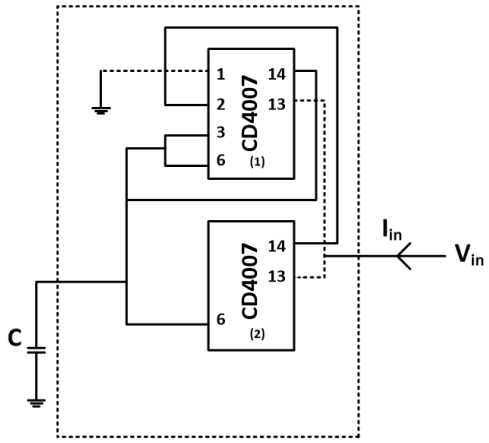


FIGURE 8. Memristor based on CD4007 MOS IC.

IC serving as the drain of M3 is connected to pin 14 of the second IC which serves as the drain of M2. The capacitor is connected to the drain of the M1 i.e., pin 14 of the first IC. Pin 3 and 6 represent the gate terminal of the PMOS in the CD4007 pin configuration. The value of the capacitor used in this experiment is 15 pF and the analyses have been done with a sinusoidal input of 750 mV at 24 MHz. Fig. 9 clearly shows the experimental observations and hence guarantees the practical feasibility of the proposed design model.

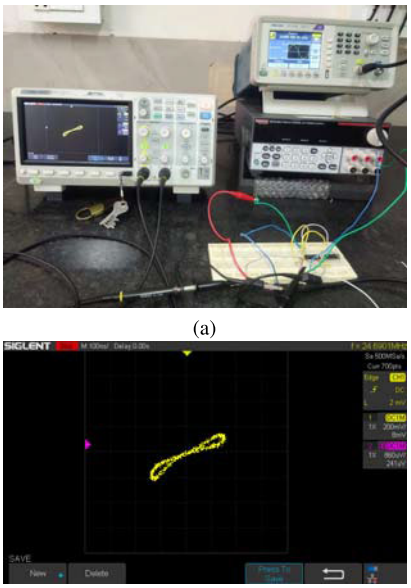
IV. COMPARISON WITH EXISTING MEMRISTOR EMULATOR

This section attempts to highlight some of the favorable features of the proposed memristor circuit over other existing emulators. The performance of the existing state of art emulators and the presented model is summarized in Table 2. Following are some of the advantages of the proposed work.

1) This work offers a very simple architecture of the memristor emulator model that operates without any bias hence zero power consumption.
2) The number of transistors in comparison to [17] is relatively less.
3) The memristor model in [19] operates at a power supply of $\pm$ 0.9 V hence the power consumption is relatively larger when compared with the proposed model.
4) A new circuit configuration emulating the memristive behavior comprising only PMOS along with a capacitor is utilized when compared with the work in [20].

TABLE 2. Comparison of the proposed memristor emulator circuit with the existing design.

Ref. No.	No. of active components	No. of passive components	Power supply	Static/Dynamic Power Consumption	No.of MOS	Operating frequency
[6]	1 - CCII, 1- Multiplier	R-1, C-1	± 10 V	NA	NA	860 kHz
[7]	1 - CCTA	R-3, C-1	± 1.5 V	NA	30	1 MHz
[8]	1 - DVCCTA	R-3, C-1	± 1.5 V	NA	29	1 MHz
[9]	1 - VDTA	C-1	± 0.9 V	8 µW/NA	16	50 MHz
[10]	1 - VDTA	R-1, C-1	± 0.9 V	CMOS	16	50 MHz
[11]	1 - CFTA	C-1	± 1.2 V	NA	28	9 MHz
[12]	2 - OTA	C-1	± 1.2 V	NA	34	8 MHz
[13]	1 - CCTA , 1 - CCII	R-3, C-1	± 1.5 V	NA	38	5 MHz
[14]	1 - CCII, 1 - OTA	R-1, C-1	± 1.2 V	9.567mW/NA	24	26.3 MHz
[16]	1 - DVCCTA	R-1, C-2	± 1 V	8.74 mW/NA	27	12.8 MHz
[17]	4 - PMOS, 3 - NMOS	C-1	± 0.9 V	NA	7	50 Hz
[18]	3 - NMOS	C-1	-	NA	3	100 kHz
[19]	2 - PMOS, 1 - NMOS	NIL	± 0.9 V	CMOS	4	100 MHz
[20]	1 - PMOS, 2 - NMOS	NIL	No DC Bias	0/NA	3	30 MHz
[21]	3 - NMOS	NIL	-	2.6 µW	4	50 MHz
This work	3- PMOS	C-1	No DC Bias	0/175 nW	3	24 MHz



(a)

(b)

FIGURE 9. (a) Experimental setup for the memristor model (b) Pinched hysteresis loop.

5) While the design in [20] also offers zero static power consumption, its operation and hence the hysteresis is entirely dependent on the parasitic capacitances of the device which puts a lot of constraint in determining the memory states of the memristor. In other words, the control over the capacitance is lost whereas the design presented here has the added advantage of tunability since the capacitor is externally connected to the circuit and can be tuned as per the requirement.
6) Far more energy efficient than [21] as the power consumption of the model is around 2.6 μW while the proposed emulator has a dynamic power consumption of 175 nW only i.e., a power reduction by $\sim$ 67%.

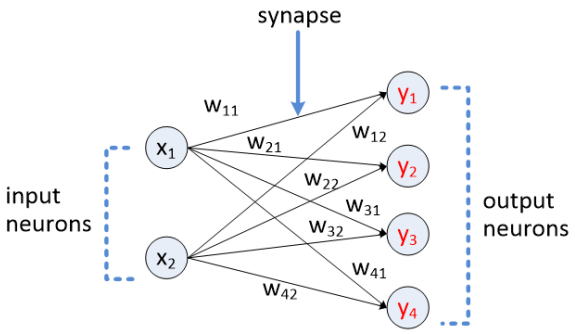


FIGURE 10. Basic neural network architecture.

V. IN-MEMORY COMPUTATION USING MEMRISTOR EMULATOR CROSSBAR ARRAY

The neural network architecture is typically inspired by the brain and mainly consists of an artificial layer of neurons and synapses as shown in Fig. 10. The artificial neurons are precisely the circles or the nodes. Their role is to accumulate, and process the inputs (x_i where i=1,2,3...n for 'n' input neurons) and pass them to the neurons in the next layer. Synapses are essentially the connecting lines of different adjustable weights (w_{ij}) between two neurons in the different layers. Here, for simplicity, we have considered a neural network of two input layer neurons and four output layer neurons. The processing of the information inside the brain takes place in the location where the information is stored (also known as in-memory computation) [30] and there is no physical separation between the memory and the processing unit unlike that of the traditional Von-Neumann

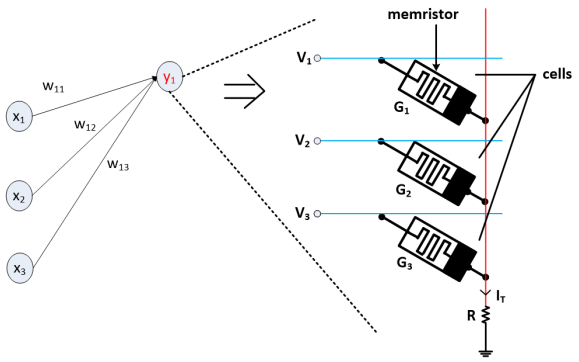


FIGURE 11. Memrsitor crossbar array.

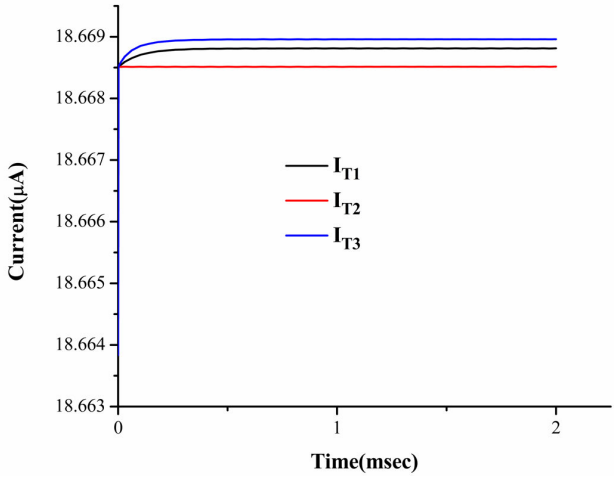


FIGURE 12. Total current I_{T1}, I_{T2}, I_{T3} at different combinations of G_1, G_2 and G_3.

architecture. Therefore, a simple memristive crossbar array of a single-neuron model using the proposed memristor emulator illustrating in-memory computation through multiply and accumulate (MAC) operation is presented in this section. This could possibly pave the path for replacing the existing CMOS-based neuromorphic hardware built upon the Von-Neumann model which is a bottleneck in terms of power and area. Basic neural computation is governed by (14) in the following way

$$y_j = \sum_{i=1}^{2} x_i w_{ji} \tag{14}$$

where y_j (j=1,2,3,4) is the output neuron and w_{ji} denotes the weight values between i_{th} input and j_{th} output neuron. In order to emphasize the MAC operation using memristors in a crossbar array, we have neglected the bias value and concept of thresholding.

To demonstrate the aforementioned scheme, a simple one-dimensional crossbar array having three rows and one column is schematically depicted in Fig. 11. The notion can be further extended to larger dimensions of the memristive crossbar arrays for solving complex problems. The rows of each cell are fed with an input voltage signal and they analogously depict the input to the neurons in the input layer. Each cell comprises the proposed memristor which acts like a synapse with adjustable weight values. The weight here refers to the different tunable conductances of each memristor in the cell. The current at each junction is the result of the multiplication of the input voltage (V_i, i=1,2,3) with the conductance (G_j, j=1,2,3) of the memristor which is basically in accordance with Ohm's law. The total current (I_T) measured in the column is primarily the accumulation or summation of the individual junction currents (Kirchoff's current law). In this design, a resistance R of 100 Ω has been used to measure the total current at the column whereas V_1, V_2 and V_3 are chosen as 1 V each. Thus the mulpilcation at each junction and the final summation at each column is popularly referred to as the MAC operation which is the essence of every neural computation. Moreover, in such arrangements of the memristive crossbar, the computation occurs on the conductance values of the memristor which can be tuned as per the need and stored in the cell itself, hence the term in-memory computation. Therefore, precise tuning of the conductances yields different values of total currents at the column of the crossbar array. Equation (15) shows the MAC operation for the memristor crossbar arrays in this paper.

$$I_T = V_1 G_1 + V_2 G_2 + V_3 G_3 \tag{15}$$

Finally, the simulation result for total currents i.e., I_{T1}, I_{T2} and I_{T3} for different combinations of tunable conductances G_1, G_2 and G_3 is shown in Fig. 12.

VI. CONCLUSION

In this brief, a novel framework for achieving a zero power-consuming memristor emulator is designed. The key feature of the proposed memristor emulator is its simple design with less transistor count and zero static as well as extremely low dynamic power consumption. The efficiency of almost $\sim$ 67% in terms of power dissipation has been achieved compared to the other works in the recent available literature. The proposed emulator has been able to replicate the fingerprints of the memristor which has been manifested by means of simulation and experiment. The design occupies an area of 1154.69 μm^2. Additionally, a memristor crossbar array has been investigated to perform neural computation and it can be forseen that such a circuit can be used to perform complex computations in other real world applications. At last, the memristor emulator circuit owing to its numerous advantages can easily alleviate some of the shortfalls of real memristive devices in near future.

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