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RESEARCH ARTICLE

A Hybrid PWM Technique to Improve the Performance of Voltage Source Inverters

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ABSTRACT Due to the rapid advancement of power semiconductor devices, the use of voltage source inverters (VSIs) has gained widespread acceptance. As a consequence, the performance of the voltage source inverter has emerged as a critical aspect that is highly reliant on the modulation strategy. The pulse width modulation (PWM) technique is the most widely utilized method of controlling power semiconductor switches of VSI. Power quality is always considered as an industrial concern for VSI-based power system such as grid-connected renewable energy systems and industrial motor drives which largely depends on the PWM technique used for switching. However, the existing PWM schemes for VSIs suffer from high total harmonic distortion (THD) and power loss problems. To mitigate the THD and power loss of VSI, a hybrid PWM technique has been proposed in this paper. The proposed hybrid PWM technique introduces a modified modulating signal along with newly shaped carrier signal. A two-level VSI is used to evaluate the performance of the proposed hybrid PWM technique both for with and without filter conditions against RL load. The proposed hybrid PWM technique offers 0.89% filtered voltage THD and 0.69% filtered current THD which are lower than that of existing PWM techniques. On the contrary, at without filter condition, the proposed hybrid PWM technique shows THDs of 45.77% and 12.50% for inverter output voltage and current, respectively which are also lower than those of existing PWM techniques. Apart from these, the proposed hybrid PWM technique reduces the switching and conduction power losses of the VSI as compared to existing PWM techniques. The simulation works are carried out in MATLAB/Simulink environment and a reduced scale experiment is conducted in laboratory to evaluate the performance of the proposed hybrid PWM technique.

INDEX TERMS Voltage source inverter, pulse width modulation, total harmonic distortion, switching loss, conduction loss.

I. INTRODUCTION

Voltage source inverters (VSIs) are used in a variety of applications such as variable frequency drives, grid integration of renewable energy systems, high voltage DC (HVDC) power transmissions, uninterrupted power supply (UPS) circuits and low-cost solid-state frequency charger circuit etc. [1]. Grid-connected photovoltaic systems and induction motor drives are the mostly used research area for VSI-based power systems. Power quality is a constant challenge for any kind of VSI based power system which mostly relies on the pulse width modulation (PWM) scheme used for inverter switching [2]. The power quality of VSI depends on some critical parameters. Total harmonic distortion (THD) and switching

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loss are considered as the main performance parameters of VSI [3]. The international standard IEC-61000-3-2 governs the THD of the inverter. According to IEEE Standard 519-2014, the THD of the voltage must be kept to a bare minimum and must be less than 5% for harmonic spectra up to the 49th harmonic. For critical VSI based power systems, maintaining THD according to IEEE regulations is always a research concern. A number of PWM switching techniques can be used to regulate the THD of VSI. Apart from THD, PWM technique has a substantial impact on the switching and conduction power losses of the inverter. The THD and power loss of the inverter may be reduced using the appropriate PWM scheme which increases the power quality of VSI based power system by reducing THD and power loss [4].

Different types of PWM schemes for VSI are offered by various researchers for improving the power quality. Each PWM technique has its own set of benefits and drawbacks depending on the application of the VSI. The most common PWM methods are sinusoidal PWM (SPWM), third-harmonic injected PWM (THPWM), conventional space vector PWM (CSVPWM), sixty-degree PWM (SDPWM), thirty-degree bus clamping PWM (TDBCPWM), and sixty-degree bus clamping PWM (SDBCPWM) [5]. SPWM is the most basic modulation technique used in VSIs. A VSI switched by SPWM technique is unable to generate adequate voltage as there is a significant attenuation of the magnitude of the fundamental component. By over modulating the inverter, enough voltage can be generated, but the output voltage waveform will then be deformed [6]. By adding a measure of 3rd harmonic component to the modulating signal of SPWM, it is possible to enhance the output voltage quality of a VSI beyond what is feasible with pure sinusoidal modulation. When the amplitude of the 3rd harmonic is one-sixth that of the fundamental, the highest increment in output voltage is produced. This technique is called THPWM. This approach allows for a 15% increase in the output voltage of PWM inverters without creating line-to-line voltage distortion [7]. Three-dimensional space vector modulation (SVM) is the most often used method, and that might be used in two-level VSIs [8]. CSVPWM uses an advanced computational switching approach to decrease THD, it has shown superior performance in terms of lower THD, higher power factor (PF), and lower switching losses. It also decreases switching losses by only changing one switching state at a time, ultimately resulting in a single-phase voltage shift. Moreover, as compared to SPWM, CSVPWM provides superior performance at high switching frequencies [9].

Over CSVPWM, hybrid PWM approaches, such as THSDPWM, can reduce both THD and switching loss. The harmonic performance of VSI has been proven to improve across a wide range of modulation indexes employing CSVPWM, SPWM, and THSDPWM [10], [11]. When compared to CSVPWM, THPWM approach is widely recognized for reducing THD at high modulation indices at an average switching frequency. In comparison to conventional SPWM, THSDPWM, and CSVPWM approaches, the suggested modulation technique delivers 4.07% THD of input line current [12]. Inverter losses are not emphasized in the paper. To lessen computing overhead in real-time implementation, unified PWM is implemented in [13]. Several PWM approaches, including SPWM, CSVPWM, and discontinuous space vector PWM (DSVPWM) were utilized for VSI based systems. These discontinuous PWM techniques were evaluated for improving the efficiency of the VSI by reducing switching losses but the analysis for harmonic contents in the inverter output voltage was not focused in those works.

Existing PWM schemes include flaws, such as a higher number of switch commutations at high current throughout the fundamental period including the use of extra reference signals. In [14], the presented modulation strategy, known as simple-boost modified space vector (SBMSV) modulation, decreases the amount of switch commutations for a short period of time during the fundamental cycle, simplifies gate signal generation by utilizing only three reference signals.

Most PWM techniques fail to address the specific requirements of broader power factor operation and THD. In [15], a unique scalar PWM scheme for VSIs has been proposed to address such significant disadvantages. The power losses in the inverter switches are not addressed in the paper.

In [16], sawtooth carrier-based PWM (SCPWM) schemes have been presented for the reduction of common mode voltage (CMV) in both the peak-to-peak amplitude and the carrier frequency. These techniques are easily adaptable to symmetrical multiphase VSI with any odd phase number. But these SCPWM schemes deteriorate the THD of output current. In [17], a carrier based PWM scheme has been suggested which includes two novel carriers named as M-type and CD-type carrier. The carrier based PWM exhibits promising performance in terms of both THD and power loss. A hybrid PWM technique called minimal switching loss PWM is suggested in [18]. The suggested method results in a decrease in harmonic distortion. For high modulation indices, specific sequences may effectively reduce switching loss as well as line current ripple. The use of a hybrid modulation method demonstrated in [19] to reduce switching loss while preserving output voltage/current quality and allowing for quick dynamic control of the neutral point voltage. These characteristics facilitate the creation of low-capacitance dc-bus PV inverters with improved efficiency and output waveform quality.

The inverter power loss is a very crucial parameter to analyze the performance of the VSI. Different PWM methods exhibit different switching and conduction losses. Image processing of datasheet characteristics and numerical methodology are the foundations methods for analyzing switching and conduction power loss that are provided in [20]. Instead of using linear characteristics for the approximation, higher order polynomials are used for semiconductors for calculating losses at various operating points [21].

In [22], switching and conduction losses of the switches as a percentage of the output power for various output power values are acquired by using SVPWM and modified SVPWM schemes, while SPWM and THPWM modulation technique implied almost the same losses as the SVPWM scheme, and the bus clamping thirty-degree PWM (BCTH-PWM) scheme gives almost the same losses as the modified SVPWM scheme. The benefit of utilizing the modified SVPWM modulation scheme is for better conversion efficiency [23]. Although the THD has not been addressed in the paper. It can be observed that different PWM modulation techniques are utilized in VSIs which have their both advantages and disadvantages. According to the application of the VSI, suitable PWM technique should be selected for minimizing power losses and THD which will lead to improved efficiency of the system [24], [25].

To resolve the aforementioned shortcomings of existing PWM techniques employed for VSI, a novel hybrid PWM technique is proposed in this paper to reduce the THD and power losses of the inverter. A two-level VSI has been taken into consideration for evaluating the performance of the proposed hybrid PWM technique. The proposed PWM technique introduces a new composite harmonic injected modulating signal along with newly shaped carrier signal. That's why the name hybrid is used. The major contributions of the proposed hybrid PWM technique are as follows:

- Mitigates the THD of the VSI;
- Reduces the switching losses of the switches;
- Reduces the conduction losses of the switches;
- Reduces the amount of heat and stress on the power semiconduction switches by minimizing power loss;

II. INVESTIGATED INVERTER TOPOLOGY

The performances of the proposed PWM technique are investigated for a two-level VSI as shown in Fig. 1.

The VSI consists six IGBT switches which are named as S1, S3, S_5, S_4, S_6, and S_2, respectively. The DC input voltage is chosen as 400V during simulation study. The LC filter is used in between the VSI and load to suppress the harmonics. The switch pairs (S_1, S_4), (S_3, S_6), and (S_5, S_2) should not be turned ON simultaneously to avoid the short-circuiting of DC source. In the gate pulse generation block, the mechanism of generating the gate signals for the VSI is depicted. Three modulating signals (M_a, M_b, and M_c) are compared to a high frequency carrier signal to generate the gate pulse for the IGBTs. The proposed modulating and carrier signals are used here to produce the gate pulses for the VSI. The simulation results are recorded for an RL load throughout the paper.

III. EXISTING PWM TECHNIQUES FOR VSI

There are various PWM techniques used in VSIs. The most commonly utilized PWM techniques are SPWM, THPWM, CSVPWM, and SDPWM which are frequently used in various VSI based applications. Table 1 represents the mathematical expressions of different existing PWM schemes. These PWM techniques are widely used to drive the power switches

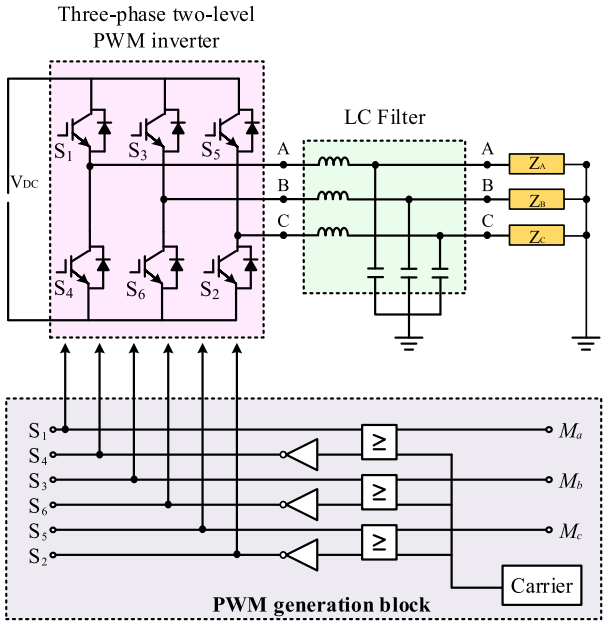

FIGURE 1. Three-phase two-level VSI with PWM generation block.

of VSI. Their performance can be further improved in terms of THD and inverter power loss by bringing some changes into the modulating signal. Modification of the conventional carrier signal can also provide some promising performance improvements for the VSIs. Fig. 2 shows the modulating signals for the existing PWM methods along with the proposed hybrid PWM technique.

TABLE 1. Mathematical representation of different PWM techniques.

PWM	Mathematical Representation
SPWM [3]	$M_1 = A\sin(\omega t + \theta)$ $[M_{1a}\ M_{1b}\ M_{1c}] = [M_{1_{\theta=0^\circ}}\ M_{1_{\theta=-120^\circ}} M_{1_{\theta=120^\circ}}]$
THPWM [5]	$C = kA\sin(3\omega t)$ $M_2 = A\sin(\omega t + \theta) + C$ $[M_{2a}\ M_{2b}\ M_{2c}] = [M_{2_{\theta=0^\circ}}\ M_{2_{\theta=-120^\circ}} M_{2_{\theta=120^\circ}}]$
CSVPWM [8]	$M_3 = \frac{2}{\sqrt{3}}[A\sin(\omega t + \theta)] - \frac{1}{2}\{\max(M_{1a}, M_{1b}, M_{1c}) + \min(M_{1a}, M_{1b}, M_{1c})\}$ $[M_{3a}\ M_{3b}\ M_{3c}] = [M_{3_{\theta=0^\circ}}\ M_{3_{\theta=-120^\circ}} M_{3_{\theta=120^\circ}}]$
SDPWM [10]	$M_4 = \frac{2}{\sqrt{3}}[A\sin(\omega t + \theta)] + \frac{1}{2\pi}[A\sin(3\omega t + \theta)] + \frac{1}{60\pi}[A\sin(9\omega t + \theta)] + \frac{1}{180\pi}[A\sin(15\omega t + \theta)]$ ... $[M_{4a}\ M_{4b}\ M_{4c}] = [M_{4_{\theta=0^\circ}}\ M_{4_{\theta=-120^\circ}} M_{4_{\theta=120^\circ}}]$

IV. DEVELOPMENT OF THE PROPOSED HYBRID PWM TECHNIQUE

The proposed hybrid PWM technique consists of a modified modulating signal and a new carrier signal. The design, mathematical development, and generation procedure of the proposed modulating and carrier signals are described in this section.

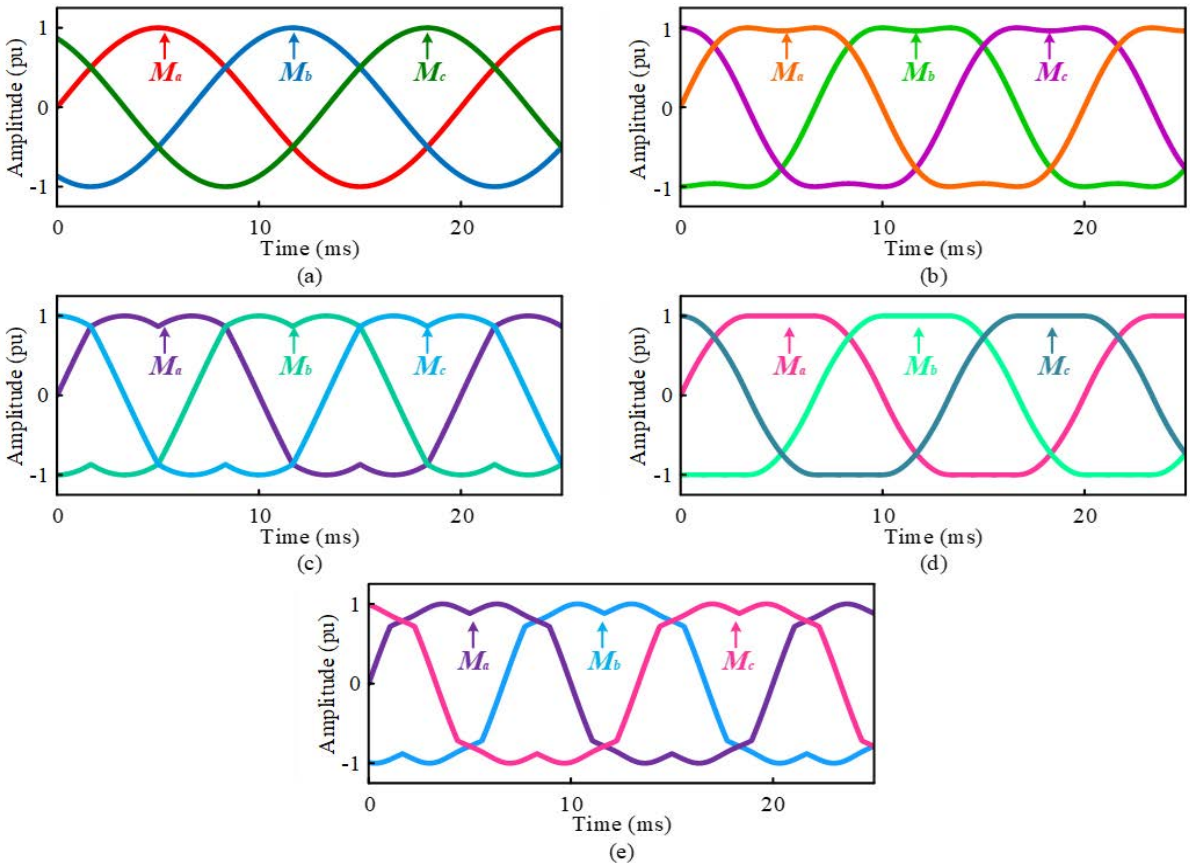

FIGURE 2. Three-phase modulating signals of (a) SPWM, (b) THPWM, (c) CSVPWM, (d) SDPWM, and (e) the proposed hybrid PWM technique.

A. DESIGN OF THE PROPOSED MODULATING SIGNAL

The proposed modulating signal consists of several signals. Saturated triangular, sinusoidal, inverted triangular and 7th harmonic signal are mixed together in order to produce the proposed modulating signal. To generate the proposed modulating signal at first, a triangular signal, W' of line frequency is taken as:

$$W' = m2\pi \sin^{-1}\{A \sin(\omega t + \theta)\} \tag{1}$$

where, m2π and A are the amplitude constants of W' and the sinusoidal signal, respectively. The triangular signal, W' is then saturated at a defined level to produce the signal, W as follows:

$$W' = W = \begin{cases} nA_m; & W > nA_m \\ -nA_m; & W < nA_m \end{cases} \tag{2}$$

After that, a sinusoidal signal (X) of line frequency is generated as:

$$X = pA \sin(\omega t + \theta) \tag{3}$$

Then an inverted triangular signal (Y) of line frequency shown in (4) is produced.

$$Y = -q2\pi \sin^{-1}\{A \sin(\omega t + \theta)\} \tag{4}$$

Finally, a 7th harmonic component (Z) of low amplitude is produced as shown (5).

$$Z = rA \sin(7\omega t + \theta) \tag{5}$$

where, p, q, and r correspond to the amplitude constant of X, Y, and Z, respectively. Finally, the signal W, X, Y, and Z are added up to generate the proposed modulating signal (M). The mathematical expression and three-phase representation of the proposed modulating signal are given in (6) and (7), respectively.

$$M = W + X + Y + Z \tag{6}$$

$$\left[M_a\ M_b\ M_c\right] = \left[M_{a_{\alpha=0^\circ}}\ M_{b_{\alpha=-120^\circ}}\ M_{c_{\alpha=120^\circ}}\right] \tag{7}$$

Thus, the proposed modulating signal, M is produced. The detailed step by step generated procedure of the proposed modulating signal, M is depicted in Fig. 3 with necessary equations and waveforms. The three-phase version of the proposed modulating signal is shown in Fig. 4.

B. DESIGN OF THE PROPOSED CARRIER SIGNAL

To generate the proposed carrier signal, a sinusoidal wave (P) is taken as at first:

$$P = aA \sin(\omega t + \theta) \tag{8}$$

Then a triangular wave (Q) is produced having triple the frequency of the sinusoidal signal (P) which is

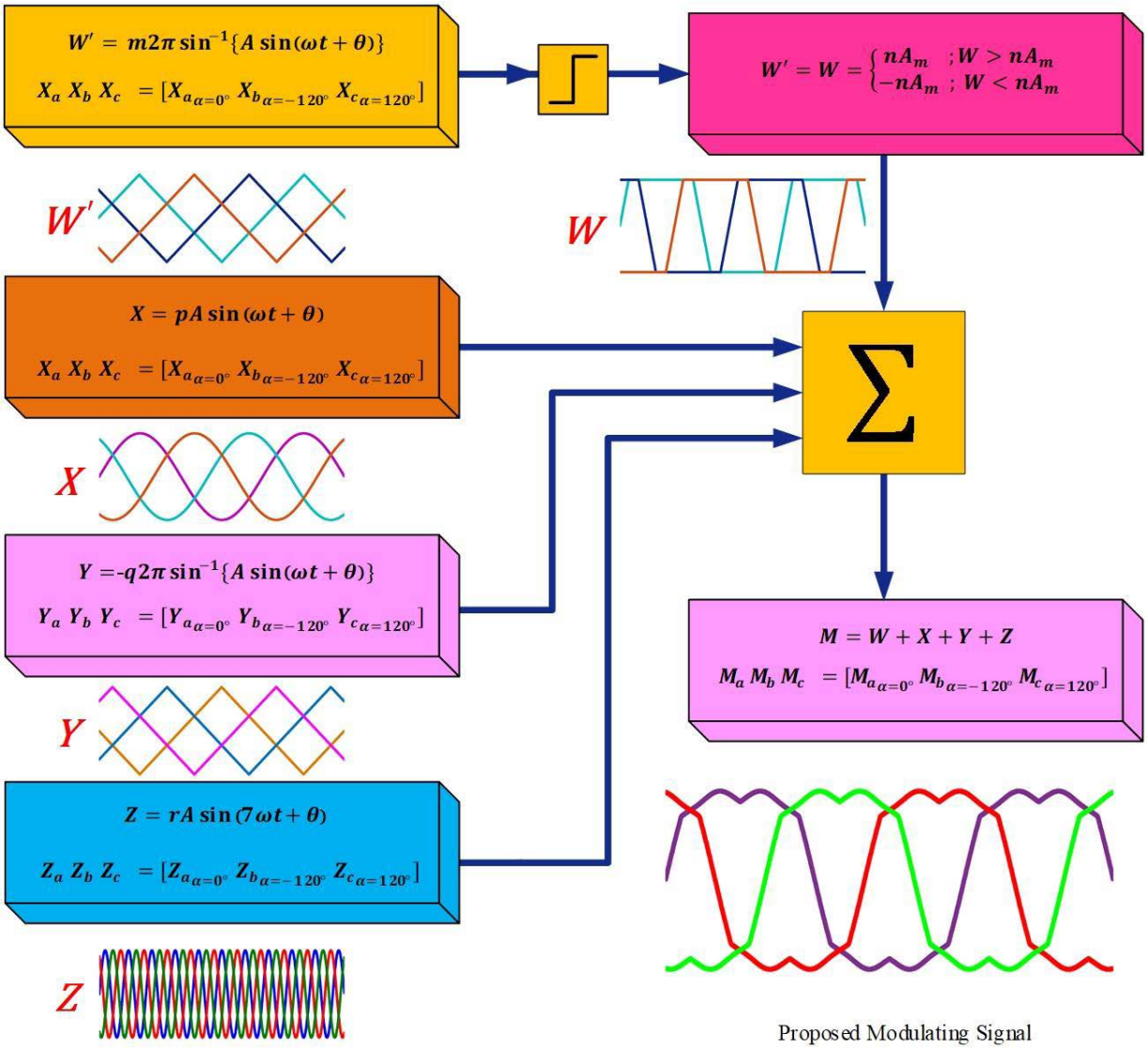

FIGURE 3. Generation procedure of the proposed modulating signal.

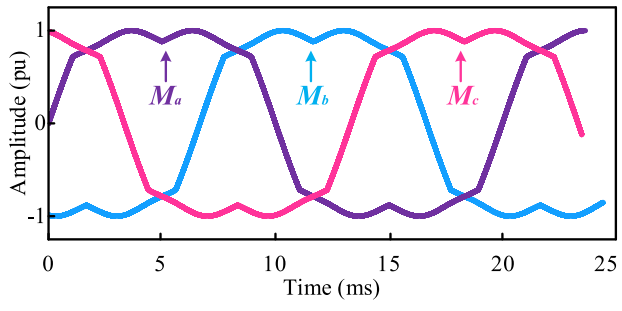

FIGURE 4. Three-phase representation of the proposed modulating signal.

represented as:

$$Q = b2\pi \sin^{-1}\{A\sin(3\omega t+\theta)\} \tag{9}$$

The sinusoidal wave (P) and triangular wave (Q) are then added to generate the signal (R).

$$R = P + Q \tag{10}$$

After that, a sinusoidal signal, S' having double the frequency of signal, P is taken as:

$$S' = cA\sin(2\omega t+\theta) \tag{11}$$

where, a, b, and c are the amplitude constants. Then the signal, S' is compared to zero to generate the signal, S as shown in (12).

$$\begin{aligned} S' = S &= 0\,[when S < 0] \\ &= 1\,[when S > 0] \end{aligned} \tag{12}$$

Finally, the signals, R and S are multiplied to generate the proposed carrier signal, C as given in (13)

$$C = RS \tag{13}$$

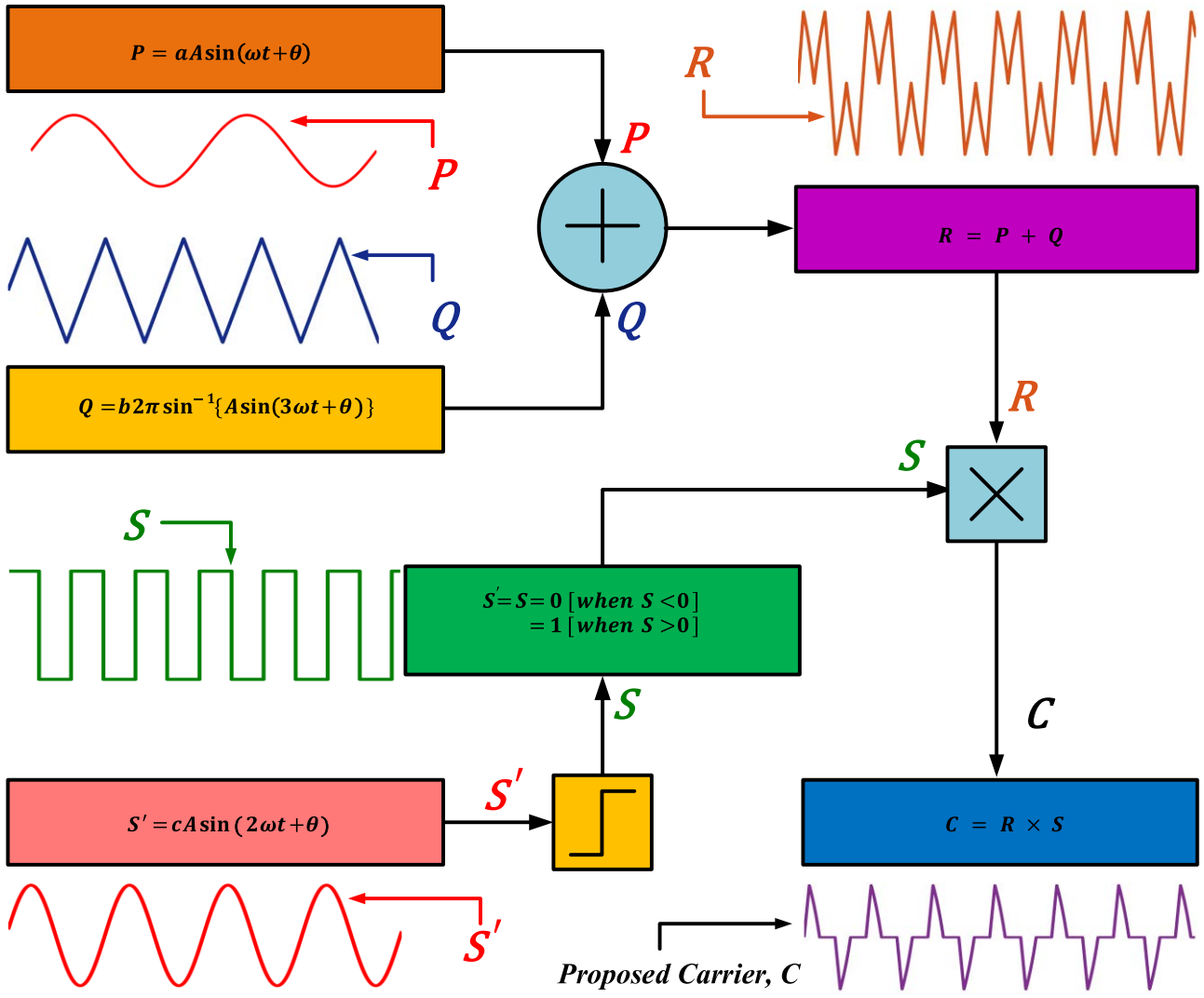

FIGURE 5. Generation procedure of the proposed carrier signal.

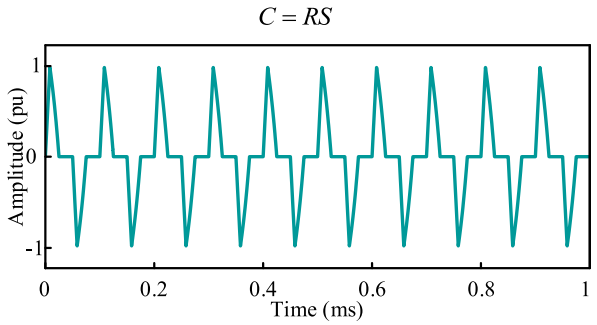

FIGURE 6. Proposed carrier signal.

Fig. 5 depicts the detailed step by step generation procedure of the proposed carrier signal with corresponding waveforms and equations. The proposed carrier signal of 10kHz frequency is shown in Fig. 6. The proposed modulating signal of Fig. 4 as well as the proposed carrier signal of Fig. 6 form the proposed hybrid PWM technique.

C. GATE PULSE GENERATION WITH THE PROPOSED HYBRID PWM TECHNIQUE FOR THE VSI

To produce the gate pulses for the IGBTs of the VSI, the proposed modulating signal is compared with the proposed carrier signal. Fig. 7 depicts the gate pulse generation procedure for the proposed hybrid PWM technique. When the amplitude of the modulating signal is greater than the amplitude of the carrier signal, the gate pulse will be high. On the contrary, when the amplitude of the modulating signal is less than the amplitude of the carrier signal, the gate pulse will be low. The gate pulses of Fig. 7 are shown for 1kHz carrier signal frequency to clearly visualize the comparison of the modulating signal and the carrier signal. It can be observed that the proposed carrier signal generates more symmetrical gate pulses. The pulse symmetry plays a vital role in overall performance of VSI. Therefore, more symmetrical gate pulses are desired as it reduces not only the harmonic distortion but also the overall power losses of the inverter. This is the superiority of the proposed hybrid PWM technique

compared to existing counterparts. The modulation index controls the output voltage of the inverter which is defined as the ratio of the modulating signal amplitude and carrier signal amplitude.

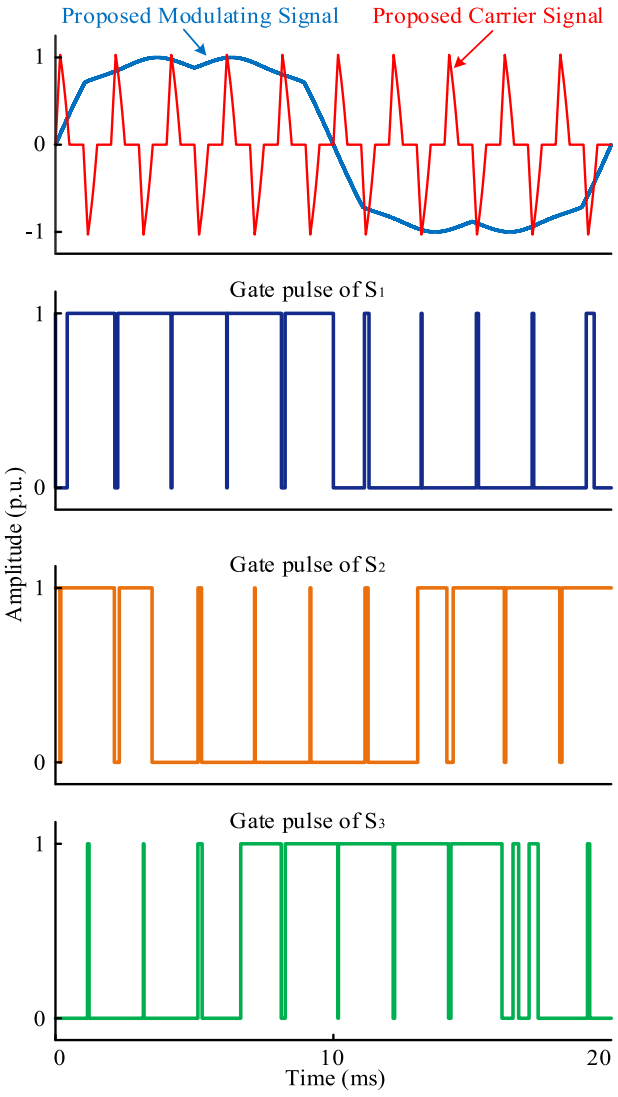

FIGURE 7. Gate pulse generation procedure with the proposed hybrid PWM technique for VSI.

V. PERFORMANCE ANALYSIS OF THE PROPOSED HYBRID PWM TECHNIQUE

A. THD ANALYSIS FOR THE PROPOSED HYBRID PWM TECHNIQUE

The unfiltered output line voltage and current waveforms of the VSI with the proposed hybrid PWM technique are shown in Fig. 8(a) and Fig. 8(c), respectively. The unfiltered voltage and current THDs are 45.77% and 12.50% as depicted in Fig. 8(b) and Fig. 8(d), respectively. To limit the THD according to IEEE-519 standard, an LC filter is introduced in between the inverter and the load. The filtered voltage and current waveforms of the VSI are shown in Fig. 9 (a) and Fig. 9(c), respectively. The filtered voltage THD with the proposed hybrid PWM technique is 0.89% as shown in Fig. 9(b).

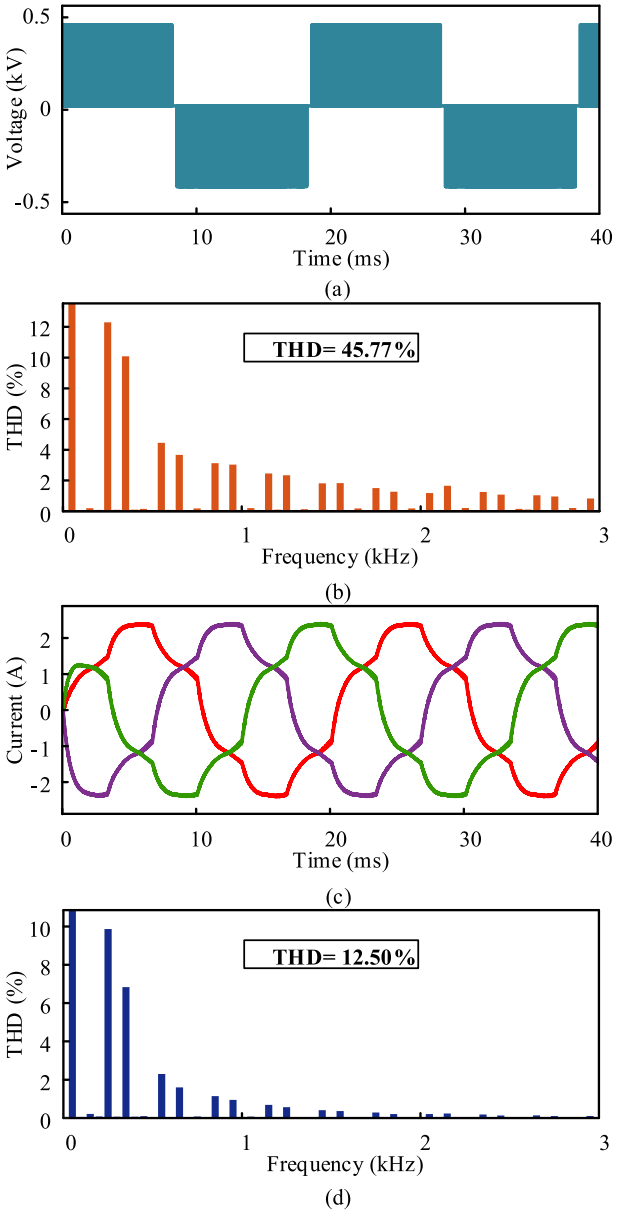

FIGURE 8. Unfiltered inverter line voltage and current for the proposed hybrid PWM technique along with their THDs: (a) unfiltered line voltage, (b) unfiltered voltage THD, (c) unfiltered line current, and (d) unfiltered current THD.

Whereas the filtered current THD is 0.69% as depicted in Fig. 9(d). The lower order harmonic components are properly attenuated by the proposed hybrid PWM technique. With the change of output filter size, the THD of the inverter will change. The proposed hybrid PWM technique performs better in terms of THD than those of existing SPWM, THPWM, CSVPWM, and SDPWM techniques under any circumstances of the VSI which are analyzed and discussed in the later sections.

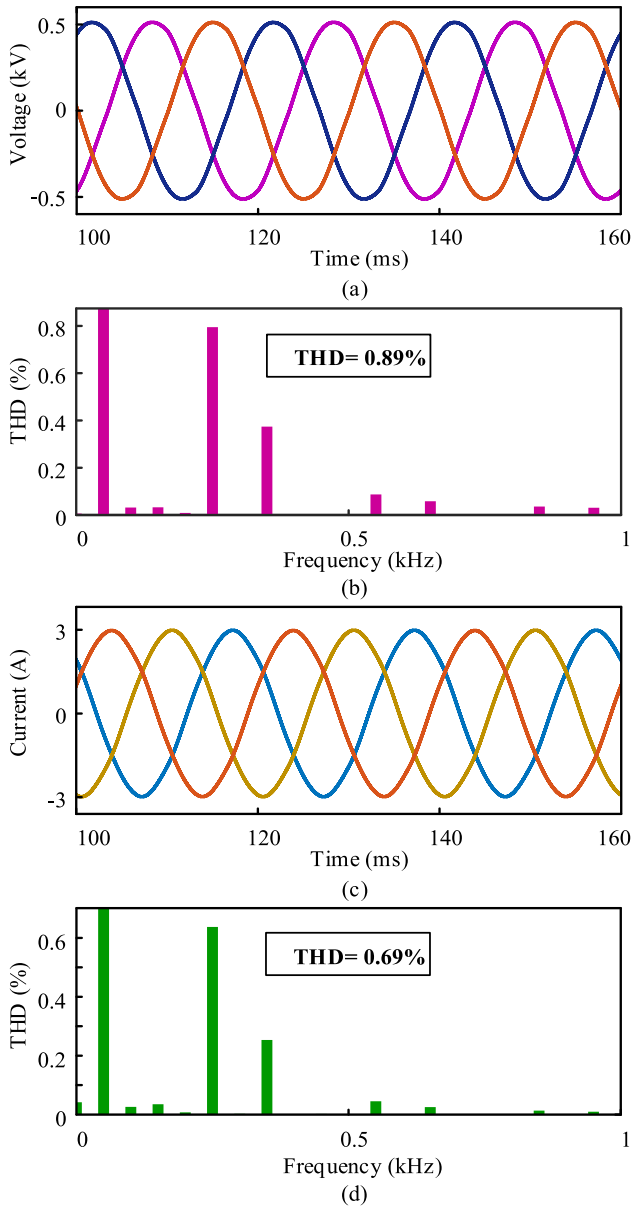

FIGURE 9. Filtered inverter line voltage and current for the proposed hybrid PWM technique along with their THDs: (a) filtered line voltage, (b) filtered voltage THD, (c) filtered line current, and (d) filtered current THD.

B. THD COMPARISON WITH EXISTING PWM TECHNIQUES

The comparative analysis of THD is conducted by varying the switching frequency and modulation indices for different PWM techniques. The unfiltered THDs for SPWM, THPWM, CSVPWM, SDPWM, and the proposed hybrid PWM techniques are shown in Fig. 10(a). Under unfiltered condition, the proposed hybrid PWM scheme exhibits 33.6% less THD as compared to SPWM technique. The proposed hybrid PWM scheme exhibits 44.7% less unfiltered THD as compared to SPWM technique. For unfiltered output voltage, the proposed hybrid PWM technique shows THD improvement of 12.62%, 13.28% and 13.54% as compared to THPWM, CSVPWM and SDPWM techniques, respectively. The filtered THDs of SPWM, THPWM, CSVPWM, SDPWM, and the proposed hybrid PWM techniques are shown in Fig. 10(b) against carrier frequency variation ranging from 1kHz to 20kHz. Table 2 summarizes the THDs of SPWM, THPWM, CSVPWM, SDPWM, and the proposed hybrid PWM techniques with the variation of carrier frequency for both filtered and unfiltered conditions. From the Table 2, it can be observed that the proposed hybrid PWM scheme brings significant improvement in terms of THD performance of the output voltage of the VSI. The optimum switching frequency can be considered to be 10kHz as it provides the optimum THD because higher frequency will result in high switching losses.

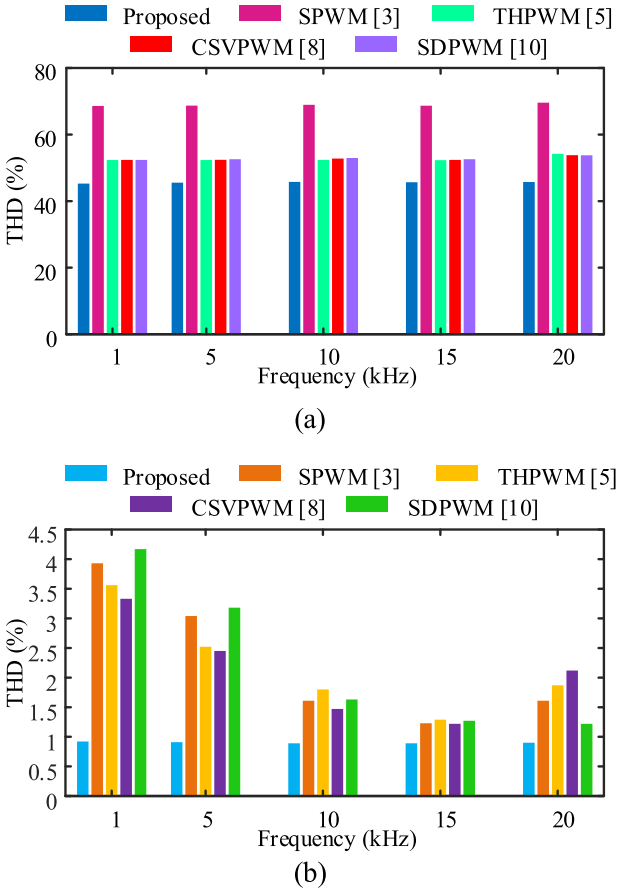

FIGURE 10. THD comparison among different PWM techniques for varying switching frequency: (a) non-filtered voltage THD (b) filtered voltage THD

The filtered and unfiltered THDs for the SPWM, THPWM, CSVPWM, SDPWM, and the proposed hybrid PWM techniques are shown in Fig. 11(a) and Fig. 11(b), respectively against modulation index variation. Three different modulation indices are shown these are under modulation index, unity modulation index, and over modulation index, respectively. From Fig. 11(a) and Fig. 11(b), it is evident that the proposed hybrid PWM technique shows minimum THD under different modulation indices variation as compared to

TABLE 2. THD comparison with the variation of carrier frequency.

Frequency (kHz)	Proposed		SPWM [3]		THPWM [5]		CSVPWM [8]		SDPWM [10]	
	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)
1	45.28	0.92	68.59	3.93	52.33	3.56	52.38	3.33	52.39	4.17
5	45.55	0.91	68.69	3.04	52.35	2.52	52.41	2.45	52.58	3.18
10	45.77	0.89	68.93	1.61	52.38	1.8	52.78	1.47	52.94	1.63
15	45.67	0.89	68.64	1.23	52.32	1.29	52.37	1.22	52.57	1.27
20	45.73	0.90	69.58	1.61	54.19	1.87	53.8	2.12	53.78	1.22

TABLE 3. THD comparison with the variation of modulation index.

MI	Proposed		SPWM [3]		THPWM [5]		CSVPWM [8]		SDPWM [10]	
	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)	Non-filtered Voltage THD (%)	Filtered voltage THD (%)
0.7	64.95	1.02	104.7	1.70	90.46	1.71	90.25	1.45	90.37	1.79
0.8	59.23	0.97	92.02	1.77	77.38	1.92	77.53	1.77	76.71	1.77
0.9	52.52	0.93	79.47	1.54	64.44	1.40	64.24	1.28	64.35	1.60
1.0	45.77	0.89	68.93	1.61	52.38	1.80	52.78	1.47	52.94	1.63
1.1	40.00	0.89	62.10	3.42	47.68	3.43	46.14	4.87	49.00	2.40
1.2	37.35	0.93	58.24	4.67	45.33	5.70	43.6	7.38	46.72	4.07
1.3	35.75	1.00	55.40	4.76	43.26	8.00	41.86	9.48	44.63	6.01

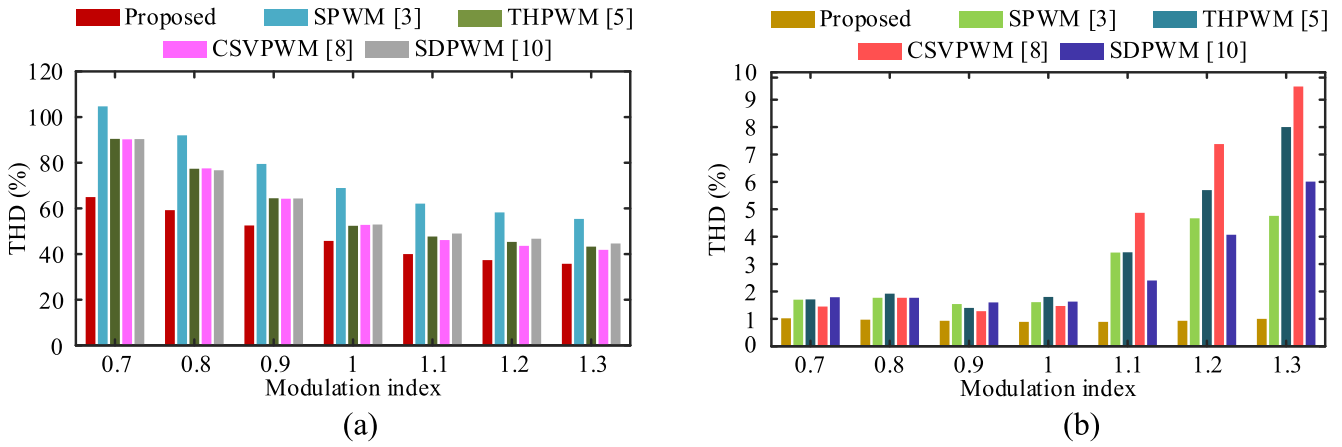

FIGURE 11. THD comparison among different PWM techniques for varying modulation index: (a) non-filtered voltage THD and (b) filtered voltage THD.

existing SPWM, THPWM, CSVPWM, and SDPWM techniques, respectively. Table 3 summarizes the overall THDs with numerical values for SPWM, THPWM, CSVPWM, SDPWM, and the proposed hybrid PWM techniques with modulation index variations. For modulation index 1, the THD is found to be acceptable as compared to lower or higher modulation indices as cleared from Table 3.

From Fig. 10, Fig. 11, Table 2 and Table 3, it is evident that the proposed hybrid PWM technique offers low THD with the variation of carrier frequency and modulation index as compared to existing SPWM, THPWM, CSVPWM, and SDPWM techniques.

C. POWER LOSS COMPARISON WITH EXISTING PWM TECHNIQUES

Conduction loss and switching loss are both a part of inverter loss. Switch conduction and anti-parallel diode conduction cause conduction loss for an IGBT module. Switch activation, switch deactivation, and diode activation and deactivation are the causes of switching loss. The turn-on loss for contemporary fast-recovery diodes is quite small. IGBT data sheets that correspond to the loss of the inverter are utilized to conduct loss analysis. Using the curve fitting tool in MATLAB, a 5th order polynomial equation is determined using the characteristic curves from the datasheet. The 5SNA

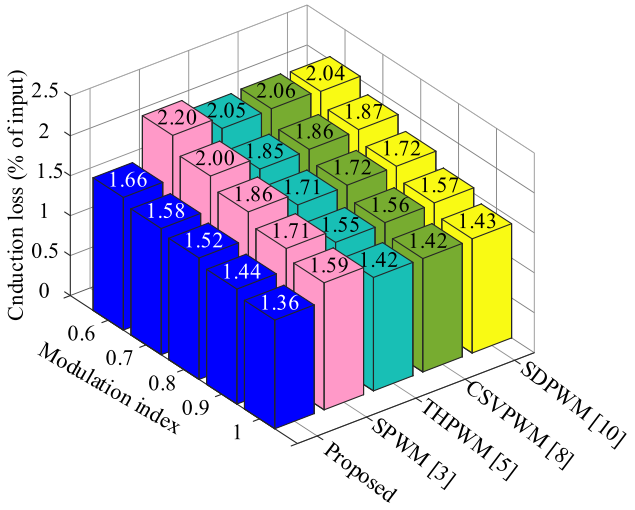

FIGURE 12. Conduction loss comparison for different PWM techniques with varying modulation index.

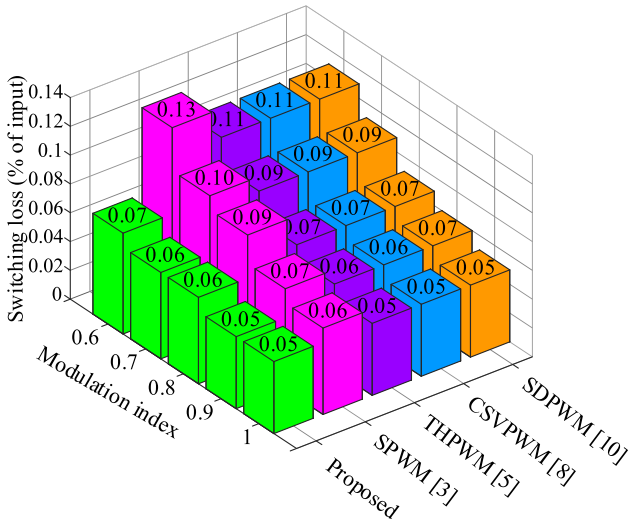

FIGURE 13. Switching loss comparison for different PWM techniques with varying modulation index.

1220G450300 IGBT module from ABB Hipak is used for the loss analysis of the VSI. Table 4 shows the conduction and switching losses of SPWM, THPWM, CSVPWM, SDPWM and the proposed hybrid PWM technique with the variation of modulation index. Figs.12-14 show the switching loss (P_{SL}), conduction loss (P_{CL}), and total power loss (P_{TL}) of the VSI for SPWM, THPWM, CSVPWM, SDPWM and the proposed hybrid PWM techniques with the variation of modulation index. The proposed hybrid PWM technique exhibits 14.46% better performance in terms of conduction loss and 16.66% improvement in switching loss compared to SPWM technique as cleared from Fig. 12 and Fig. 13, respectively. The total power loss is the sum of conduction and switching losses. SPWM technique shows the highest

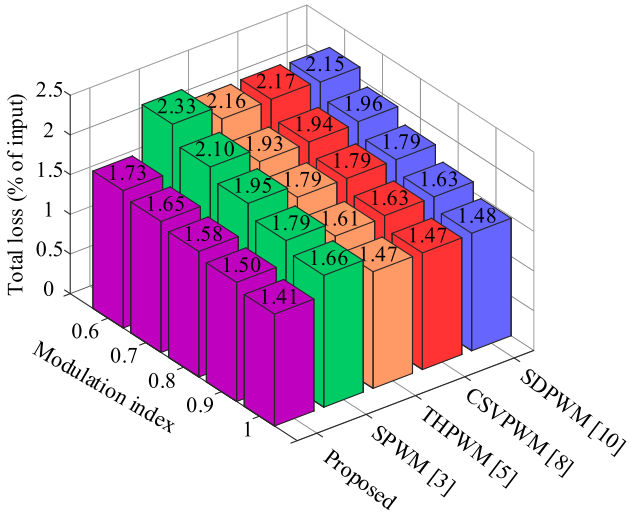

FIGURE 14. Total power loss comparison for different PWM techniques with varying modulation index

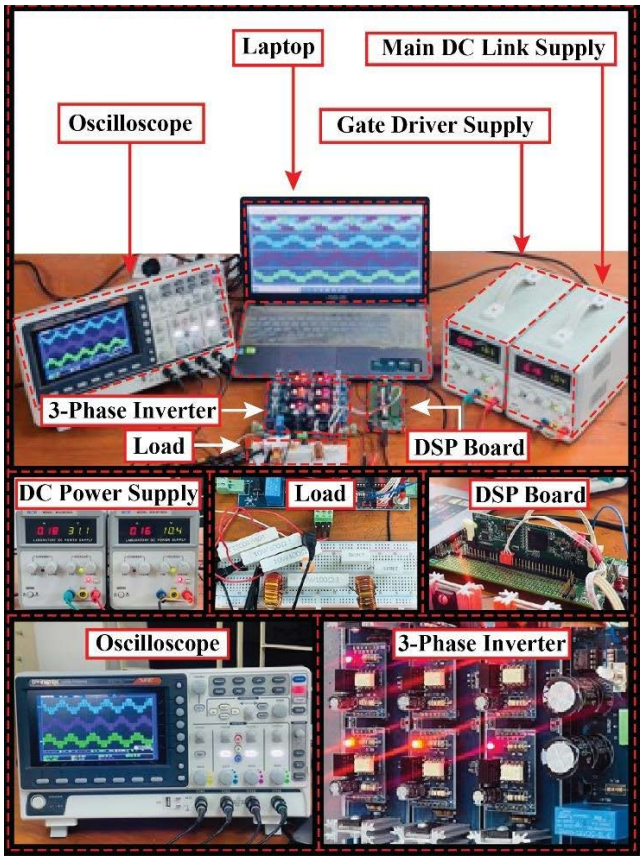

FIGURE 15. Photograph of the experimental test rig.

total power loss among the existing PWM techniques. The proposed hybrid PWM technique shows 15.06% improvement of power loss over SPWM technique as depicted in Fig. 14. The proposed hybrid PWM technique exhibits 4.08% improvement over both THPWM and CSVPWM techniques

TABLE 4. Power loss comparison with among different PWM techniques.

MI	Proposed			SPWM [3]			THPWM [5]			CSVPWM [8]			SDPWM [10]		
	P_{CL} (% of input)	P_{SL} (% of input)	P_{TL} (% of input)	P_{CL} (% of input)	P_{SL} (% of input)	P_{TL} (% of input)	P_{CL} (% of input)	P_{SL} (% of input)	P_{TL} (% of input)	P_{CL} (% of input)	P_{SL} (% of input)	P_{TL} (% of input)	P_{CL} (% of input)	P_{SL} (% of input)	P_{TL} (% of input)
0.6	1.66	0.07	1.73	2.20	0.13	2.33	2.05	0.11	2.16	2.06	0.11	2.17	2.04	0.11	2.15
0.7	1.58	0.06	1.65	2.00	0.10	2.10	1.85	0.09	1.93	1.86	0.09	1.94	1.87	0.09	1.96
0.8	1.52	0.06	1.58	1.86	0.09	1.95	1.71	0.07	1.79	1.72	0.07	1.79	1.72	0.07	1.79
0.9	1.44	0.05	1.50	1.71	0.07	1.79	1.55	0.06	1.61	1.56	0.06	1.63	1.57	0.06	1.63
1	1.36	0.05	1.41	1.59	0.06	1.66	1.42	0.05	1.47	1.42	0.05	1.47	1.43	0.05	1.48

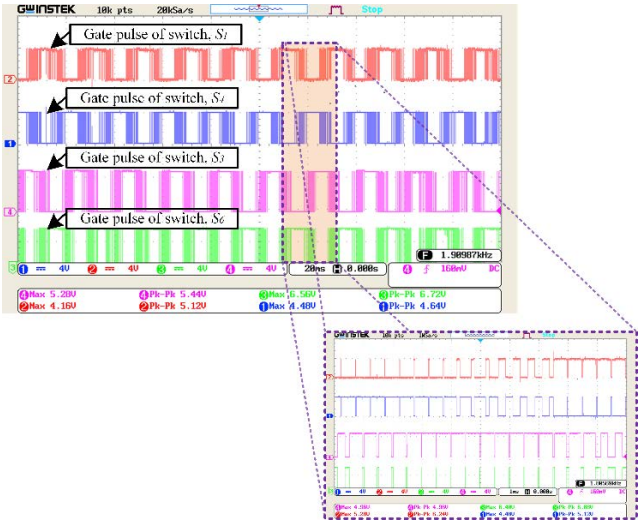

FIGURE 16. Experimental gate pulses for the IGBTs utilizing the proposed hybrid PWM technique.

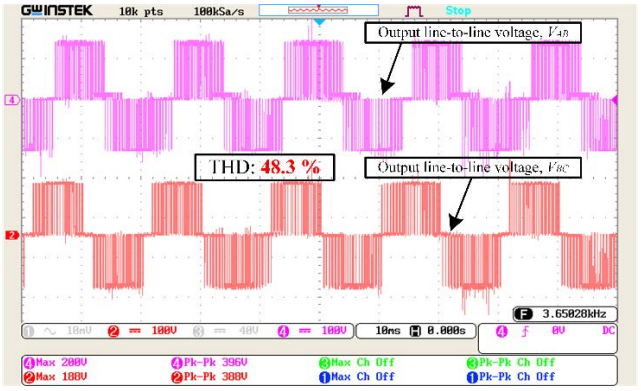

FIGURE 17. Experimental line-to-line voltage waveforms of the inverter with the proposed hybrid PWM technique.

and 4.72% improvement over SDPWM technique in terms of total inverter loss as cleared from Fig. 14. Table 4 summarizes the results of power loss analysis for different PWM techniques. From Table 4, it is evident that the proposed hybrid PWM technique performs better in terms of switching, conduction, and total inverter power loss as compared to existing SPWM, THPWM, CSVPWM, and SDPWM techniques.

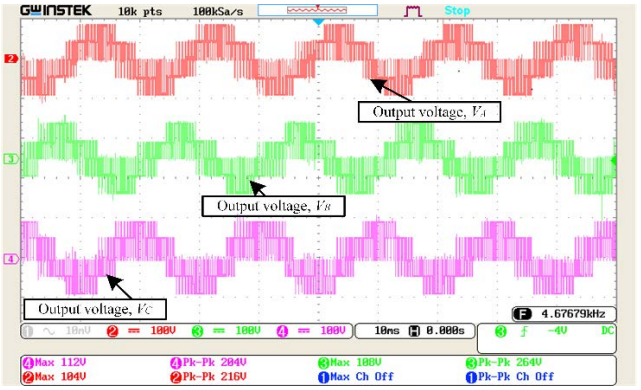

FIGURE 18. Experimental phase voltage waveforms of the inverter with the proposed hybrid PWM technique.

VI. EXPERIMENTAL VALIDATION

For the experimental validation of the proposed modulation technique, a reduced scale laboratory prototype is implemented. A photograph of the experimental test rig is shown in Fig. 15. 600V, 15A G15N60 N-channel IGBTs from Fairchild Semiconductors are utilized to construct the inverter. A GDS-1104B four channel oscilloscope is used to observe the experimental waveforms of the presented setup. Gate pulses are produced using the proposed PWM technique, which is also implemented in MATLAB/Simulink, and Simulink block sets are dumped into TMS320F28335 DSP control card digital I/O ports. For real-time interface applications, the GPIO ports provide 88 output pins.

The TLP 250 driver is supplied with the generated pulses from the TMS320F28335 DSP control card. The PWM pulse pattern will be boosted by the gate driver from 5 V to 15 V since 15V pulses are more suited to turning on the power switches. The DC input voltage of the inverter is set as 100V during the experiment. The results are validated at steady state condition and also performed with resistive load. The generated gate drive signals utilizing the proposed PWM technique is shown in Fig. 16. The four gate pulses of Fig. 16 correspond to the gate signals of S_1, S_4, S_3, and S_6 IGBTs.

The inverter line-to-line voltages are depicted in Fig. 17. The experimental THD is calculated by processing the CSV file of oscilloscope in MATLAB/Simulink environment with the aid of SimPowerSystems toolbox. The experimental THD

for the line-to-line voltage of the inverter is recorded 48.30% whereas the simulated line-to-line voltage THD was 45.77%. So, it can be said that the experimental result agrees well with the simulated result. The experimental phase voltage waveforms are also shown in Fig. 18 for the proposed hybrid PWM technique.

VII. CONCLUSION

This paper proposes a hybrid PWM technique for a VSI. The proposed hybrid PWM technique introduces a composite harmonic injected modulating signal along with a new carrier signal. The unfiltered and filtered THDs are 45.77% and 0.89%, respectively for the proposed hybrid PWM technique which is a significant improvement as compared to existing PWM schemes. The proposed hybrid PWM technique also reduces the inverter power loss as compared to existing PWM schemes. The conduction and switching power loss for the proposed hybrid PWM technique are 1.36% and 0.05% of input power, respectively which are lower than those of existing SPWM, THPWM, CSVPWM, and SDPWM techniques. By minimizing the total power loss of the VSI, the proposed hybrid PWM technique can reduce the switching stress and thermal breakdown. Thus, the proposed hybrid PWM technique can be considered as the best candidate for different power converter applications where reduction of THD and power losses are the major crucial issues.

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