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RESEARCH ARTICLE

Two New Common Ground Extended-Boost Active Quasi Z-Source Inverter With Reduced Passive Components

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ABSTRACT A high voltage gain inverter is a critical component of any high voltage power system, which feeds from a limited DC source. Numerous inventive solutions proposed to increase the boost factor. However, many of them have a large number of components and no short circuit immunity. While retaining the inherent characteristics of conventional quasi Z-source inverters (qZSI) with fewer components, this paper proposes two new active impedance source inverters based on qZSIs that utilize an additional active switch. In addition to the inherent benefits of qZSIs, the proposed topologies have a higher boost capability. They have an additional degree of freedom that allows the voltage ratio of the capacitors adjusted to any desired value without affecting the gain of the converter. They can also control the dc-link voltage without being fully dependent on the shoot-through time duration, resulting in a higher utilization factor for the dc-link. Additionally, the proposed topologies establish a common-ground connection between the input and output terminals, which is useful for some applications. In order to drive the inverters' boost factor, the operation and steady-state analysis described. Furthermore, the comparative analysis done to illustrate the features of proposed topologies. Finally, a simulation and experimental analysis carried out to validate that the proposed inverters are feasible.

INDEX TERMS Active impedance source, high boost, modified quasi Z-source inverter, two-level inverter.

I. INTRODUCTION

In addition to electromagnetic interference (EMI), the ability to only perform buck operation and the need to provide dead-time to the bridge's legs are two of the most significant drawbacks of systems that use conventional voltage source inverters (VSI). The DC-DC power stage is the conventional method for boosting low-level DC voltage. Since two-stage conversion resulted in low efficiency, Peng [1] was the first to introduce Z-source inverters (ZSI). ZSIs provide EMI immunity and enhance reliability by eliminating dead-time and enabling buck-boost power conversion in a single stage. Nonetheless, this solution hampered by start-up inrush current, a high passive component rating, a discontinuity of input current, and the absence of a common ground between the input and output of the impedance source. The quasi Z-source inverter (qZSI) was introduced in [2] as a means of overcoming these drawbacks without sacrificing the benefits.

It inherits all the advantages of ZSI and none of the aforementioned disadvantages. Several types of high-boost modifications presented in order to increase the boost factor by adding extra capacitors, inductors, and diodes to the traditional ZSI/qZSIs. Reference [3], [4], [5], [6], [7], and [8]. The mains are referred to as diode-assisted [3], capacitor-assisted [5], and switched-inductor [8] buck-boost inverters. As shown in Fi. 1, these topologies utilize numerous components, which increases the cost and size.

Using a transformer-based ZSI/qZSI structure [9] is another potential solution; however, these structures degrade the signal quality by generating spikes at the DC-link due to transformer leakage inductance. Thanks to an additional active switch, switched boost inverters (qSBI) can provide the same features with fewer passive components, resulting in a more efficient cost-benefit ratio and a smaller

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inverter [10]. Among them is the utilization of switched capacitor (SC) technique. The SC technique employs a lesser number of DC sources in accordance with the voltage across the capacitor [11]. Based on how the impedance network formed by combining passive and active elements with the new active switch, [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22] present a series of high-gain switch boost inverters. The topologies presented in [12] and [13] are based on the switched capacitor technique, and despite having a high gain, they employ a large number of components. The same issue that exists in the majority of presented topologies.

This paper presented two new topologies as a potential solution by adding one switch and one diode to the traditional qZSI: continuous current current active quasi Z-source inverter (CC-AqZSI) and discontinues current active quasi Z-source inverter (DC-AqZSI). These topologies have an additional degree of freedom because of the additional switch, allowing the voltage gain and modulation index adjusted independently of the shoot-through time. This feature allows the capacitors' voltage to be set to the desired level, which is useful for establishing an adjustable midpoint.

The structure of the reminder of the paper is as follows: Section II presents the structure of topologies. Section III discusses the steady-state operating principle analysis and the derivation of the boost factor. Section IV contains the parameter design guidelines. Small-signal analysis and comparison of characteristics with other high boost inverters presented in Sections V and VI, respectively. Section VII is where simulation and experimental verification take place. Finally, Section VIII contains the conclusion.

II. CONFIGURATION OF THE PROPOSED TOPOLOGY

The proposed inverter topology depicted in Fig. 2. The boost factor of both topologies is the same, as will be demonstrated later; however, the CC-AqZSI has a continuous input current, whereas the DC-AqZSI has a lower stress voltage on the input capacitor. The structure of these topologies is straightforward and has the same number of components. They made up of a traditional qZS (L_1, L_2, C_1, C_2 and D_1), an extra switch (Sd), diode D_2, a standard three-phase, two-level bridge (Sij, where i= 1 to 2 and j=a, b, c), an output filter (L_f, C_f) and a three-phase load resistance R. CC-AqZSI, thanks to the series input inductance, can suppress inrush current during startup, whereas DC-AqZSI has a lower capacitance stress voltage.

III. OPERATION PRINCIPLE OF THE SUGGESTED INVERTER

In this section, the operating principles of these two topologies thoroughly described and discussed. To simplify the analysis, we assume that all AqZSIs components are ideal and that all passive components are linear, time-invariant, and frequency-independent. The dead time intervals are short enough to be ignored, and the impedance network's capacitances are sufficient to keep the capacitor's voltage constant.

There are two distinct operating modes for the inverter: non-ST and ST. The equivalent circuits of these modes for CC-AqZSI and DC-AqZSI depicted in Fig. 3 and 4, respectively. As shown in Fig. 2 and 3, the most significant difference between these topologies and the conventional structure is that in the proposed structure, the inductor L_2 can be in either charging mode (d1-state) or non-charging mode (d2-state) without needing AqZSI to operate in shoot-through mode. The operational principles of the proposed AqZSIs described by the switching states listed in Table 1.

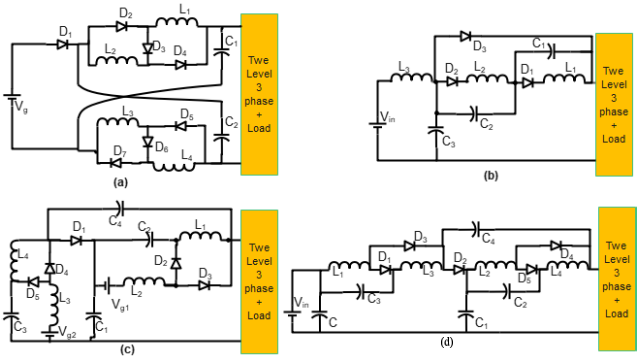

FIGURE 1. Some traditional high gain impedance source Inverters: (a) Switched-inductor ZSI [4], (b) Extended-Boost ZSI [5], (c) Embedded Switched-Inductor qZSI [6], (d) Enhanced-boost qZSI [7].

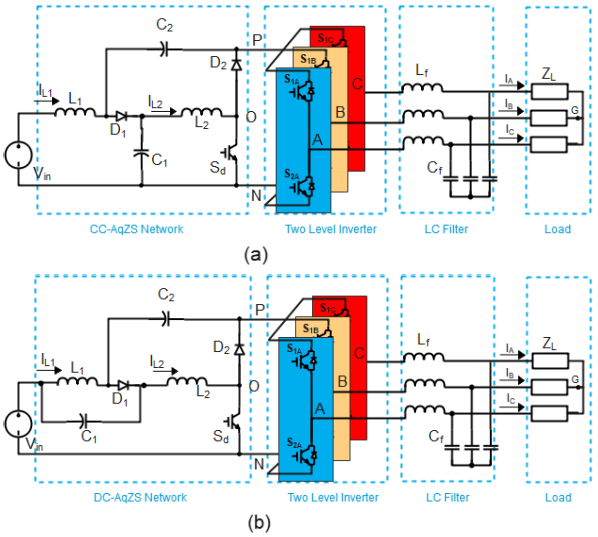

FIGURE 2. Proposed topology with (a) continuous input current (CC-AqZSI), (b) discontinuous input current (DC-AqZSI).

TABLE 1. Switching status and system output during different modes.

State		Switch			Diode		V_{xN}
		S_{1x}	S_{2x}	S_d	D_1	D_2	
d1-state	P	on	off	Off	on	on	$V_{C1}+V_{C2}$
	N	off	on				0
d2-state	P	on	off	on	on	off	$V_{C1}+V_{C2}$
	N	off	on				0
ST-state		on	on	On/Off	off	on	0

A. SHOOT-THROUGH OPERATING MODE

The ST-mode for CC-AqZSI is depicted in Fig. 3(c) and 3(d) where type-1 and type-2 indicate wether S_d is turned on and off. In this mode, all power switches (S_{ij}) are turned on and conducted simultaneously from at least a phase leg of the bridge. In ST-mode, the voltage of S_d is zero, and whether it is on or off has no effect, as there is no power transfer to the load. Inductor L_1 energized through both input voltage source and capacitor C_2, while capacitor C_1 discharges energy to inductor L_2. Also, unlike D_2, diode D_1 is reverse-biased. The time interval of ST-mode is $d_{ST}.T_S$, where d_{ST} is the ST time duty ratio of the inverter bridge and T_S is the switching period.

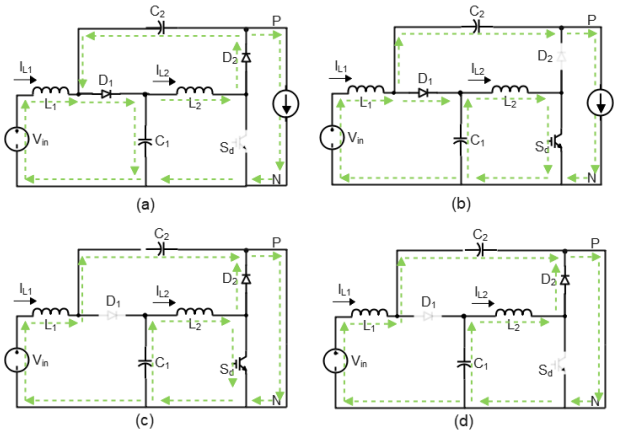

FIGURE 3. Equivalent circuits of the CC-AqZSI Topology. (a) Non-shoot-through-d1 state, (b) Non-shoot-through-d2 state, (c) Shoot-through state type 1, (d) Shoot-through state type 2.

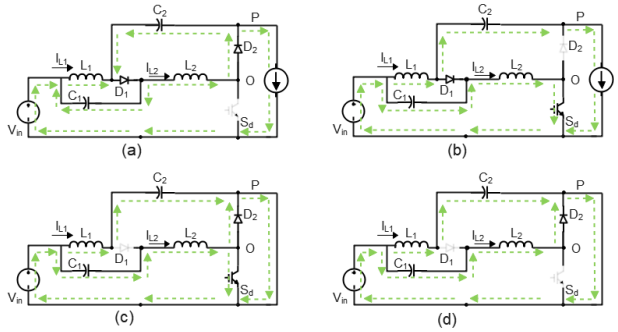

FIGURE 4. Equivalent circuits of the DC-AqZSI Topology. (a) Non-shoot-through-d1 state, (b) Non-shoot-through-d2 state, (c) Shoot-through state type 1, (d) Shoot-through state type 2.

As shown in Fig. 4(a) and 4(b), the operation principle of DC-AqZSI is similar to that of CC-AqZSI, with the exception that inductor $\boldsymbol{L_2}$ charged by both $\boldsymbol{C_1}$and the input voltage source. The following equations obtained by using KVL and KCL for CC-AqZSI and DC-AqZSI, respectively

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = V_{in} + V_{c2} \\ L_2 \dfrac{d_{iL2}}{dt} = V_{c1} \\ \hat{V}_{PN} = 0 \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{d_{Vc1}}{dt} = -i_{L2} \\ C_2 \dfrac{d_{Vc2}}{dt} = -i_{L1} \end{cases} \tag{1}$$

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = V_{in} + V_{c2} \\ L_2 \dfrac{d_{iL2}}{dt} = V_{in} + V_{c1} \\ \hat{V}_{PN} = 0 \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{d_{Vc1}}{dt} = -i_{L2} \\ C_2 \dfrac{d_{Vc2}}{dt} = -i_{L1} \end{cases} \tag{2}$$

B. NON-SHOOT-THROUGH OPERATING MODE

d1-state:

Fig. 3(a) and 4(a) depict the equivalent circuit of d_1-state for CC-AqZSI and DC-AqZSI, respectively. As illustrated, there is no short-circuit in the bridges for this state, and the switch S_d is open. There is no difference between this state and that of traditional qZSIs because the extra diode D_2 is conducting and has no effect on the circuit. The time interval of this operating mode is $d_1 \cdot T_S$. By applying KVL and KCL for this state, voltage and current relations extracted as (3) and (4) for CC-AqZSI and DC-AqZSI, respectively

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = V_{in} - V_{c1} \\ L_2 \dfrac{d_{iL2}}{dt} = -V_{c2} \\ \hat{V}_{PN} = V_{C1} + V_{C2} \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{d_{Vc1}}{dt} = i_{L1} - i_{PN} \\ C_2 \dfrac{d_{Vc2}}{dt} = i_{L2} - i_{PN} \end{cases} \tag{3}$$

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = -V_{c1} \\ L_2 \dfrac{d_{iL2}}{dt} = -V_{c2} \\ \hat{V}_{PN} = V_{C1} + V_{C2} + V_{in} \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{d_{Vc1}}{dt} = i_{L1} - i_{PN} \\ C_2 \dfrac{d_{Vc2}}{dt} = i_{L2} - i_{PN} \end{cases} \tag{4}$$

where i_{PN} is the average DC-link current in non-ST modes [15].

d2-state:

In this mode, there is no short-circuit in the bridges and switch S_d is turned on, as Fig. 3(b) and 4(b) show, same as ST-state, inductor L_2 is in charging mode, Diode D_2 is reverse-biased and the rest of circuit is the same as d_1-state. The time interval of this operating mode is $d_2 \cdot T_S$, where d_2 is the time during which S_d is conducting. During non-shoot-through-d_2 state, it is possible to extract inductor voltages and capacitor currents as (5) and (6) for CC-AqZSI and DC-AqZSI, respectively

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = V_{in} - V_{c1} \\ L_2 \dfrac{d_{iL2}}{dt} = V_{c1} \\ \hat{V}_{PN} = V_{C1} + V_{C2} \\ C_1 \dfrac{d_{Vc1}}{dt} = i_{L1} - i_{L2} - i_{PN} \\ C_2 \dfrac{d_{Vc2}}{dt} = -i_{PN} \end{cases} \tag{5}$$

$$\begin{cases} L_1 \dfrac{d_{iL1}}{dt} = -V_{c1} \\ L_2 \dfrac{d_{iL2}}{dt} = V_{c1} + V_{in} \\ \hat{V}_{PN} = V_{C1} + V_{C2} + V_{in} \\ C_1 \dfrac{d_{Vc1}}{dt} = i_{L1} - i_{L2} - i_{PN} \\ C_2 \dfrac{d_{Vc2}}{dt} = -i_{PN} \end{cases} \tag{6}$$

C. BOOST FACTOR CALCULATION

The voltage gain of CC-AqZSI is deduced by applying voltage balance law across the inductors and taking into account that each periodic time is divided into three parts of d_1, d_2, and d_{st}.

$$d_1 + d_2 + d_{st} = 1 \tag{7}$$

$$V_{C1}\,(d_{st} + d_2) = d_1 V_{C2} \tag{8}$$

$$(V_{in} + V_{C2})\,d_{st} + (V_{in} - V_{C1})\,(d_1 + d_2) = 0 \tag{9}$$

Considering (7)–(9), the voltage of the capacitors calculated as follows

$$\begin{cases} V_{C1} = \dfrac{d_1}{d_1 - d_{st}} V_{in} \\ V_{C2} = \dfrac{1 - d_1}{d_1 - d_{st}} V_{in} \end{cases} \tag{10}$$

Using the same method for DC-AqZSI, we have

$$\begin{cases} (V_{in} + V_{C2})\,d_{st} = (d_1 + d_2) V_{C1} \\ (V_{in} + V_{C1})\,(d_{\mathrm{st}} + d_2) = d_1 V_{C2} \end{cases} \tag{11}$$

$$\begin{cases} V_{C1} = \dfrac{d_{st}}{d_1 - d_{st}} V_{in} \\ V_{C2} = \dfrac{1 - d_1}{d_1 - d_{st}} V_{in} \end{cases} \tag{12}$$

Consequently, for both topologies, the dc-link voltage and boost factor B of the inverter calculated as

$$\hat{V}_{PN} = \frac{V_{in}}{d_1 - d_{st}} \tag{13}$$

$$B = \frac{\hat{V}_{PN}}{V_{in}} = \frac{1}{d_1 - d_{st}} \text{ where } \begin{cases} 0 \le d_{st} \le \dfrac{1}{2} \\ d_{st} \le d_1 \le 1 - d_{st} \end{cases} \tag{14}$$

The inverter's inversion voltage gain G defined as

$$G = M.B = \frac{\hat{V}_o}{V_{in}} \tag{15}$$

where $\hat{V}_o$ denotes the peak load voltage, and M is the modulation index. The relationship between M and B is determined by the PWM control strategy used. In this paper, like [14], the simple boost control (SBC) is applied. As a result, the modulation index is constrained by the ST duty ratio, as illustrated bellow

$$M \le 1 - d_{st} \tag{16}$$

By considering the highest modulation index, the maximum peak load voltage can be extracted as

$$\hat{V}_{o\_max} = \frac{\bar{V}_{PN}}{2} = (1 - d_{st})\frac{\hat{V}_{PN}}{2} \tag{17}$$

where $\bar{V}_{PN}$ is the mean voltage of the inverter dc-link.

As it is evidenced from (9) and (11), the most significant contribution of the proposed topology is the addition of one degree of freedom to the impedance network, which increases the gain factor while simultaneously controlling the capacitors voltage level. This contribution makes these topologies useful for some symmetric and asymmetric multilevel inverters, needing a controlled midpoint besides boosting input voltage. In this regard, three-level diode clamped inverter, four-leg, and fault-tolerant inverters are some examples of applications for which the proposed topologies can be helpful.

IV. INDUCTOR AND CAPACITOR DESIGN

Due to the operation principles, inductor currents are influenced by the ST state and rise rapidly. The current ripple of inductors and the associated value of inductors can be calculated using (1-6), (9), and (11) as below for CC-AqZSI and DC-AqZSI respectively.

$$\begin{cases} \Delta i_{\mathrm{L1}} = \dfrac{d_{st}}{n f_s L_1}(V_{in} + V_{C2}) \\ \Delta i_{\mathrm{L2}} = \dfrac{(d_{st} + d_2)}{n f_s L_2} V_{C1} \\ L_1 = \dfrac{d_{st}(1 - d_{st})B}{n f_s \Delta i_{\mathrm{L1}}} V_{in} \\ L_2 = \dfrac{d_1(1 - d_1)B}{n f_s \Delta i_{\mathrm{L2}}} V_{in} \end{cases} \tag{18}$$

$$\begin{cases} \Delta i_{\mathrm{L1}} = \dfrac{d_{st}}{n f_s L_1}(V_{in} + V_{C2}) \\ \Delta i_{\mathrm{L2}} = \dfrac{(d_{st} + d_2)}{n f_s L_2}(V_{in} + V_{C1}) \\ L_1 = \dfrac{d_{st}(1 - d_{st})B}{n f_s \Delta i_{\mathrm{L1}}} V_{in} \\ L_2 = \dfrac{d_1(1 - d_1)B}{n f_s \Delta i_{\mathrm{L2}}} V_{in} \end{cases} \tag{19}$$

where n is the number of shoot-through states that happen in one switching period. Operation principle shows unlike conventional qZS networks, the charging times of inductors are different. Same as capacitors voltage, by applying the amp-second balance property of capacitors C_1 and C_2, the average current across inductors in steady-state is calculated as follows.

$$I_{L1} = I_{L2} = \frac{1 - d_{st}}{d_1 - d_{st}} I_{PN} \text{ and } I_{PN} = \frac{\hat{V}_{PN}}{R_L} \tag{20}$$

where R_L is the ac side circuit's simplified equivalent, DC load [23]. By these considerations, the average inductors'

current, which is equal to the average current of the input source, derived as follows

$$I_{L1} = I_{L2} = \frac{(1 - d_{st})B^2}{R_L} V_{in} \tag{21}$$

Further, concerning (1-6), (9) and (11), for both topologies, capacitors' voltage ripple and therefore, the corresponding capacities extracted as follows

$$\begin{cases} \Delta V_{C1} = \dfrac{I_{L2}(d_{st} + d_2)}{nf_s C_1} \\ \Delta V_{C2} = \dfrac{(I_{L2} - I_{PN})d_1}{nf_s C_2} \\ C_1 = \dfrac{(1 - d_{st})(1 - d_1)B^2}{nf_s \Delta V_{C1} R_L} V_{in} \\ C_2 = \dfrac{(1 - d_1) d_1 B^2}{nf_s \Delta V_{C2} R_L} V_{in} \end{cases} \tag{22}$$

V. SMALL-SIGNAL DYNAMIC ANALYSIS AND CONTROL METHODOLOGY

For small-signal analysis, the output load simplified further by modeling it as a simplified equivalent dc-inductive load [23]. In this circumstance, the voltage and current of the load are identical to those of the dc-link. Using the procedure outlined for small-signal analysis in [23], the transfer function of capacitor voltage with respect to $\boldsymbol{d_{st}}$ **(s)**, after the necessary simplifications, is as follows.

$$\begin{cases} sL_1 i_{L1}(s) = (V_{C1} + V_{C2})\, d_{st}(s) + (D_{st} - 1)\, v_{c1}(s) \\ +D_{st} v_{c2}(s) + V_{in}(s) \\ sL_2 i_{L2}(s) = (1 - D_1)\, v_{c1}(s) - D_1 v_{c2}(s) \\ sC_1 v_{C1}(s) = \left(I_{pn} - I_{L1}\right) d_{st}(s) + (1 - D_{st})\, i_{L1}(s) - \\ (1 - D_1)\, i_{L2}(s) + (D_{st} - 1)\, i_{pn}(s) \\ sC_2 v_{C2}(s) = \left(I_{pn} - I_{L1}\right) d_{st}(s) - D_{st} i_{L1}(s) + \\ D_1 i_{L2}(s) + (D_{st} - 1)\, i_{pn}(s) \\ sL_{pn} i_{pn}(s) = -(V_{C1} + V_{C2})\, d_{st}(s) + (1 - D_{st}) v_{c1}(s) + \\ (1 - D_{st}) v_{c2}(s) - R_{pn} i_{pn}(s) \end{cases} \tag{23}$$

$$\left.\frac{v_{c1}(s)}{d_{st}(s)}\right|_{v_{in}=0} = \frac{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{24}$$

Fig. 5 depicts the Bode plot of the system described as (20), for two different input voltages, in order to analyze the stability of the proposed. As evidenced, at the crossing frequency, the slope of the graph is -20db/dec and all the poles of the system are located on the left side, proving that the system is stable for different inputs.

For the AqZSI as with other standard qZSIs, the ac-side can be controlled independently of the dc-side; therefore, the method described in [24] has been employed for this purpose. Given that this voltage is not continuous, it is not possible to obtain direct feedback from the dc-link in order to control it. To solve this problem, the voltage of the capacitors is used. The block diagram of the dc-side control method depicted in Fig. 5(b). Due to the non-minimum phase property of the capacitor voltage, the inductor reference current is initially determined by a PI controller and then fed to a second controller, which determines the final value of d_{st}. In each of these stages, the value of d_1 is constant and predetermined.

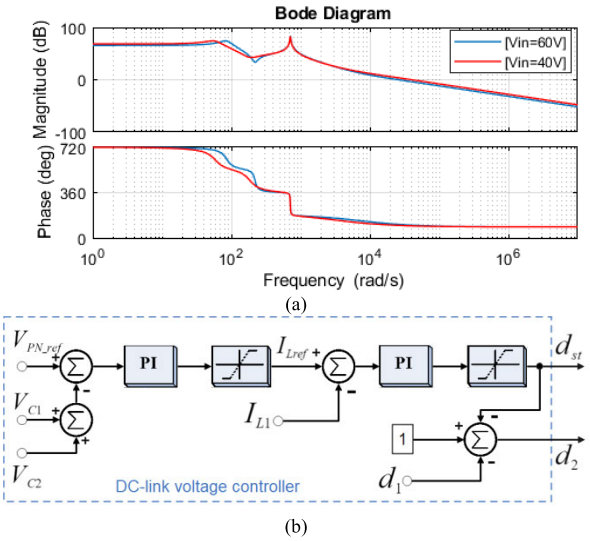

FIGURE 5. (a) Bode plots of the Vpn/dst transfer function of the proposed topology when Vin=60V, d1=0.5, dst=0.38 and Vin=40V, d1=0.5, dst=0.42, (b) Control block diagram of the proposed topologies.

VI. PERFORMANCE COMPARISON

Utilizing an inverter with a high voltage gain at higher modulation index, preferably with fewer components, is one of the most important factors for enhancing voltage quality. In this section, several non-transformer-based high voltage gain topologies compared to the proposed inverter's characteristics, and an in-depth comparison analysis presented.

A. COMPARISON OF THE NUMBER OF ELEMENTS

Table 2 provides a comprehensive comparison between the proposed topology and other similar topologies. Fig. 1 and 2 demonstrate that, in comparison to other high voltage gain qZSI topologies that do not employ an active switch, the proposed topologies reduce the number of passive elements significantly. They simultaneously increase the boost factor. In contrast, as shown in Table 2, this topology employs fewer or an equal number of components compared to other similar topologies. The only [22] has a smaller capacitor, but it does not share a common ground between input and output terminals and instead employs numerous diodes.

B. COMPARISON OF THE BOOST ABILITY

Since the proposed topologies have one more degree of freedom, it is preferable to demonstrate the boost capability in three-dimensional space. Based on the values of d_1 and d_{st}, the boosting capability of the proposed topologies can vary

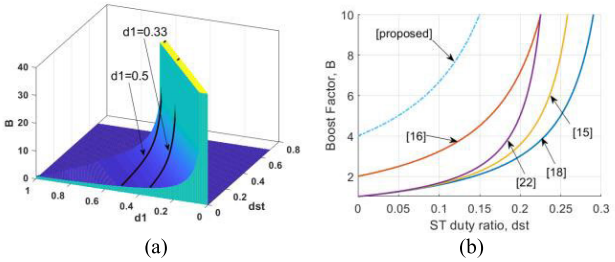

FIGURE 6. (a) Boosting ability of the proposed inverters and (b) comparison of proposed gain and other topologies.

substantially, as shown in Fig. 6(a). For instance for d_1 =0.2, the boost factor is equal to

$$B = \frac{\hat{V}_{PN}}{V_{in}} = \frac{5}{1-5d_{st}} \text{ for } d_1 = 0.2 \tag{25}$$

Although theoretical value can reach infinity, parasitic effects will limit the experimental boost factor. Fig. 6(b) compares the boosting ability of proposed topology for $\boldsymbol{d_1} = 0.25$; as shown, the boost factor of the proposed is greater than all others.

C. COMPARISON OF THE CURRENT AND VOLTAGE STRESS

Current and voltage stress of components is one of the most crucial parts of qZS inverters. Fig. 7 depicts a comparison of the current and voltage stresses of all devices utilized in various topologies. Fig. 7(a) shows the current stress of the inductors. Evidently, the majority of topologies contain inductors with unequal currents. Comparing the proposed inductor current to the maximum inductor current of other topologies reveals that, with the exception of [18], the proposed current is identical to that of all other topologies. The voltage stress on capacitors, diodes, and the additional switch depicted in Fig. 7(b), 7(c), and 7(e), respectively. As seen, in the majority of topologies, components within the same category do not have identical values, and one topology cannot be favored over another. Comparing voltage stresses reveals that the proposed topology has acceptable voltage stresses, and in many cases, including diodes and switches, it has less voltage stress.

Fig. 7(d), 7(f), and 7(g) depict, respectively, the current stresses of diodes, the additional switch, and the shoot-through state for all topologies.

As with voltage stresses, the proposed topology has excellent performance in this instance. In the meantime, although the shoot-through current of the proposed topology like [22] is greater than that of the others, it has the lowest current stress in the additional switch, which reduces the switch losses and improves efficiency.

D. POWER LOSS AND EFFICIENCY COMPARISON

The system losses made up of the losses of inductors, capacitors, diodes and switches utilized in the system.

1) LOSSES OF INDUCTORS

Inductors account for the majority of the system losses. Using (18) to get the rms value of inductor current, the

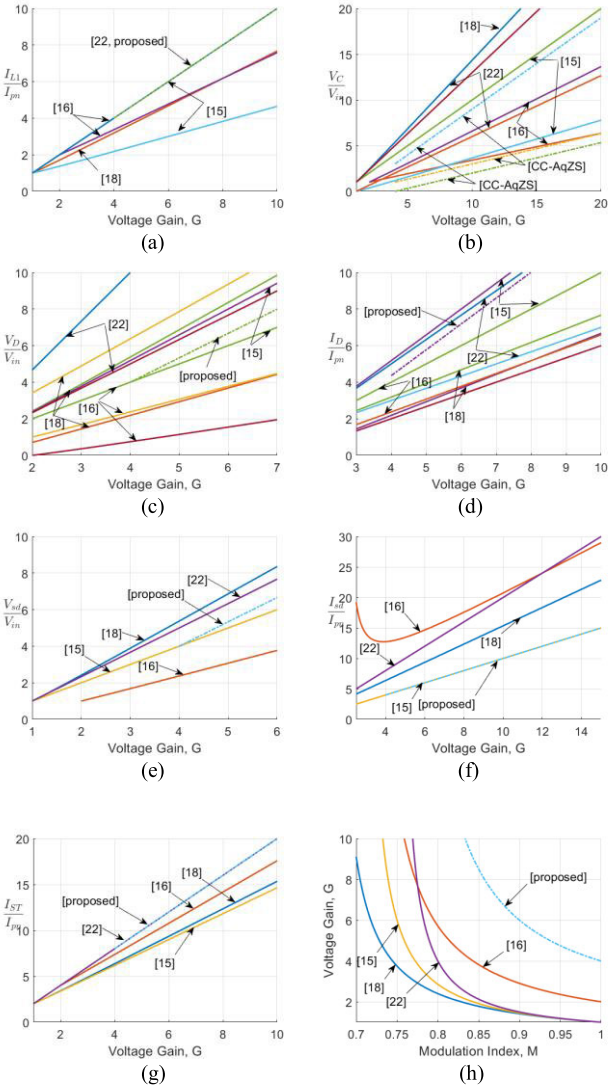

FIGURE 7. Voltage and current stresses comparison of: (a) inductor current, (b) capacitors voltage, (c) diode voltage, (d) diode current, (e) switch voltage, (f) switch current, (g) shoot through current and (h) gain vs modulation index.

inductor losses calculated as follows

$$p_L = I_{L1(rms)}^2 r_L + I_{L2(rms)}^2 r_L \Big| I_{Lrms} = \frac{p_{out}}{G^2 V_{in}} \tag{26}$$

2) LOSSES OF CAPACITORS

Capacitor current in different working modes is determined as follows

$$i_C = \begin{cases} (MB-1)I_{pn}, & d_1 \\ -I_{pn}, & d_2 \\ -MBI_{pn}, & d_{st} \end{cases} \tag{27}$$

After determining the capacitor current's rms value, its power loss estimated as follows

$$p_C = I_{C1(rms)}^2 r_{C1} + I_{C2(rms)}^2 r_{C2} \tag{28}$$

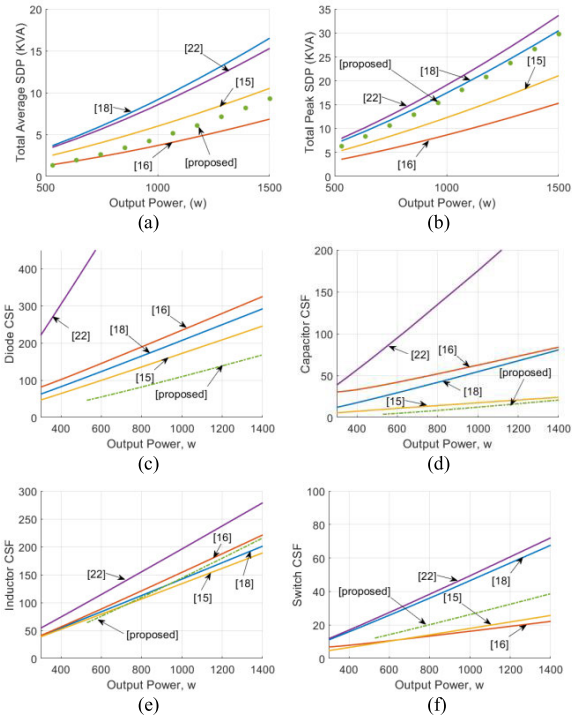

FIGURE 8. (a) Total average SDP comparison, (b) total peak SDP comparison and CSF comparison of: (c) diodes, (d) capacitors, (e) inductors, (f) switches.

3) LOSSES OF DIODES

The current of the diodes that vary from one another is equal to

$$i_{D_1} = \begin{cases} (2MB-1)\, I_{pn}, & d_1 \\ -I_{pn}, & d_2 \\ 0, & d_{st} \end{cases} \quad i_{D_2} = \begin{cases} MBI_{pn}, & d_1 \\ 0, & 1-d_1 \end{cases} \tag{29}$$

The average and rms value of the current flowing through the diodes used to calculate the three forms of losses present in diodes: a reverse recovery loss and two types of conduction power loss.

$$\begin{cases} p_{D_{rr}} = 0.5 * Q_{rr} * V_{D1} * f_s + 0.5 * Q_{rr} * V_{D2} * f_s \\ p_{V_F} = I_{D1(Avg)} V_F + I_{D2(Avg)} V_F \\ p_{r_D} = I^2_{D1(rms)} r_D + I^2_{D2(rms)} r_D \\ p_D = p_{D_{rr}} + p_{V_F} + p_{r_D} \end{cases} \tag{30}$$

where Q_{rr} represents the reverse recovery charge of the diode and f_s refers to the switching frequency.

4) LOSSES OF SWITCHES

Switch losses are divided into two categories: conduction power loss and switching power loss. The following describes the switches current in their distinct operating modes.

$$i_{sd} = \begin{cases} MBI_{pn}, & d_2 \\ 0, & 1-d_2 \end{cases} \tag{31}$$

$$i_{sb} = \begin{cases} \dfrac{MBI_{pn}}{3}, & d_{st} \\ \dfrac{4p_{out}}{3MBV_{in}cos\varphi\pi}, & 1-d_{st} \end{cases} \tag{32}$$

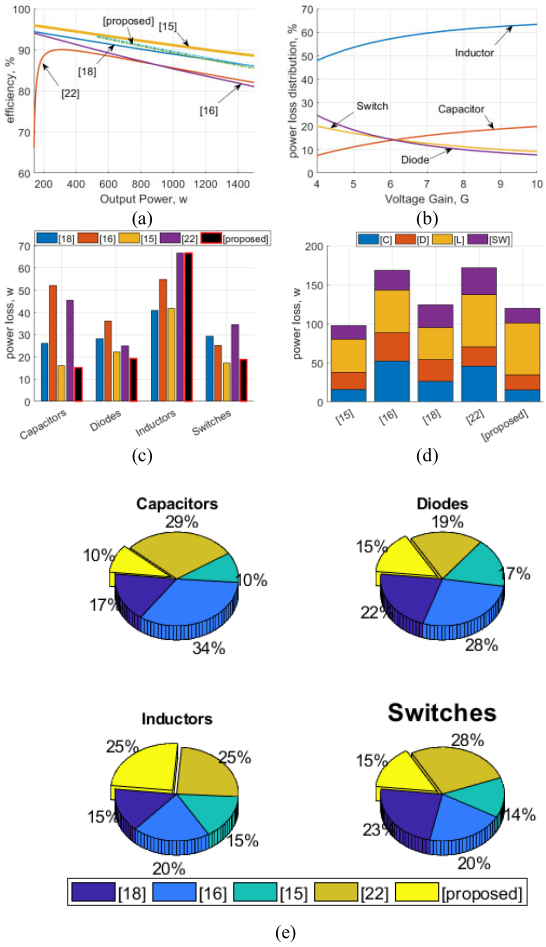

FIGURE 9. Efficiency and power loss comparisons: (a) efficiency comparison, (b) proposed topology loss distribution percentage, (c) power loss distribution comparison, (d) stacked loss comparison, (e) equipment category loss comparison for output power of 1000 w.

where i_{sd} and i_{sb} are the additional and bridge switch current respectively. Based on (27)-(28), the power losses calculated as follows

$$\begin{cases} p_{s_{rr}} = \dfrac{t_{on} + t_{off}}{2} f_s * V_s * I_s \\ p_{s_{cond}} = I^2_{s(rms)} r_s \end{cases} \tag{33}$$

The delay durations for turning switches on and off are denoted by t_{on} and t_{off}, respectively, and r_s is the drain-to-source resistance of switches.

The value of the internal parasitic parameters shown in Table 3. Based on that, Fig. 9(b) shows and compares Loss distribution percentage of the proposed topology. As observed, a significant proportion of losses related to the inductors. Fig. 9(c)-9(e) compare the losses of the proposed topology to those of the other topologies in various ways. As can be seen, the proposed topology has lower losses than the others except [15], indicating the proposed topology's relative superiority over them. Fig. 9(a) compares the efficiency of different topologies. As expected, AqZS has better efficiency than other topologies with the exception of [15].

TABLE 2. Comparison of the proposed topology with some other inverters.

	[16]	[15] HG-qSBI	[22] SCL-ASBI	[18] ASC/SL-qZSI	Proposed* DC-AqZSI	Proposed* CC-AqZSI
Boost Factor (B)	$\frac{2}{1-4d_{st}+2{d_{st}}^2}$	$\frac{1}{1-4d_{st}+2{d_{st}}^2}$	$\frac{1}{1-4d_{st}}$	$\frac{1+d_{st}}{1-3d_{st}}$	$\frac{1}{d_1-d_{st}}$	$\frac{1}{d_1-d_{st}}$
sources	1	1	1	1	1	1
Inductor	2	2	2	2	2	2
Capacitor	3	2	3	1	2	2
Diode	5	2	3	5	2	2
Switch	1	1	1	1	1	1
V_C/V_{in}	C_1: $(2M-1)B/2$; C_2,C_3: $B/2$	C_1: MB; C_2: $d_{st}B$	C_1: B; C_2,C_3: $2d_{st}B$	B	C_1: $d_{st}B$; C_2: $(1-d_1)B$	C_1: d_1B; C_2: $(1-d_1)B$
I_L/I_{PN}	L_1: MB; L_2: M^2B	L_1: MB; L_2: M(2M-1)B	MB	$\frac{MB}{2-M}$	MB	MB
V_{sd}/V_{in}	$B/2$	MB	B	B	B	B
I_{Sd}/I_{PN}	$MB/2dst$	MB	$2MB$	$2MB/(2-M)$	MB	MB
V_D/V_{in}	D_1: MB; D_2: $dstB$; D_3, D_4, D_5: $B/2$	D_1: B; D_2: MB	D_1, D_2: B; D_3: $2B$	D_1, D_2: (B-1)/2; D_3: 1+B; D_4, D_5: B	B	B
I_D/I_{PN}	D_1, D_2: MB; D_3, D_4: $B/2$; D_5: $MB/2dst$	D_1: $2M^2B$-1; D_2: MB	D_1: (2M-1)B; D_2: $2d_{st}B$; D_3: B	D_1, D_2, D_3, D_5: $MB/(2-M)$; D_4: $2d_{st}/(3M-2)$	D_1: MB-1; D_2: MB	D_1: MB-1; D_2: MB
Gain Voltage (G=MB)	$\frac{2M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{4M-3}$	$\frac{M(2-M)}{3M-2}$	$\frac{M}{M+d_1-1}$	$\frac{M}{M+d_1-1}$
Input Current	Continuous	Continuous	Discontinuous	Discontinuous	Discontinuous	Continuous
I_{ST}/I_{PN}	$M(M+1)B$	$2M^2B$	$2MB$	$2MB/(2-M)$	$2MB$	$2MB$
Common Ground	YES	NO	NO	NO	YES	YES

E. COMPONENT STRESS FACTOR (CSF) CALCULATION AND COMPARISON

One of the most effective methods for analyzing and comparing alternative topologies for a particular application is its Component stress factor (CSF). The method calculates converter stresses and provides a quantitative performance measurement. To do this, the CSF value of capacitors (CCSF), inductors (WCSF), switches (SCSF) and diodes (DCSF) is determined as follows

$$CCSF = \sum_{Capacitors} \frac{\sum_k W_k}{W_i} \cdot \frac{V_{rms}^2 I_{rms}^2}{P_{out}^2} \tag{34}$$

$$SWSF = \sum_{Windings} \frac{\sum_k W_k}{W_i} \cdot \frac{V_{avg}^2 I_{rms}^2}{P_{out}^2} \tag{35}$$

$$SCSF = \sum_{Switches} \frac{\sum_k W_k}{W_i} \cdot \frac{V_{rms}^2 I_{rms}^2}{P_{out}^2} \tag{36}$$

$$DCSF = \sum_{Diodes} \frac{\sum_k W_k}{W_i} \cdot \frac{V_{rms}^2 I_{rms}^2}{P_{out}^2} \tag{37}$$

where W_i is the given individual weight for component i and $\sum_k W_k$ is the total of the individual weight factors. Fig. 8(c)-8(f) compares the CSF values of different components of the proposed topology with other topologies. As can be observed, the suggested topology yielded the best results when compared to other topologies, with the exception of CCSF, where [15] and [16] yielded superior results. This means that the proposed topology has an appropriate current stress, reconfirming that it has more favorable qualities than the others.

F. SWITCHING DEVICE POWER (SDP) CALCULATION AND COMPARISON

The highest impressed voltage, as well as the peak and average current, are among the selection criteria for switching devices in inverters. For this regards, the SDP index developed. The SDP of a switching device or cell is the product of the voltage and current stresses and described as follows

$$Total\ AverageSDP = SDP_{Avg} = \sum_{i=1}^{n} V_{i(avg)} I_{i(avg)} \tag{38}$$

$$Total\ PeakSDP = SDP_{Peak} = \sum_{i=1}^{n} V_{i(peak)} I_{i(peak)} \tag{39}$$

In AqZS, the current that passes through the inverter is the shoot-through current during the d_{st} time period and the load current at all other periods which, owing to symmetry, is split evenly across the switches.

Using (28) and the shoot-through current value and due to the symmetry, the average current of switches derived as

$$I_{s(avg)} = \frac{2}{3} I_{L1} d_{st} + \frac{4P_{out}}{3V_{pn} cos\varphi \pi}(1-d_{st}) \tag{40}$$

The maximum voltage on the switches formed when the output power is zero and the dc-link voltage is at its maximum value. In this instance, we will have

$$SDP_{avg} = 6 * V_{s(max)} I_{s(avg)} = 6 * V_{pn} I_{s(avg)} \tag{41}$$

In addition, when the line current of phase A is at its peak and the output is short-circuited, the inverter switches'

TABLE 3. System specification.

Parameter	*Symbol*	*Value*
Rated power of qZSI	P_{load}	1 kVA
AqZS DC-link peak voltage	V_{PN}	500 V
DC source voltage	V_{in}	30V-140V
Amplitude of ac phase voltage	V_m	110 Vrms
Ac load frequency	f_{ref}	60 Hz
Switching frequency	f_s	20 kHz
AqZS Capacitors	C_1/C_2	1 mF, 110mΩ
AqZS Inductor	L_1/L_2	2 mH, 0.13Ω
AqZS Diode(FP40R12KT3)	D_1/D_2	1600V, 50A, V_f=1.2V
Switches (FP40R12KT3)	S_1~S_6/S_d	1200V, 55A, 30mΩ
Filter Inductor	L_f	3 mH/phase
Filter Capacitor	C_f	5 µF/phase
Three Phase Resistive Load	R_L	22Ω-120Ω/phase

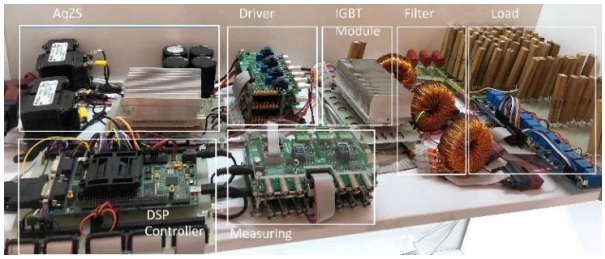

FIGURE 10. The prototype of the CC and DC- AqZSI system.

maximum current flows and we have

$$I_{s(peak)} = \frac{2}{3}I_{L1} + \frac{1}{2}I_a \text{ where } I_a = \frac{4P_{out}}{3V_{pn}cos\varphi\pi} \quad (42)$$

$$SDP_{peak} = 6 * V_{s(max)}I_{s(peak)} = 6 * V_{pn}I_{s(peak)} \quad (43)$$

Repeating this method for diodes and the additional switch yields the SDP value of the system. The average SDP and peak SDP of the proposed topology compared to those of other topologies in Fig. 8(a) and 8(b). As can be observed, the suggested topology has the lowest average SDP value, with the exception of [16]. In addition, its peak SDP value is smaller than [22] and [18]. The obtained results indicate that the proposed topology is a cost-effective and SDP-compliant option.

VII. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed topologies verified with simulation and experimental results. The simulations are done with Simulink MATLAB, while laboratory prototypes carry out the feasibility. The input voltage varies from 30 to 140 volts, and the switching frequency is set to 20 kHz. Table 3 demonstrates the circuit parameters used.

A. SIMULATION RESULTS

Fig. 10(a) depicts the simulation results of the proposed CC-AqZSI with d1=0.2, dst=0.08, and $\hat{V}_{PN}$= 500V. Since the desired peak output voltage is 155 volts (110 Vrms) for an input voltage of 60 V, as shown in Fig. 10(a), the capacitor C1 and C2 voltages are 99 and 398 volts, respectively, which are slightly lower than the values calculated in (9) due to the parasitic parameters considered in the simulation. The DC-link voltage increased to 498 V, which is consistent with the analytical results. The peak-to-peak of inductor current

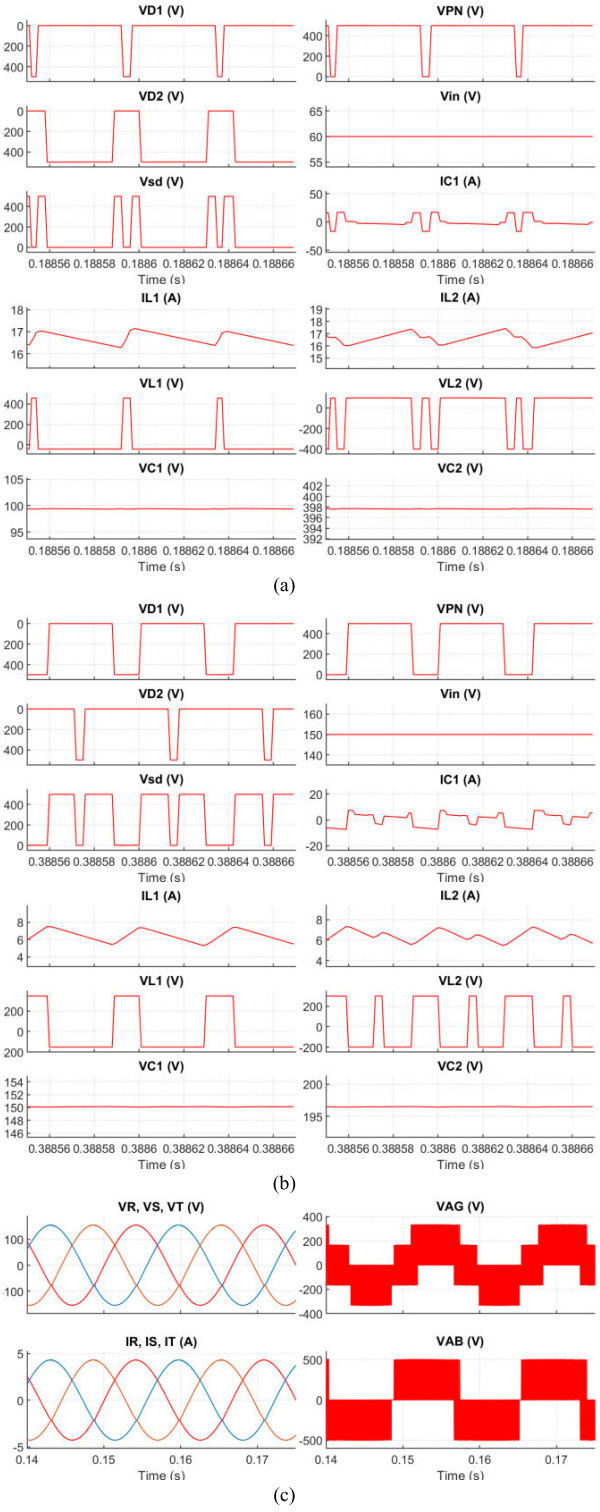

FIGURE 11. Simulation results with a resistive load of 1000 w (a) current and voltage of CC-AqZSI when Vin=60; VPN=500; d1=0.2, (b) current and voltage of DC-AqZSI when Vin=150; VPN =500; d1=0.6 (c) the output voltage and current.

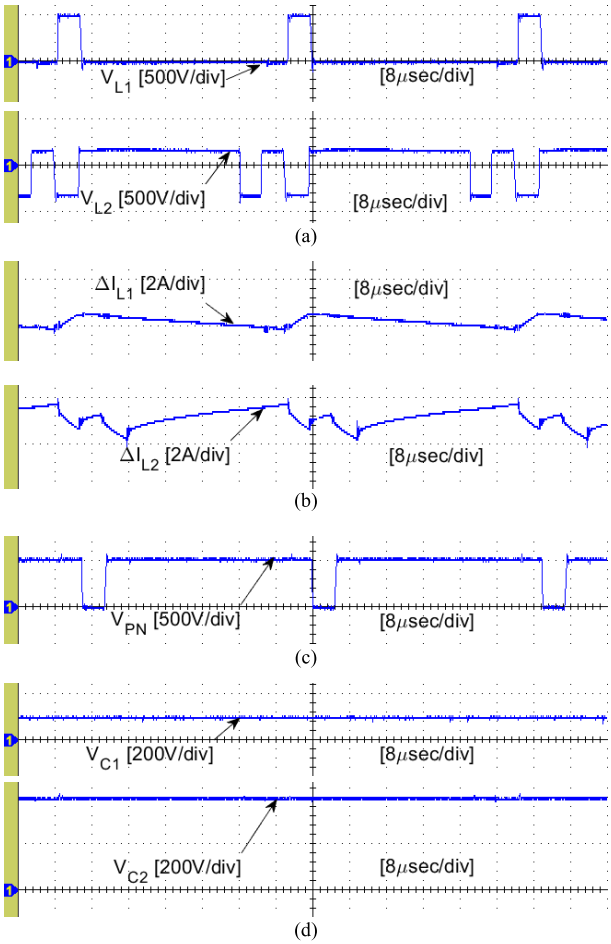

FIGURE 12. CC-AqZSI Experimental results with a resistive load of 1000 w when Vin=60; VPN =500; d1=0.2; dst=0.1 (a) inductors voltage (VL1, VL2), (b) inductors current ripple (Δ IL1, ΔIL2), (c) DC-link voltage (VPN), (d) capacitor voltage (VC1,VC2).

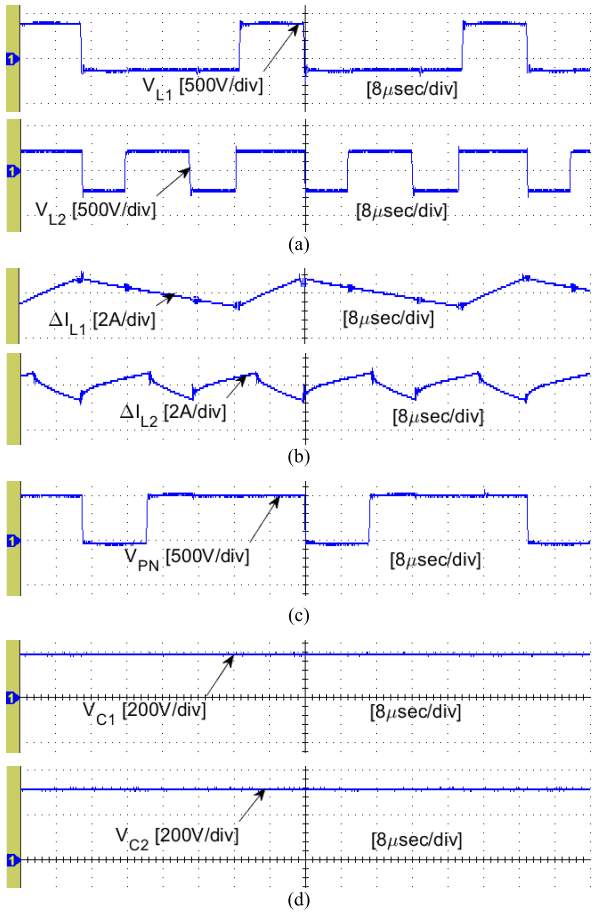

FIGURE 13. CC -AqZSI Experimental results with a resistive load of 1000 w when Vin=60; VPN=500; d1=0.4; dst=0.28 (a) inductors voltage (VL1, VL2), (b) inductors current ripple (ΔIL1, ΔIL2), (c) DC-link voltage (VPN), (d) capacitor voltage (VC1,VC2).

ripple is 1V and 1.8V for L_1 and L_2 respectively which almost agrees with (15).

The same procedure is carried out for the proposed DC-AqZSI, but with an input voltage of 90V, d1=0.6, dst=0.3, and $\hat{V}_{PN}= 500V$; the results are depicted in Fig. 10. (b). As anticipated, the voltages of C_1 and C_2 changed to 150V and 197V, respectively, which is almost agree with (11). The peak-to-peak current ripple of the inductor is 2.2V and 2.45V for L_1 and L_2 respectively, which, as anticipated, is greater than that of CC-AqZSI and roughly coincides with (16). The dc-link voltage is 498 V, which is nearly identical to CC-AqZSI voltages. Fig. 10(c) depicts the voltages and currents of the output phase. The RMS value of voltage is 110V, and there is no voltage or current distortion.

B. EXPERIMENTAL RESULTS

A 1-kVA prototype was constructed and utilized to validate the simulation and analytical results. Table 3 lists the value of prototype component parts. Fig. 11 is a photograph of the hardware configuration. It consists of an impedance network circuit, a DSP controller, a measuring unit, a driver board, an output filter, and a 1-kVA controllable. The inverter bridge performed by an FP40R12KT3 module, ensuring greater compatibility and a more compact circuit. Here, we performed all active components of the impedance network with the same module.

A DSP TMS320F28335 controller generates PWM control signals with a triangle frequency of 20 kHz. The drive circuits utilized the ISO5852 smart and high-performance gate driver IC from Texas Instruments, which has a very high common-mode immunity of 100 kV/us.

Fig. 12 shows the practical results for CC-AqZSI with Vin = 60V and $d_1 = 0.2$. The control system is set to maintain the dc-link voltage at 500V. Fig. 12(d) shows that the capacitor C_1 and C_2 voltages are 98V and 397V, respectively. They differ slightly from the theoretical results since the parasitic found in the experiment. Fig. 12(c) also demonstrates that the dc-link voltage is square and remains maximum unless the bridge's legs shorted. The peak voltage of the dc-link is 494 V, which is close to the set value of 500V. The experimental results prove that the inductor currents have two different charging and discharging patterns. It shows that, L_2 is charged twice per cycle, as opposed to the L_1, which is charged only in ST-mode. Furthermore, the intensity of its changes is greater than the L_1 inductor, consistent with the theoretical results.

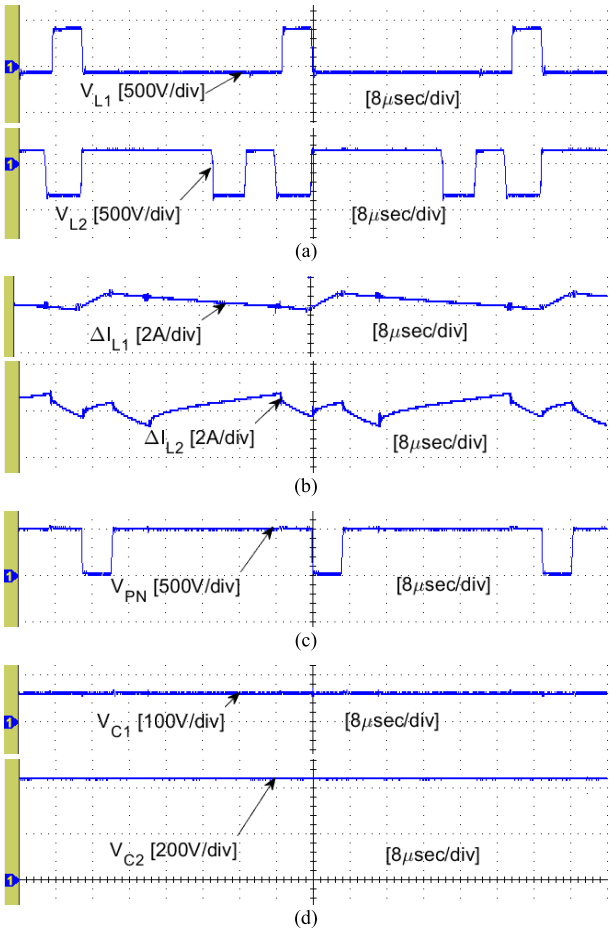

FIGURE 14. DC-AqZSI Experimental results with a resistive load of 1000 w when Vin=90; VPN=500; d1=0.3; dst=0.12 (a) inductors voltage (VL1, VL2), (b) inductors current ripple (ΔIL1, ΔIL2), (c) DC-link voltage (VPN), (d) capacitor voltage (VC1,VC2).

Fig. 13 depicts the practical results when the value of d_1 changed to 0.4 while the other conditions remain constant. Based on (11), dst increased to 0.28, and d_2 decreased to 0.32. As the ST-mode increases, the peak-to-peak inductor current ripple of L_1 and L_2 increases to 1A and 2.5A, respectively. Furthermore, the voltages of capacitors C_1 and C_2 have been changed to 197V and 295V, which are acceptable despite being slightly lower than the theoretical results. The same procedure followed for the proposed DC-AqZSI. Fig. 14 depicts the practical results for the DC-AqZSI with an input voltage of 90 V and d1 = 0.3. Fig. 14(d) shows that the capacitor voltage for this topology equals 58V and 345V, respectively. These values are lower than the calculated value for CC-AqZSI but agree with (16). Except for the voltage of the capacitors, other waveforms, particularly the dc-link voltage, follow the same rule described previously for CC-AqZSI and do not affected by topological changes. Using this method, it is simple to determine the voltage of the capacitors so that the voltage at the point of connection between two capacitors is equal to half the voltage of the dc-link; this point considered the middle point of the inverter. With this method, the impedance network used for three-level

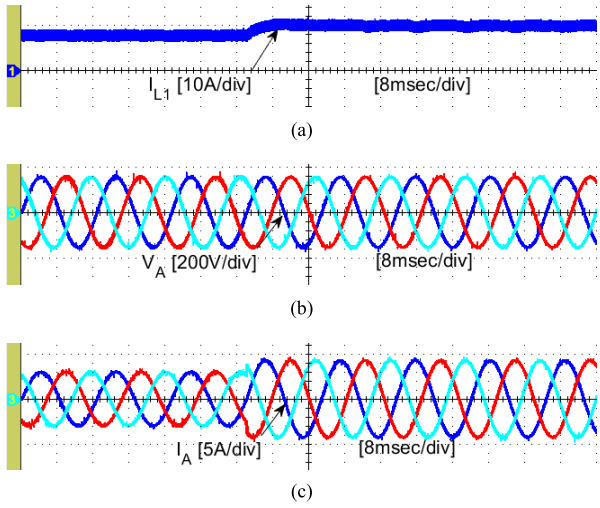

FIGURE 15. Experimental results of the dynamic response of the proposed when Vin=100 and load changes from 700 to 1000 w; (a) Inductor current (I_{L1}) (b) Output phase voltage (c) Output phase current.

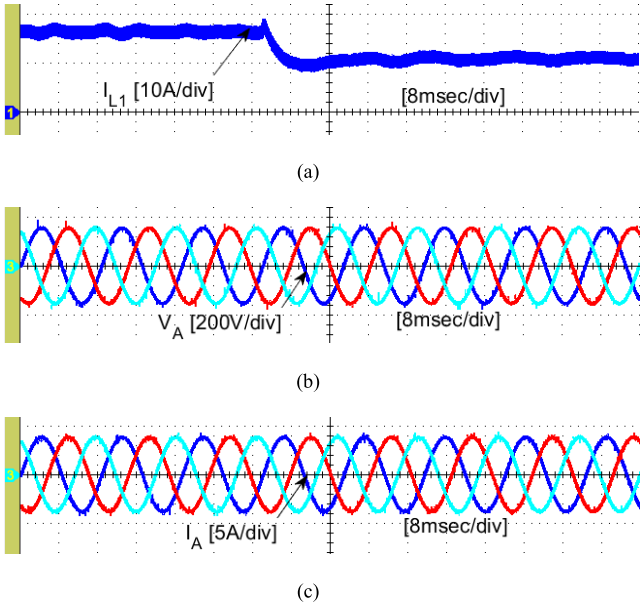

FIGURE 16. Experimental results of the dynamic response of the proposed when output power is 1000_W and input voltage changes from 60V to 90V; (a) Inductor current (IL1) (b) Output phase voltage (c) Output phase current.

inverters. In general, Fig. (12)–(14) show that the DC-AqZSI topology is only effective when the input voltage and d1 are both high. Under these conditions, the capacitor voltage is minimal and significantly different from CC-AqZSI. In other cases, the CC-AqZSI topology is preferred and recommended due to the continuity of the input current.

Fig. 15 depicts the experimental waveform of the output voltages during the transient state when the load power increases from 700 w to 1000 w while the input voltage set to 100 V. In accordance with the applied control policy, the input current increased in response to the increase in output current and power, and the load voltage stabilized at its previous levels. Fig. 16 depicts the dynamic response

of the system when the input voltage stepped from 60V to 90V and the load remains constant at 1000 w. As expected, thanks to the controller's proper operation, the input current is gradually decreasing, and the output voltage and current stabilized at their previous levels.

VIII. CONCLUSION

This paper presented two novel Active impedance source inverters based on the quasi Z-source inverter with a high voltage gain and a lower component count. Except for input current continuity and capacitor stress voltage, the gain of both topologies is identical. In addition to the control system's specifics, the analysis of the circuit and guidelines for parameter selection presented. In addition, comparisons between the proposed topologies and other similar topologies reveal that they have an additional degree of freedom, allowing for a wide range of gain and capacitor voltage adjustments. The introduced topology has favorable characteristics, and the current and voltage stresses of the internal components are superior or comparable to those of other topologies. The simulation and prototype results confirm the feasibility of the proposed topologies.

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