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RESEARCH ARTICLE

Novel Zero-Voltage Zero-Current Transition Buck Converter With Minimal Impact of Active Auxiliary Cell on Overall Dynamics

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ABSTRACT This paper presents a novel zero-voltage zero-current transition DC/DC buck converter, which uses an active auxiliary resonant network to achieve soft switching operation of semiconductor switches and soft-recovery of power diodes over wide output power range and offers high efficiency. The auxiliary cell in the proposed converter does not cause any additional current stress on the semiconductor switches and has minimal impact on overall dynamics of the converter. Steady-state performance of the converter has been presented with detailed theoretical analysis of all operating modes. The design of auxiliary cell components and development of small signal model of the converter have been carried out from the mathematical equations depicting its dynamic behaviour. A closed loop voltage mode controller with a type III compensator has been developed for the converter to achieve the desired transient response under the influence of external disturbances. Power loss analysis and superiority of the proposed converter over other conventional configurations are also presented here. Finally, soft-switching behaviour and step-input transient response of the converter are verified by hardware experimentation on a 150W, 100 kHz prototype model. The experimental measurements have successfully validated the theoretically predicted behaviour of the converter.

INDEX TERMS Buck converter, soft-switching, zero current switching (ZCS), zero voltage switching (ZVS).

I. INTRODUCTION

Extensive technological performance power converters enabling efficient integration of renewable energy sources to the DC/AC microgrids. Solar photovoltaic sources, wind generators, fuel cells and battery storages are popularly used in typical renewable energy systems as shown in Fig.1. Modern dc-dc power supplies are intended to be portable with large power to volume ratio, high efficient and able to provide tight regulation of the output voltage. The size and weight of magnetic and filter components of the power converters can be reduced by many folds with high switching frequency operation, but at the cost of excessive switching

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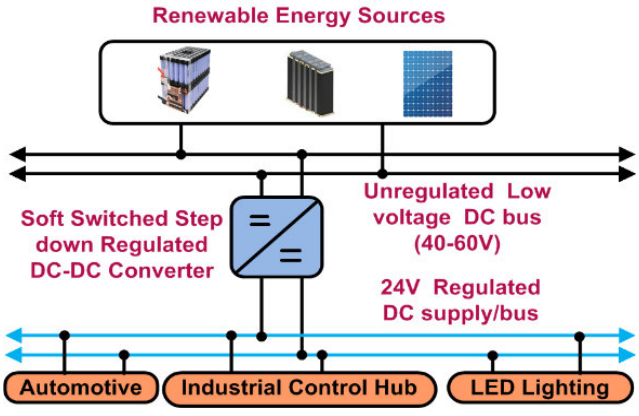

FIGURE 1. Structure of renewable energy system for regulated dc bus.

loss, increased current and voltage stress of semiconductor elements, large RFI &EMI, if operated with conventional hard switching. Extensive research works [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [22], [25] are therefore carried out to minimize above issues by adopting soft-switching transition of semiconductor switches. To meet the demand of modern applications, major research has been carried out in recent years to develop new topologies of soft-switched buck converters.

Auxiliary networks using active and/or passive components including coupled or tapped inductors [1], [2], [3], [4], [10] have been extensively used in the converters to meet one or more of the desirable features like, extended voltage gain [2], [3], [5], [6], wide duty-ratio operation [3], [9], [13]. The interleaved structure [5], [6] can provide high step down ratio as well as low ripple content at the load current. In [7] and [8] soft turn on is obtained by triggering the gate pulse when the body diode of the switch is in conduction making the voltage across the semiconductor switch zero. ZVS transition is achieved by utilizing the leakage energy of the coupled inductor with the aid of an auxiliary network consists of an inductor, a switch and a diode in [9]. Switched capacitor network [11] or voltage multiplier cells [12] or a combination of switched capacitor and coupled inductor [1], [2], [3], [4], [11], [12] have been used in many buck converters to extend the voltage gain. In [14], a switched inductor network is used for step down purpose. But, soft-switched transition of all switches has not been ensured in these converters. However, the converters [1], [2], [5], [10], [11] suffer from the drawback that the semiconductor switch used for the converter does not turn off with soft-switched phenomenon. Apart from ZVS turn-on of the switch, the converter [7], [8] also provides soft recovery of the power diode. But, turn-off of the switch lacks fully soft-switched condition. One of the mandatory requirements of the modern dc power supplies is to maintain the output load voltage at desired set point by automatically adjusting the duty cycle against any drift in supply voltage, load current or any external disturbance. Classical state space averaging techniques can be useful in developing the small signal model of the hard-switched power converter [15], [16], [17], operation of which in continuous conduction mode (CCM) is completed within two modes (active mode and passive mode) in a switching cycle. Conventional closed-loop controllers are designed based on the system transfer functions, obtained from the small-signal model of the converters. In [15] a contoured robust controller bode plot has been used to design the voltage- mode controller for a fifth order boost converter. This controller enjoys the advantages of more freedom in placing the poles and zeros and achieve better stability margin compared to conventional PI controller. Design of k–factor based type III controllers with optimum performance and faster transient response have been presented in [16], [18]. Method of Pole placement for controller design using all accessible state variables are used in [19]. PI controller along with sigma delta modulator has been implemented for the converter presented in [20] and [24]. Restrictions of dominant pole placement (DPP) method of controller is analysed in [21]. The control scheme adopted in [23] shapes the auxiliary inductor current for the improvement of dynamic response.

Soft-switching quasi-resonant converters (QRC) use active and/or passive resonant networks, in addition to basic components of normal pulse-width-modulation (PWM) converters. The resonant networks are activated at the switching instants to create the favorable conditions for soft-switching operation of the semiconductor elements. For the rest of the switching cycle the QRCs behave like normal PWM converters and operate at a fixed switching frequency.

Classical state space averaging technique cannot be readily used to develop the small signal model of QRC due to the presence of many resonant components apart from the large energy storing filter components. However, state-space modeling of these converters has not been adequately explored in any literature.

This paper proposes a novel zero-voltage zero-current transition DC/DC buck converter comprising of an auxiliary network of active and passive components to achieve soft-switched performance of the semiconductor devices. One of the novel aspects of proposed topology is the fully soft switched transition of semiconductor devices mitigating the switching and reverse recovery loss and thus maintaining high efficiency over a wide load range. The quasi-resonant soft–switched operation of the converter has also reduced di/dt and dv/dt of the semiconductor switches. The converter's EMI and RFI, which primarily depend on di/dt and dv/dt of the switching devices [26], have thus been reduced. The proposed buck converter maintaining high efficiency over wide load range can therefore be popularly used in typical renewable energy systems (Fig.1), integrating solar photovoltaic (SPV) sources, wind generators, fuel cells and battery storages, as an interface between a 40V-60V unregulated DC bus and a 24V DC bus, as well it can be used to extract maximum power from SPV sources under wide ambient conditions. Detailed operation of the proposed converter has been thoroughly described with topological equivalent circuits and typical time domain waveforms. The performance of the proposed converter with varying load conditions have been evaluated and presented in the subsequent sections. Finally, the soft-switched performance and the step-input transient response of the converter is validated through real time testing of a laboratory scale hardware prototype of proposed topology along with a type III closed loop compensator.

II. OPERATION AND ANALYSIS OF PROPOSED CONVERTER

The circuit configuration of proposed converter is depicted in Fig.2. In addition to the primary components of classical buck converter: semiconductor switch (S_1), diode (D_1), inductor (L_1) and output capacitor (C_O), the proposed converter uses an auxiliary network comprising a semiconductor switch (S_2), a capacitor (C_2), inductor (L_2 and L_3), and two diodes (D_2 and D_3). The diodes (D_m and D_a) are integral body diodes

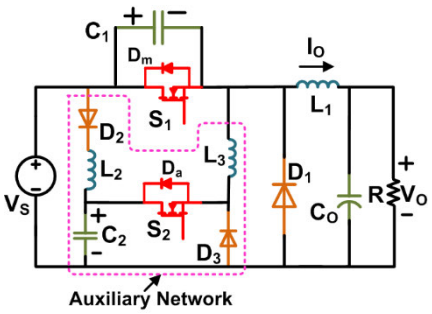

FIGURE 2. Circuit diagram of proposed soft switched buck converter.

of the semiconductor switch (S_1 and S_2) respectively. C_1 is the main switch snubber capacitor, which includes its body capacitance.

The proposed soft-switched buck converter is designed to operate at high switching frequency to reduce the size and weight of inductor and capacitors by manifolds and simultaneously maintain high efficiency. The increment in converter size due to the addition of the auxiliary network is quite insignificant in comparison to the reduction in size and weight, obtained through high frequency operation.

The steady state working methodology of the converter is detailed considering the assumptions mentioned below.

I. The buck inductor (L_1) is large enough to maintain constant load current (I_O) during one switching cycle.

II. All the semiconductor switches and diodes are ideal.

III. Continuous conduction mode (CCM) is being considered for converter operation.

Initially, assuming that the proposed converter is operating in passive mode, in which the buck inductor (L_1) linearly transfers its stored energy to the output through the diode D_1. All other diodes and active switches are now in OFF condition. The resonant inductors (L_2 and L_3) are in de-energised state. The initial voltages of snubber capacitor (C_1) and the resonant capacitor (C_2) at (t_0) are supply voltage ($V_{C1} = V_S$) and a voltage level above $2V_S$ (say, V') respectively. Fig.3 describes converter equivalent circuits in ten operating modes and the theoretical time-domain current and voltage waveforms of the converter is shown in Fig.4.

MODE 1 ($t_0 - t_1$)***:*** Stage 1 begins at $t = t_0$ as the auxiliary switch (S_2) is turned on, the resonant capacitor C_2 starts discharging through S_2 and the load in resonance with inductor (L_3). As, the current (i_{L3}) through inductor (L_3) rises resonantly from zero, the switch (S_2) realizes zero current turn-on (ZCS) and the current through buck diode (D_1) decreases in the same fashion, to maintain the constant buck inductor current (I_O). The equations governing mode 1 are given by,

$$i_{S2}(t) = i_{L3}(t) = \frac{V'}{\sqrt{L_3/C_2}} \sin \omega_1 (t - t_0) \quad (1)$$

$$i_{D4}(t) = I_O - i_{L3}(t) \quad (2)$$

$$v_{C2}(t) = V' \cos \omega_1 (t - t_0) \quad (3)$$

$$\text{where, } \omega_1 = 1/\sqrt{L_3 \cdot C_2} \quad (4)$$

This switching mode ends at time $t = t_1$ when current flowing through the inductor L_3 reaches to the buck inductor (L_1) current (I_O) and the diode (D_1) recovers softly.

Duration of this switching interval is given by,

$$t_{01} = t_1 - t_0 = \frac{1}{\omega_1} \sin^{-1}\left(\frac{I_O}{V'}\sqrt{\frac{L_3}{C_2}}\right) \quad (5)$$

At the end of this state, the voltage (v_{C2}) across the terminals of resonant capacitor (C_2) is given by,

$$v_{C2}(t_1) = V' \cos \omega_1 t_{01} \quad (6)$$

MODE 2 ($t_1 - t_2$)***:*** As the discharge current of capacitor (C_2) rises above I_O, the excess current ($i_{L3} - I_O$) of the inductor (L_3) resonantly discharges the snubber capacitor (C_1) from its initial voltage (V_S). The following voltage and current equations governing this mode are derived as below.

$$v_{C2}(t) = \frac{1}{C_1 + C_2}[v_{C2}(t_1).\{C_2 + C_1 \cos \omega_2 (t - t_1)\} - I_O \cdot (t - t_1) - \frac{C_1}{C_2} I_O \sqrt{L_3 C} \sin \omega_2 (t - t_1)] \quad (7)$$

$$v_{C1}(t) = V_S - v_{C2}(t_1)\frac{C}{C_1}\{1 - \cos \omega_2 (t - t_1)\} + I_O \frac{C}{C_1 \cdot C_2}\{(t - t_1) - \sqrt{L_3 C} \sin \omega_2 (t - t_1)\} \quad (8)$$

$$i_{L3}(t) = \frac{I_O}{C_1 + C_2}\{C_2 + C_1 \cos \omega_2 (t - t_1)\} + \frac{v_{C2}(t_1)}{\sqrt{L_3/C}} \sin \omega_2 (t - t_1) \quad (9)$$

$$\text{where, } C = \frac{C_1 C_2}{C_1 + C_2} \quad (10)$$

$$\text{and } \omega_2 = 1/\sqrt{L_3 C} \quad (11)$$

Complete discharge of snubber capacitor (C_1) marks the end of mode 2. The current of inductor (L_3) is now reached to its peak. Duration of this switching interval (t_{12}) can be computed from equation (8) through numerical analysis. At t_2, the capacitor voltage (v_{C2}) and the inductor current (i_{L3}) are given by,

$$v_{C2}(t_2) = \frac{1}{C_1 + C_2}\{v_{C2}(t_1).(C_2 + C_1 \cos \omega_2 t_{12}) - I_O t_{12} - \frac{C_1}{C_2} I_O \sqrt{L_3 C} \sin \omega_2 t_{12}\} \quad (12)$$

$$i_{L3}(t_2) = \frac{I_O}{C_1 + C_2}(C_2 + C_1 \cos \omega_2 t_{12}) + \frac{v_{C2}(t_1)}{\sqrt{L_3/C}} \sin \omega_2 t_{12} \quad (13)$$

MODE 3 ($t_2 - t_3$)***:*** As the capacitor (C_1) is completely discharged, the excess current ($i_{L3} - I_O$) of inductor (L_3) is now maintained through the body diode (D_m), impressing zero voltage across the main power switch (S_1). The main power switch (S_1) can now be turned on under zero-voltage zero-current switching (ZV-ZCS) condition with the application of its switching gate pulse (G_{S1}). During this mode, the capacitor (C_2) discharges resonantly through L_3.

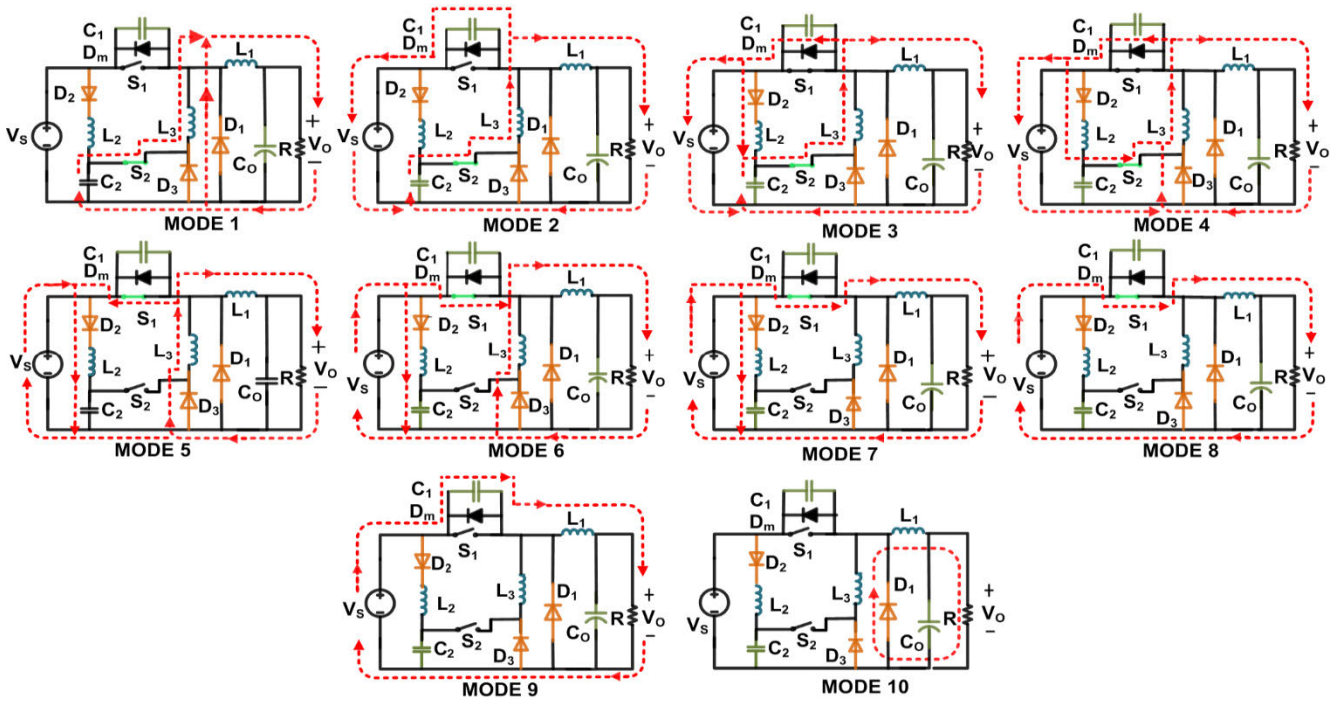

FIGURE 3. Soft switched buck converter equivalent circuits in different switching modes.

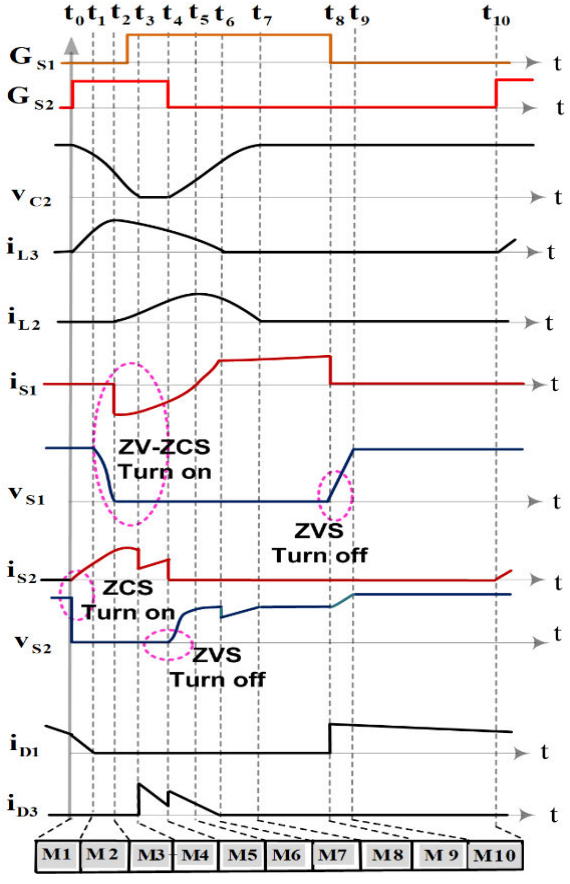

FIGURE 4. Steady state theoretical waveforms in different modes.

For simplification of analysis, it is assumed that during mode 3, the capacitor (C_2) starts simultaneously getting charged from the supply voltage (V_S) in resonance with the inductor (L_2). Thus, the diode (D_2) starts conduction with zero current. The valid equations related with mode 3 are given by,

$$i_{L3}(t) = \frac{v_{C2}(t_2) - V_O}{\omega_3 L_3} \sin\omega_3(t - t_2) + i_{L3}(t_2)\cos\omega_3(t - t_2) + \frac{L_3}{L_2 + L_3} \cdot i_{L3}(t_2)\{1 - \cos\omega_3(t - t_2)\} \quad (14)$$

$$i_{L2}(t) = \frac{L_3}{L_2 + L_3} \cdot i_{L3}(t_2)\{1 - \cos\omega_3(t - t_2)\} - \frac{v_{C2}(t_2) - V_O}{\omega_3 L_2} \sin\omega_3(t - t_2) \quad (15)$$

$$v_{C2}(t) = V_S + \{v_{C2}(t_2) - V_O\}\cos\omega_3(t - t_2) - \frac{i_{L3}(t_2)}{\omega_3 C_2} \sin\omega_3(t - t_2) \quad (16)$$

$$where,\ \omega_3 = \sqrt{\frac{L_2 + L_3}{L_2 L_3 C_2}} \quad (17)$$

This mode concludes at t_3, when capacitor (C_2) is discharged completely. Time duration (t_{23}) of this mode can be computed from equation (16) through numerical analysis. The respective current expressions, through the inductors (L_3 *and* L_2) at the end of mode 3 are given by,

$$i_{L3}(t_3) = \frac{v_{C2}(t_2) - V_O}{\omega_3 L_3} \sin\omega_3 t_{23}$$

$$+\frac{i_{L3}(t_2)}{L_2+L_3}\{L_3+L_2\cos\omega_3 t_{23}\} \quad (18)$$

$$i_{L2}(t_3)=\frac{L_3}{L_2+L_3}\cdot i_{L3}(t_2)\{1-\cos\omega_3 t_{23}\} - \frac{v_{C2}(t_2)-V_O}{\omega_3 L_2}\sin\omega_3 t_{23} \quad (19)$$

MODE 4 ***($t_3 - t_4$):*** At t_4, the beginning of mode 4, the current (i_{L3}) of inductor (L_3) tends to charge capacitor (C_2) in opposite direction, the diode (D_3) gets forward biased and provides a conducting path for the current of L_3. Now, the input supply (V_S) is impressed across both the inductors (L_2) and (L_3) through the diode (D_3). Thus, the current of inductor (L_2) now starts rising linearly from $i_{L2}(t_3)$ and the current of inductor (L_3) linearly reduces from $i_{L3}(t_3)$. The difference of i_{L3} and i_{L2} is maintained through the diode (D_3). The important current equations are as below

$$i_{L2}(t) = i_{L2}(t_3)+\frac{V_S}{L_2}(t-t_3) \quad (20)$$

$$i_{L3}(t) = i_{L3}(t_3)-\frac{V_S}{L_3}(t-t_3) \quad (21)$$

$$i_{D3}(t) = i_{L3}(t_3)-i_{L2}(t) \quad (22)$$

This interval ends, when auxiliary switch (S_2) is turned off at t_4. At the end of this mode,

$$i_{L2}(t_4) = i_{L2}(t_3)+\frac{V_S}{L_2}t_{34} \quad (23)$$

$$i_{L3}(t_4) = i_{L3}(t_3)-\frac{V_S}{L_3}t_{34} \quad (24)$$

MODE 5 ***($t_4 - t_5$):*** As switch (S_2) is turned off, the capacitor (C_2) again resonantly charges from the input supply (V_S) and the stored energy of inductor (L_2) through the diode (D_2). The current (i_{L3}) of inductor (L_3) is now retained through the diode (D_3). As, D_3 is in conduction, the impressed capacitor voltage (v_{C2}) across S_2 ensures its ZVS turn-off. The significant equations for this mode are as follows,

$$i_{L2}(t) = i_{L2}(t_4)\cos\omega_3(t-t_4)+\frac{V_S}{\sqrt{L_2/C_2}}\sin\omega_3(t-t_4) \quad (25)$$

$$v_{C2}(t) = V_S\{1-\cos\omega_3(t-t_4)\} + i_{L2}(t_4)\sqrt{L_2/C_2}\sin\omega_3(t-t_4) \quad (26)$$

Now, the current (i_{L3}) flowing through inductor (L_3) continues to decrease linearly as before. This mode gets over, as the inductor current (i_{L3}) is reduced to I_O and the diode (D_m) exhibits soft commutation. Duration of this mode is given by

$$t_{45} = t_5 - t_4 = \{i_{L3}(t_4)-I_O\}.(L_3/V_S) \quad (27)$$

The current (i_{L2}) and the voltage across the capacitor (C_2) after mode 5 are given by,

$$i_{L2}(t_5) = i_{L2}(t_4)\cos\omega_3 t_{45}+\frac{V_S}{\sqrt{L_2/C_2}}\sin\omega_3 t_{45} \quad (28)$$

$$v_{C2}(t_5) = V_S(1-\cos\omega_3 t_{45})+i_{L2}(t_4)\sqrt{\frac{L_2}{C_2}}\sin\omega_3 t_{45} \quad (29)$$

Mode 6 ***($t_5 - t_6$):*** During this mode, the current (i_{L3}) through the inductor (L_3) continues to reduce linearly and the current of the inductor (L_2) changes resonantly as before. As the current of L_3 goes below I_O, the balance load current ($I_O - i_{L3}$) is now supplied by the input supply (V_S) through the main switch (S_1). Thus (S_1), the main switch, starts conduction under ZV-ZCS condition and its current increases linearly from zero. The current (i_{L3}) flowing through inductor (L_3) and the main switch current (i_{S1}) are given by,

$$i_{L3}(t) = i_{D3}(t) = I_O-\frac{V_S}{L_3}(t-t_5) \quad (30)$$

$$i_{S1}(t) = \frac{V_S}{L_3}(t-t_5) \quad (31)$$

As the inductor current (i_{L3}) is linearly diminished to zero, the diode (D_3) exhibits soft commutation. The main switch current (i_{S1}) is now increased to I_O and operation of this mode is concluded. Time interval of this state is calculated as,

$$t_{56} = t_6 - t_5 = \frac{L_3 I_O}{V_S} \quad (32)$$

MODE 7 ***($t_6 - t_7$):*** In this interval, the buck inductor (L_1) gets energized from the input supply (V_S) , as the load current (I_O) is maintained through S_1. However, the current (i_{L2}) of inductor (L_2) and the voltage (v_{C2}) across capacitor (C_2) continue to change resonantly as before. This switching state gets over, when the current of inductor (L_2) is resonantly diminished to zero and the soft commutation of diode (D_2) is ensured. At time ($t = t_7$), the capacitor (C_2) is charged to its peak value (V') given by,

$$V' = v_{C2}(t_7) = V_S - \{V_S - v_{C2}(t_6)\}\cos\omega_3 t_{67} + i_{L2}(t_6)\cdot\sqrt{L_2/C_2}\sin\omega_3 t_{67} \quad (33)$$

Time stretch of this mode is derives as,

$$t_{67} = t_7 - t_6 = \frac{1}{\omega_3} \cdot\cos^{-1}\frac{V_S - V'}{\sqrt{\{V_S - v_{C2}(t_6)\}^2+\{i_{L2}(t_6)\sqrt{L_2/C_2}\}^2}} + \frac{1}{\omega_3}\cdot\tan^{-1}\frac{i_{L2}(t_6)\sqrt{L_2/C_2}}{v_{C2}(t_6)-V_S} \quad (34)$$

MODE 8 ***($t_7 - t_8$):*** During this mode, the buck inductor (L_1) gets energised and load current (I_O) is maintained from the input supply (V_S) as before. Rest of the semiconductor devices are now in the blocking state. This mode terminates, when the main power switch (S_1) is turned off at t_8. Switching duty ratio (d) of the proposed converter is controlled by varying the time duration (t_{78}).

MODE 9 ***($t_8 - t_9$):*** After t_8, the main switch (S_1) is switched off, the capacitor (C_1) starts acquiring charge almost linearly by the stored energy of the buck inductor (L_1) and the input supply (V_S). The voltage of capacitor (C_1) is determined by,

$$v_{C1}(t) = \frac{I_O}{C_1}(t-t_8) \quad (35)$$

Mode 9 terminates, when the snubber capacitor voltage (v_{C1}) reaches to the supply voltage (V_S) and the diode (D_1) comes into conduction. This mode continues for the following duration,

$$t_{89} = t_9 - t_8 = (V_S \cdot C_1)/I_O \tag{36}$$

MODE 10 ***($t_9 - t_{10}$):*** In this mode, the load current (I_O) is maintained through diode (D_1) by the stored energy of inductor (L_1). All other diodes and semiconductor switches are now in blocking state. Passive mode operation of the converter is completed at t_{10}, as S_2 is turned on and the operating cycle is repeated.

III. SELECTION OF AUXILIARY CELL COMPONENTS

At interval 2 and 3, the resonant energy transfer to the load is very less and the major part is fed back to the source.

Considering P_c, V_O, I_O as the load power, load voltage and load current respectively for a conventional buck converter, while P_s, V'_O and I'_O as load power, load voltage and load current of the proposed converter, the relation between them becomes

$$\left.\begin{aligned} P_S &= P_c + \frac{1}{2}L_3(I'_O)^2 \cdot f \\ \frac{(V'_O)^2}{R} &= \frac{(V_O)^2}{R} + \frac{1}{2}L_3\left(\frac{V'_O}{R}\right)^2 \cdot f \end{aligned}\right\} \tag{37}$$

Taking $V'_O = V_O + \Delta V$(additional voltage at the output), $I'_O = I_O + \Delta I$ (additional current at load) and replacing the value of V'_O in equation (37), the following relation can be derived

$$L_3 = (2R/f)(1 - P_C/P_S) \tag{38}$$

As P_S tends to be equal to P_C, L_3 approaches to a small value. So, for small value of L_3 or without the auxiliary circuit the behaviour of the proposed converter is like a conventional hard switched buck converter. From above theoretical analysis, ΔV and ΔI are considered as negligible for the design of auxiliary parameters.

Main switch (S_1) always turns off under zero voltage switching (ZVS) condition because of the parallel connected snubber capacitor C_1. The capacitor C_1 must be discharged completely within the time (t_{12}) and before the withdrawal of the auxiliary switch gate pulse. In order to get ZV-ZCS turn-on of main switch, the gate pulse (G_{S1}) needs to be applied during conduction state of body diode (D_m). The value of snubber capacitor can be calculated from equation below:

$$C_1 \leq \frac{i_{L3}(t_2) - I_O}{V_S}(t_2 - t_1) \tag{39}$$

It can be concluded from (1), the turn-on of the main switch can take place under ZV-ZCS condition, if the peak current of inductor L_3 is more than the load current (Io) as expressed below.

$$\frac{V'}{\sqrt{L_3/C_2}} \geq I_O(\max) \tag{40}$$

Thus, the marginal value of i_{L3} (peak) is equal to I_O at which no current would flow through the snubber capacitor C_1 and body diode (D_m). The excess current (i_e) equal to ($i_{L3} - I_O$) will flow through D_m and provide ZVZCS situation for the main switch at turn-on. At light load the current (i_e) will be more and less at heavy load. So a minimum value of excess current should be taken into consideration and has to be added with maximum load current to get the peak current (i_{L3}) of resonant inductor L_3. The peak value of current flowing through resonant inductor L_3 is

$$i_{L3}(peak) = I_O(\max) + I_e = \frac{V'}{\sqrt{L_3/C_2}} \tag{41}$$

For design of resonant capacitor (C_2), from equation (39) & (41), the relation to be fulfilled for soft switching is depicted in (42).

$$Z_C < \frac{V'}{I_O(\max) + I_e} \tag{42}$$

where, $Z_C = \sqrt{L_3/C_2}$.

In this design, to achieve soft switch with variable loads of 48W to 144W the minimum freewheeling current has been chosen as 20% of the load current which discharges C_2 at maximum 1/25th of switching period. From equation (40), $C_1 = 4.7nF$ is taken as practical value. Relationship among (Z_C), load current (I_O), and freewheeling current (I_e) is shown in Fig.5. It can be seen from Fig.5 the safe value of Z_C is less than 15 and above 60 converter will be in hard switching state . Finally the optimized value is chosen from Fig.5 to fulfill the constraint equation (42) for soft switching. By using eqn. (38) the value of L_3 should be determined first and then the value of capacitor C_2 can be chosen from a range of practical capacitor for getting a particular value of Z_C.

The flowchart for optimizing the auxiliary cell parameters is given in Fig.6.

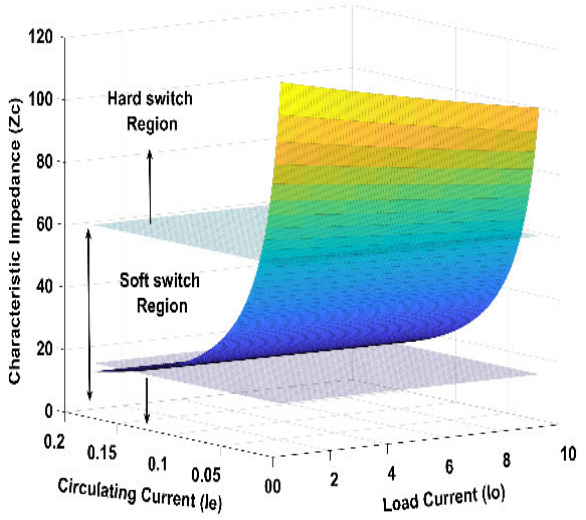

FIGURE 5. Variation of freewheeling current (i_e) under different loading conditions within the ZCS limit as parameters of load current (I_O) and ratio Z_C.

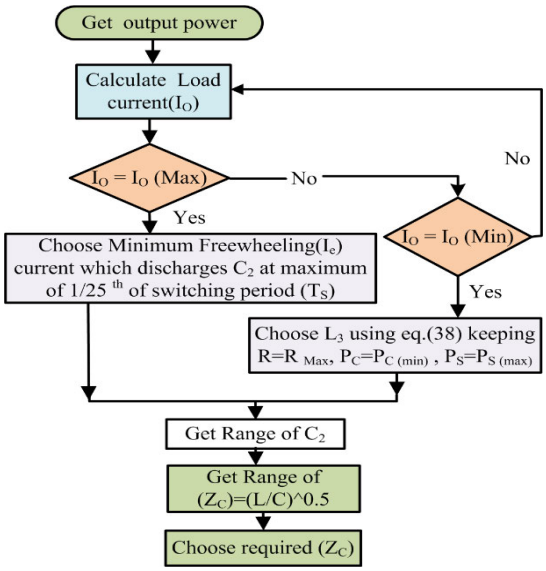

FIGURE 6. Flowchart for optimizing components of auxiliary cell.

TABLE 1. Specification and components of proposed buck converter.

Parameters	Specifications/ Component values
Input voltage(V_S)	40-60V
Output voltage(V_O)	24V
Output power(P_O)	144Watt
Switching frequency(f_{sw})	100kHz
Main switch(S_1)	IRFB3077PbF
Auxiliary switch (S_2)	IRFP4668PbF
Buck Diode(D_1)	SBR10U100CT
Auxiliary Diodes(D_2)	SBR10U150CT
Auxiliary Diodes(D_2	SBR20U200CT
Buck inductor(L_1)	170µH
Resonant inductors (L_2&L_3)	4.45µH,3.88µH
Snubber capacitor($C_{1)}$	4.72nF
Resonant capacitor(C_2)	22nF
Filter capacitor(C_O)	100µF

From mode 3, the rate of charging of resonant capacitor (C_2) should be $<$ rate of discharging. So the value of $L_2 > L_3$ has been chosen. Minimum delay time ($t_{01} + t_{12}$) of main switch from auxiliary switch can be calculated from (5) and (8). The values of L_3, L_2 and C_2 are given in Table 1.

$$\mathrm{d_i} = \frac{\text{duration of i}^{\text{th}}\text{mode}}{\text{switching time period}} \tag{43}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \\ \frac{dv_{CO}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+r_C)r_L + Rr_C}{L_1(R+r_C)} & 0 & 0 & \frac{d_2-d_9}{L_1} & 0 & -\frac{R}{L_1(R+r_C)} \\ 0 & 0 & 0 & 0 & -\frac{(d_3+d_5+d_6+d_7)}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{d_2}{L_3} & \frac{d_1+d_2+d_3}{L_3} & 0 \\ -\frac{d_2-d_9}{C_1} & 0 & \frac{d_2}{C_1} & 0 & 0 & 0 \\ 0 & \frac{(d_5+d_6+d_7)}{C_2} & \frac{(d_1+d_2+d_3+d_6)}{C_2} & 0 & 0 & 0 \\ \frac{R}{(R+r_C)C_O} & 0 & 0 & 0 & 0 & -\frac{1}{(R+r_C)C_O} \end{bmatrix} \times \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ v_{C1} \\ v_{C2} \\ v_{CO} \end{bmatrix} + \begin{bmatrix} \frac{(d_2+d_3+d_4+d_5+d_6+d_7+d_8+d_9)}{L_1} \\ \frac{d_3+d_4+d_5+d_6+d_7}{L_2} \\ -\frac{d_2+d_3-d_4-d_5}{L_3} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_S] \tag{44}$$

IV. SMALL SIGNAL MODELLING AND DESIGN OF CONTROLLER

The major components used in the proposed converter have been selected following the dynamic equations describing the behavior of the converter. The specification and the major components of the converter are detailed in Table 1. In order to regulate the output load voltage, the proposed converter has been provided with a closed loop voltage mode controller. This section analyses the steady-state and dynamic behavior of the uncompensated converter and accordingly selects a suitable compensator to achieve the desired transient response. First, state space matrix of the converter has been derived by state space averaging of the dynamic equations, describing the behavior of the converter in each mode as detailed in section II. There are six energy storing elements (L_1, L_2, L_3, C_1, C_2) and (C_O) in the power circuit of the converter. If all inductor current i_{L1}, i_{L2}, i_{L3} and capacitor voltages (V_{C1}, V_{C2}, V_{CO}) are considered as state variables, then a state space matrix of dimension 6×6 is formed. In the state space matrix, the equivalent series resistors (ESRs) of large energy storing elements buck inductor (L_1) and output capacitor, (C_O) have been represented by the parameters r_L and r_c respectively. However, comparatively small ESRs of the passive resonant components L_2, L_3, C_1 and C_2 have been neglected in the analysis. The load (R) has been considered to be purely resistive. In a complete switching cycle, the converter operation is completed in ten operating modes in the formation of average state space matrix, the duration of each mode has been represented by a factor (fractional duty ratio d_i) defined as below. Fractional duty ratio at i^{th} mode, equation (43), as shown at the bottom of the previous page.

The averaged state space matrix, thus derived for the proposed converter is expressed as equation (44), shown at the bottom of the previous page, and the output matrix is expressed in equation (45)

$$V_O = \begin{bmatrix} \frac{R \cdot r_C}{R + r_C} & \frac{R}{R + r_C} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{CO} \end{bmatrix} + [0]\, V_S \tag{45}$$

From the key waveforms of Fig. 4, the switching duty ratio (d) of the main switch (S_1) can be approximately expressed as below.

$$d = d_3/2 + d_4 + d_5 + d_6 + d_7 + d_8 \tag{46}$$

Again, the duration of each mode has been approximated from the operational analysis, described in section II and then the fractional duty ratio (d_i) of the each mode has been represented in terms of the duty ratio (d) as represented below:

$$\begin{cases} d_1 = 0.03349d; \quad d_2 = 0.048d; \; d_3 = 0.03324d; \\ d_4 = 0.0814d; \quad d_5 = 0.06466d; \; d_6 = 0.0473d; \\ d_7 = 0.135d; \quad d_8 = 0.664d; \; d_9 = 1.04 \times 10^{-4} d; \\ d_{10} = 1.402d \end{cases} \tag{47}$$

It is observed from equations (47) that, the fractional duty ratio of the modes 1, 2, 3 and 9 are very small, aggregating only 6.11% of the switching time period. Hence, for simplification of steady state analysis and controller design, the modes (1, 2, 3 and 9) have been neglected in the simplified state space matrix, without causing much loss of accuracy. The state space matrix is further simplified by neglecting the state variable (V_{C1}), as charging and discharging cycle

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dv_{C2}}{dt} \\ \frac{dv_{CO}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R + r_C)r_L + Rr_C}{L_1(R + r_C)} & 0 & 0 & 0 & -\frac{R}{L_1(R + r_C)} \\ 0 & 0 & 0 & -\frac{0.23796}{L_2} d & 0 \\ 0 & 0 & 0 & \frac{0}{L_3} & 0 \\ 0 & \frac{0.23796d}{C_2} & \frac{0}{C_2} & 0 & 0 \\ \frac{R}{(R + r_C)C_O} & 0 & 0 & 0 & -\frac{1}{(R + r_C)C_O} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ v_{C2} \\ v_{CO} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{0.31936}{L_2} d \\ -\frac{0.14606}{L_3} \\ 0 \\ 0 \end{bmatrix} [v_S] \tag{48}$$

of the snubber capacitor (C_1) gets completed within mode 2 and mode 9, total duration of which occupies very small fraction of the switching time period. Considering all these aspects, the state space matrix gets simplified as presented in equation (48), shown at the bottom of the previous page.

The small signal mathematical model of the proposed converter has been developed by introducing small a.c. perturbations to the input variables and the control signal (duty ratio) around the steady state operating point as below.

$$\left.\begin{aligned} &i_{L1} = I_{L1} + \hat{i}_{L1}, i_{L2} = I_{L2} + \hat{i}_{L2}, i_{L3} = I_{L3} + \hat{i}_{L3} \\ &v_{C2} = V_{C2} + \hat{v}_{C2}, v_{CO} = V_{CO} + \hat{v}_{CO}, v_S = V_S + \hat{v}_S \\ &d = D + \hat{d}, v_O = V_O + \hat{v}_O \end{aligned}\right\} \tag{49}$$

Substituting equation (49) in equations (45) and (48) and subsequently separating the dc and ac quantities after neglecting the second order terms, the small signal model has been developed and expressed in equations (50) and (51), as shown at the bottom of the next page. Equation (50) has been presented at the top of this page. In equations (50) and (51) the matrixes A, B, and C represent the state matrix, the input matrix and the output matrix respectively.

In order to get the numerical expression of the control-to- output transfer function ($\hat{v}_O/\hat{d}$) the considered nominal case experimental parameters and component values are listed in Table 1. By substituting the parameters and component values in (50), the control-to-output transfer function ($\hat{v}_O/\hat{d}_O$) has been obtained as equation (52), as shown at the bottom of the next page. To verify the validity of the obtained model, a frequency response plot of the actual model of the proposed converter has also been obtained by using MATLAB system identification tool box using the same operating conditions. The obtained plot is superimposed on the approximated bode plot of Fig.7. Close agreement of both the frequency response plots clearly justifies the validity of the model. From the pole zero map in Fig.8, the location of the poles and zeros are observed. One pole (P_1) at origin [(0+j0) rad/s], two complex conjugate pole pair (P_2, P_3) and (P_4, P_5) at [(−0.0±j304210) rad/s]&[(−980±j7600) rad/s] respectively. Among the four zeros, one zero (Z_1) located at the origin [(0+j0) rad/s], one pair of complex conjugate zero (Z_2, Z_3) is at [(−0±j304210) rad/s] and the other zero Z_4 is located at (−333330 rad/s). It is observed that, no pole exists on the right half plane (RHP). From the location of pole zero pairs (P_1, Z_1)(P_2, Z_2)&(P_3, Z_3), it is evident that their effect cancels each other and as a result system order is reduced. Again, the small signal model linearized around nominal and other extreme operating conditions is found to resemble a second order system after the observation of pole zero plot and frequency response. The reduced order derived model as in equation (53), as shown at the bottom of the next page, mathematical model and MATLAB identified model frequency response are given in Fig.7 and the models are found to be matching with each other. This exercise is carried out in order to develop a simplified model from the higher order system. The undesirable transient response of

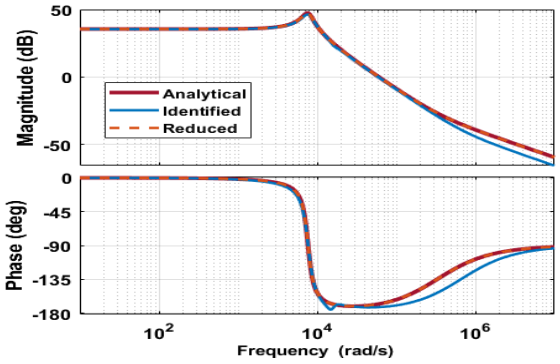

FIGURE 7. Bode plot comparison of proposed converter.

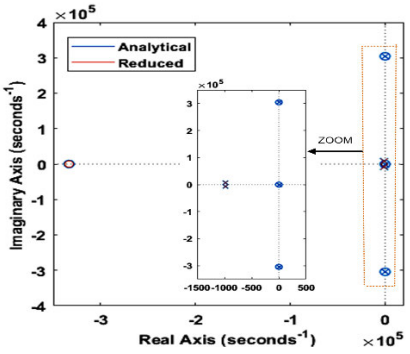

FIGURE 8. Pole zero map of the open loop system.

the system can also be estimated from the Bode plot of Fig. 7. A phase margin (PM) of only 12.1° and gain crossover frequency (bandwidth) of 9.58 kHz clearly indicates large PO, SSE and ST of the uncompensated buck converter.

V. SELECTION AND DESIGN OF CONTROLLER STRUCTURE AND PARAMETER

Now an appropriate controller is required to be designed in order to maintain the output voltage fixed under variable operating conditions. The schematic block diagram of the overall system with closed loop control circuit is shown in Fig. 9. The desired set point is the rated output voltage which needs to be tracked satisfying some performance criterion specified in frequency or time domain. A type 3 is a simple, reliable output feedback single loop voltage mode controller having greater degrees of freedom which achieves design criterion. The controller design is based on pole zero cancellation technique along with robustness considerations. The robustness aspects ensure predefined phase margin (PM) and achievable bandwidth (gain crossover point, ω_c) for the worst case plant model. The oscillatory response of the plant model is compensated by placing desired pole of the compensator and cancelling the effect of plant poles with the two zeros of the compensator. The higher degrees of freedom in the compensator whose TF is given in the equation (54), allows the compensator pole at ω_{CP2} to be placed accordingly at

$\omega_{CP2} = \omega_P$ as given in equation (55),

$$G_C(s) = \frac{k_c(1 + k_1 s + k_2 s^2)}{s(1 + s/\omega_{cp1})(1 + s/\omega_{cp2})} \tag{54}$$

$$\omega_{cp2} = \omega_p = \omega_c / \tan(90^\circ - PM) \tag{55}$$

ω_{CP1} is supposed to cancel the effect of the high frequency plant zero arising due to the ESR present in the output capacitor in the soft switched buck converter. Therefore ω_{cp1} is strategically placed at 333, 330 rad/s. In equation (55), the choice of gain crossover point has been based on general thumb rule which is around 1/10$^{\text{th}}$ of the switching frequency such that model validity is not a cause of concern. The complex conjugate zeros of the compensator are designed to offer feasible cancellation of plant poles to enhance the speed of the response with reduced overshoot and undershoot. After observation of plant's pole zero map, k_1 and k_2 has been fixed at 3.32×10^{-5} and 1.7027×10^{-8} respectively and replaced in equation (54). The only unknown left in compensator $G_C(s)$ is gain k_c which is designed upon considering the unity loop gain crossover frequency ω_c. Taking $F_m = 1/V_m$ as the PWM modulator gain, where V_m is the peak of the saw tooth wave generated before the comparator, the comparator gain k_c has

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \\ \frac{d\hat{v}_{CO}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{(R+r_C)r_L + Rr_C}{L_1(R+r_C)} & 0 & 0 & 0 & -\frac{R}{L_1(R+r_C)} \\ 0 & 0 & 0 & -\frac{0.23796}{L_2}D & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{0.23796}{C_2}D & 0 & 0 & 0 \\ \frac{R}{(R+r_C)C_O} & 0 & 0 & 0 & -\frac{1}{(R+r_C)C_O} \end{bmatrix}}_{A} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{v}_{C2} \\ \hat{v}_{CO} \end{bmatrix}$$

$$+ \underbrace{\begin{bmatrix} \frac{1}{L_1}D & \frac{V_S}{L_1} \\ \frac{0.31936}{L_2}D & \frac{0.31936\,V_S - 0.23796\,V_{C2}}{L_2} \\ -\frac{0.14606}{L_3}D & -\frac{0.14606 V_S}{L_3} \\ 0 & \frac{0.23796\,I_{L2}}{C_2}D \\ 0 & 0 \end{bmatrix}}_{B} \begin{bmatrix} \hat{v}_S \\ \hat{d} \end{bmatrix} \tag{50}$$

$$\hat{v}_O = \underbrace{\begin{bmatrix} \frac{Rr_C}{R+r_C} & 0 & 0 & 0 & \frac{R}{R+r_C} \end{bmatrix}}_{C} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{v}_{C2} \\ \hat{v}_{CO} \end{bmatrix} \tag{51}$$

$$G_p(s) = \hat{v}_O(s) \Big/ \hat{d}(s)$$

$$= \frac{(1054s^4 + 3.512 \times 10^9 s^3 + 9.75 \times 10^{14} s^2 + 3.25 \times 10^{20} s - 1.361 \times 10^{11})}{s(s^4 + 1952s^3 + 9.26 \times 10^{10} s^2 + 1.806 \times 10^{14} s + 5.435 \times 10^{18})} \tag{52}$$

$$G_r(s) = \frac{(1.054 \times 10^4 s + 3.512 \times 10^9)}{(s^2 + 1952s + 5.873 \times 10^7)} \tag{53}$$

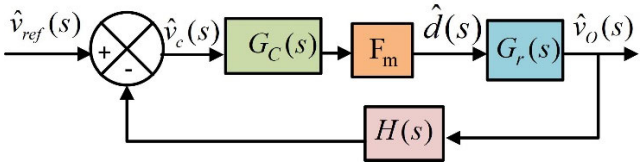

FIGURE 9. Voltage control loop schematic diagram.

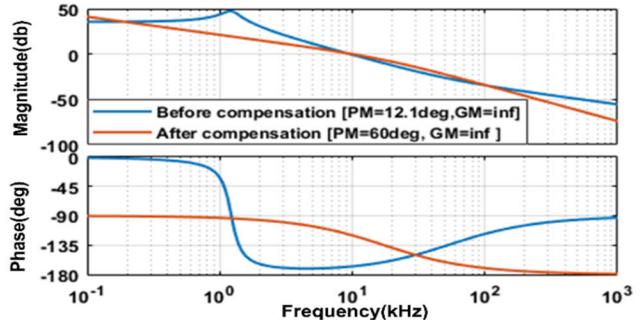

FIGURE 10. Bode diagram of compensated and uncompensated transfer functions of output voltage.

been calculated after considering the magnitude of the loop gain to be 1 at $\omega = \omega_c$,

$$(k_c \times F_m \times k_L) \Big/ \omega_c \sqrt{1 + (\omega_c / \omega_p)^2} = 1 \tag{56}$$

Therefore,

$$k_c = \omega_c \sqrt{1 + (\omega_c / \omega_p)^2} \Big/ (F_m \times k_L) \tag{57}$$

with k_L being constant open loop gain of the reduced order plant model. Following these simple mathematical calculations, k_c has been found to be 3638.4 and the derived controller transfer function is

$$G_C(s) = \frac{6.195 \times 10^{-5} s^2 + 0.1208\, s + 3638}{s(2.757 \times 10^{-11} s^2 + 1.219 \times 10^{-5} s + 1)} \tag{58}$$

Pole zero cancellation technique is an effective way to compensate undesirable effects posed by the plant poles as arbitrary pole placement (APP) is not recommended to design output feedback controller. The APP method demands higher order controller or use of full state feedback controller after checking the rank of the controllability matrix to be same as system order [21]. Finally, the passive components of the compensator have been determined considering availability and ease of use, the resistors R'_{C1}, R'_{f3}, R'_{f1}, R'_{f2}, have been selected to be 20kΩ, 1.33kΩ, 25kΩ and 1.1kΩ respectively and the capacitors C'_{C1}, C'_{C2}, C'_{Cf3} have been selected to be 7.1nF, 0.155nF and 2.66nF respectively in the hardware prototype. The frequency response plot of the proposed converter before and after the realization of controller has been recorded in Fig.10. The figure clearly shows the improved phase margin of 60^0 and a gain crossover frequency of 10 kHz compared to the phase margin of 12.1^0 and gain crossover

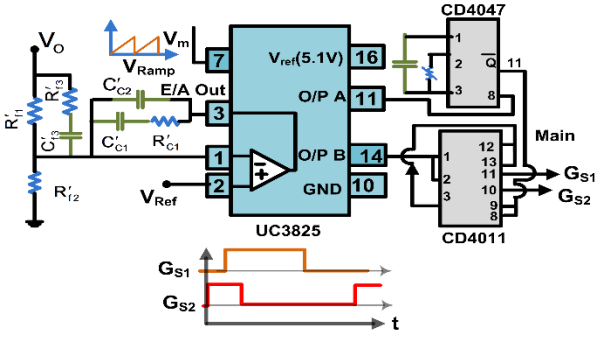

FIGURE 11. Implementation of controller using UC3825.

frequency of 9.58 kHz of uncompensated system. A PWM controller IC (UC3825) is employed for pulse generation and two IC CD4011, CD4047 are used for making the delay between pulses and to set the auxiliary pulse width as shown in Fig.11.

The power circuit proposed control scheme, although uses multiple energy storing elements, exhibits the dynamics of a traditional 2nd order system and hence realized with a low cost analog PWM controller with simple PI compensator.

VI. EFFICIENCY ESTIMATION

To investigate the efficiency of proposed soft switched buck converter the average and root mean square (RMS) value of currents flowing through different elements should be considered. The required equations are depicted in Table 2.

However, the power dissipation of control circuit, which is independent of load condition and accounts for a small fraction of total power loss, has not been considered in the efficiency analysis.

Due to soft switching of both the switches at turn on and turn off, the switching loss is zero. Therefore, the losses comprises of core, conduction and forward voltage drops are noted in Table 3. The parasitics of the components is also given in Table 3, in which r_{L1}, r_{L2}, r_{L3} are the equivalent series resistance (ESR) of inductor L_1, L_2, L_3 respectively.

Similarly $V_{FD1}, V_{FD2}, V_{FD3}$ denotes the forward voltage drop, r_{D1}, r_{D2}, r_{D3} represents on state resistance of diode D_1, D_2 and D_3 respectively. The resistance $r_{DS(m)}, r_{DS(a)}$ are the conduction resistances of main and auxiliary switch, whereas r_{C1}, r_{C2}, r_{CO} are internal resistances of snubber, resonant and output capacitor respectively. The theoretical loss distribution and efficiency estimation of the experimental prototype at full load is shown in Table 3. The core loss of selected resonant inductors (L_2, L_3) and buck inductor (L_1) at (100 kHz, B = 100mT, T = 1000C) are ≤0.23W (EE2506) each and ≤0.68W (EE3012) respectively.

Based on Fig.12, loss related with the switches are 2.71% of the total loss whereas maximum loss of 46.72% is for the forward voltage loss of diodes. The loss associated with inductor and for conduction of diodes are 42.03% and 8.38% of the total loss respectively. Again, the loss of snubber capacitor and resonant capacitors are insignificant due to

TABLE 2. Various average and RMS values for loss calculation.

RMS CURRENT OF INDUCTORS	$I_{L1}^{RMS} \approx I_O$	$I_{L2}^{RMS} = (I_O/4)\sqrt{d_3+d_4+d_5+d_6+d_7} = (0.6I_O/4)\sqrt{d}$	$I_{L3}^{RMS} = I_O\sqrt{d_1+d_2+d_3+d_4+d_5+d_6} = 0.515I_O\sqrt{d}$
RMS AND AVERAGE CURRENT OF DIODES	$I_{D1}^{RMS} = I_O\sqrt{d_1+d_{10}} \cong I_O\sqrt{(1-d)}$ $I_{D1}^{AVG} = (1-d)I_O$	$I_{D2}^{RMS} = (I_O/4)\sqrt{d_3+d_4+d_5+d_6+d_7} = (0.6I_O/4)\sqrt{d}$ $I_{D2}^{AVG} = \frac{I_O}{4}(d_3+d_4+d_5+d_6+d_7) = 0.36\frac{I_O d}{4}$	$I_{D3}^{RMS} = I_O\sqrt{d_4+d_5+d_6} = 0.439I_O\sqrt{d}$ $I_{D3}^{AVG} = I_O(d_4+d_5+d_6) = 0.193\,d\,I_O$
RMS AND AVERAGE CURRENT OF CAPACITORS	$I_{C1}^{RMS} = I_O\sqrt{d_2} = 0.21I_O\sqrt{d}$ $I_{C1}^{AVG} = 0$	$I_{C2}^{RMS} = I_O\sqrt{d_1+d_2+d_3+d_5+d_6+d_7} = 0.1453I_O\sqrt{d}$; $I_{C2}^{AVG} = 0$	$I_{CO}^{RMS} = \Delta i_{L1}/12 = 0.1I_O/12$ $I_{CO}^{AVG} = 0$
RMS CURRENT OF SWITCHES	$I_{S1}^{RMS} = I_O\sqrt{d}$	$I_{S2}^{RMS} = I_O\sqrt{d_1+d_2+d_3+d_4} = 0.4424I_O\sqrt{d}$	

TABLE 3. Distribution of losses and efficiency analysis.

Power Loss (Type)	Power Loss(W)	% age of total Loss
Conduction loss of S1 and S2	0.11W	2.71%
Conduction loss of Inductors	0.57W	14.15%
Core loss of inductors	1.14W	27.88%
Conduction loss of diodes	0.34W	8.38%
Forward voltage loss of diodes	1.91W	46.82%
Conduction loss of capacitors	0.002W	0.06%
Total Loss	4.09W	Efficiency (%)
		97.24%
$P_O = 144Watt, V_S = 24V, f = 100kHz, d = 0.4, r_{L1} = 15m\Omega$ $r_{L2} = 7m\Omega, r_{L3} = 5m\Omega, r_{DS1} = 2.8m\Omega, r_{DS2} = 8m\Omega, r_{D1} = 15m\Omega$ $r_{D2} = 10m\Omega, r_{D3} = 20m\Omega, V_{FD1} = 0.53V, , V_{FD2} = 0.6V$ $V_{FD3} = 0.62V, r_{CO} = 20m\Omega.$		

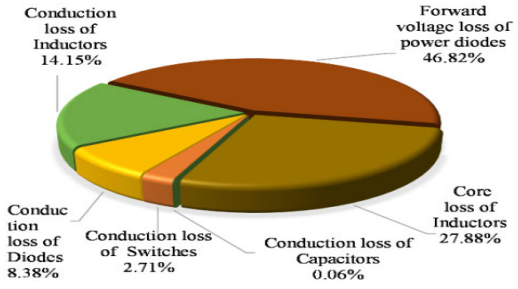

FIGURE 12. Power loss distribution of the converter.

very negligible resistance and conduction time the loss in capacitors including output capacitor are only 0.06% of the total loss.

VII. COMPARISON WITH OTHER CONVERTERS

In order to inculcate the superiority in performance of the proposed converter, a comparison is carried out in Table 4 with some other structures and conventional buck converter.

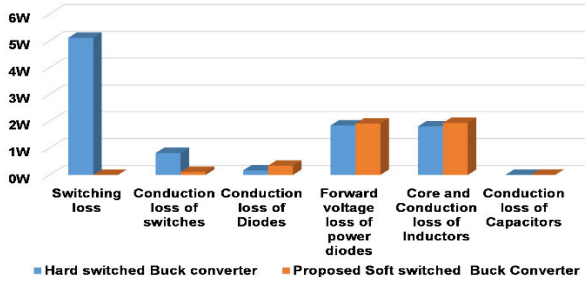

FIGURE 13. Comparison of power loss between conventional hard switched buck converter and proposed converter.

In [4] an auxiliary network is utilized for ZVS phenomenon at turn on hard turn of the main switch decreases efficiency.

The same problem of hard turn off persists in [2], [4], and [7], and [9] along with hard commutation of diodes except the ZCS turn of diode in [2]. Due to bidirectional nature of auxiliary inductor [7], [8] and main inductor in [7], power drawn by the inductor is more for magnetic alignment and as a result peak current of the switch is very high (more than 2 times of load current). The ZCS on of the switch is totally dependent on the negative current conduction time of auxiliary inductor which is very short and does not depend on load current. In [8], the use of variable inductor increases the volume of the converter and in context of close loop control, it is very difficult and complex to get ZCS by controlling dc current of variable auxiliary inductor for variable load. In comparison to other structures the switches can achieve full soft switching condition at variable load by simple voltage mode control with high efficiency and with very less current stress at main switch. Also, In comparison with classical hard switched buck converter in Fig.13 for the same power the switching loss is 5.11W (52.42% of total loss) whereas zero loss in proposed converter and the conduction loss also reduced from 8.38% to 2.71%.

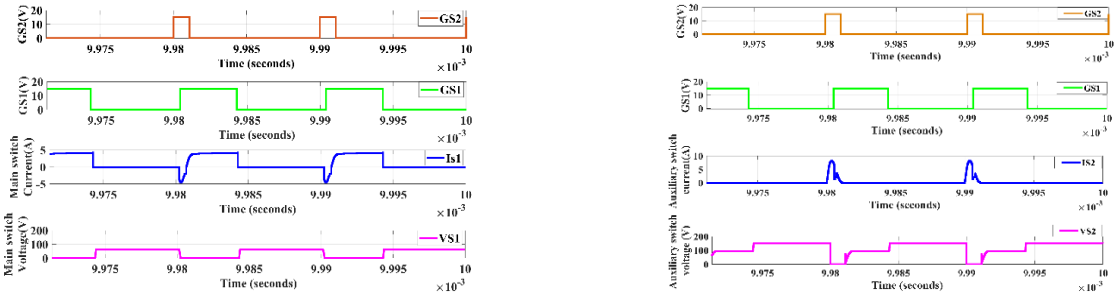

FIGURE 14. Simulated waveforms (a) Top: Auxiliary switch trigger pulse (G_{S2}), 2nd: Main switch trigger pulse (G_{S1}), 3rd: main switch current (i_{S1}), bot: Main switch voltage (v_{S1}), (b) Top: Auxiliary switch trigger pulse (G_{S2}), 2nd: Main switch trigger pulse (G_{S1}), 3rd: Auxiliary switch current (i_{S2}), bot: Auxiliary switch voltage (v_{S2}).

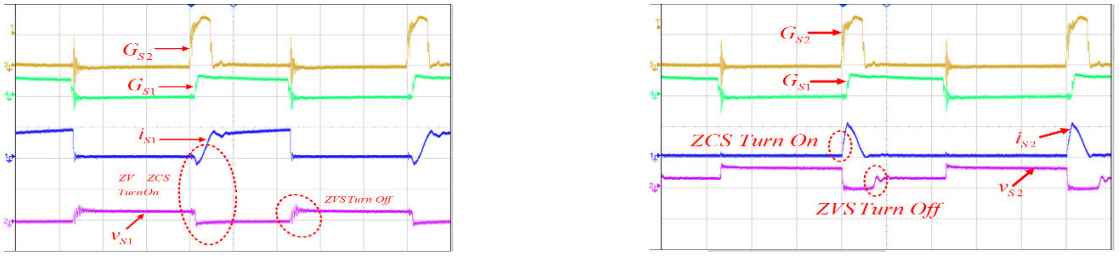

FIGURE 15. Experimental waveforms: (a) trace 1: gold: Auxiliary switch trigger pulse ($G_{S2} = 10V/div$), trace 2: green, Main switch trigger pulse ($G_{S1} = 20V/div$), trace 3: blue: main switch current (i_{S1}), scale (5A/div), trace 4: pink, main switch voltage (v_{S1}), scale (200V/div Time scale: 2μs/div; (b) trace 1: gold: Auxiliary switch trigger pulse ($G_{S2} = 10V/div$), trace 2: green, Main switch trigger pulse ($G_{S1} = 20V/div$), trace 3: blue: Auxiliary switch current (i_{S2}), scale (5A/div), trace 4: pink, Auxiliary switch voltage (v_{S2}), scale (200V/div), Time scale: 2μs/div.

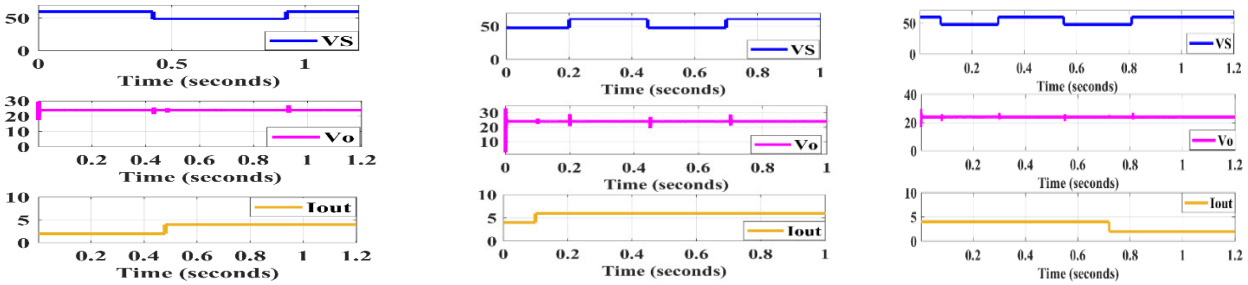

FIGURE 16. Simulated waveforms (a) output voltage transient response against step change in supply voltage (60-to-48V- to-60V and the load current from 2-to-4A Top: Input voltage (V_S), 2nd: Output voltage (V_O), bot: output current (I_O), (b) output voltage transient response against step change in supply voltage (48V-to-60V- to-48V and the load current from 4A-to-6A Top: Input voltage (V_S), 2nd: Output voltage (V_O), bot: output current (I_O), (c) output voltage transient response against step change (60V-to-48V- to-60V and the load from 6Ω-to-12Ω Top: Input voltage (V_S), 2nd: Output voltage (V_O), bot: output current (I_O).

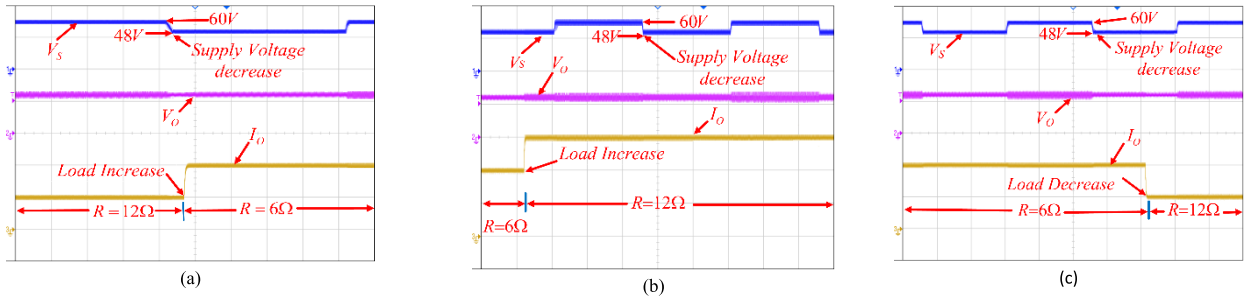

FIGURE 17. Experimental results: (a) Dynamic response against step change in supply voltage (60V to 48V and again back to 60V and step change in load current from 2A to 4A (trace 1 (blue): Supply voltage ($V_S = 40V/div$), trace 2: pink, output voltage ($V_O = 20V/div$), trace 3: gold, output current (I_O), scale (2A/div), Time scale: 100ms/div; (b) output voltage transient response against step change in supply voltage (48V-to-60V- to-48V and the load current from 4A-to-6A (a) trace 1: blue, Supply voltage ($V_S = 40V/div$), trace 2: pink, output voltage ($V_O = 20V/div$), trace 3: gold, output current (I_O), scale (2A/div), Time scale: 100ms/div; (c) Dynamic response against step change in supply voltage (60V-to-48V- to-60V and the load from 6Ω-to-12Ω (a) trace 1: blue, Supply voltage ($V_S = 40V/div$), trace 2: pink, output voltage ($V_O = 20V/div$), trace 3: gold, output current (I_O), scale (2A/div), Time scale: 100ms/div.

TABLE 4. Comparison between proposed converter and other buck converters.

Ref	Main switch voltage stress	Main switch Current stress	Buck diode voltage stress	Switching Transitions		Buck diode comm utation	Switching frequency f_s (kHz)	Switching devices		D_N	L_N /C_N	T_{CC}	Efficiency [%]
				Turn-on	Turn-off			S_m	S_a				
TR	V_S	$I_O + \Delta i_L/2$	V_S	Hard	Hard	Hard	100	1	-	1	1/1		93.5
[9]	V_S	$> I_O + \Delta i_L/2$	V_S	S1-ZVS Sa-ZCS	Hard Sa-hard	Hard	125	1	1	2	2/2	8	95
[2]	V_S	$> I_O + \Delta i_L/2$	$\frac{(1+n)}{(1+2n)V_S}$	S1-ZVS S2-ZVS	Hard	ZCS	100	2	-	2	3/3	10	94
[7]	V_S	$> 2I_O + \Delta i_L/2$	V_S	S1-ZVS	Hard	ZCS	37	1	-	1	2/3	7	96.78
[8]	V_S	$> 2I_O + \Delta i_L/2$	V_S	S1-ZVS	S1-ZVS	ZCS	75	1	-	1	2/2	6	97.17
[4]	V_S	$(n-k_2)i_{Da} + I_O$	V_S	S1-ZVS S2-ZVS	Hard	ZCS	100	2	-	1	2/1	6	93.5
[10]	V_S-V_O	$\gg I_O + \Delta i_L/2$	$(V_S$-$V_O)/n$	S1-ZVS S2-ZVS	Hard	Hard	50	2	-	2	2/2	8	93.8
Prop#	V_S	I_O	V_S	S1-ZV-ZCS S2-ZCS	S1-ZVS S2-ZVS	ZCS	100	1	1	3	3/3	11	97.24

D_N:No of diodes,L_N:No of Inductors,C_N:No of capacitors,S_m: Main switch,S_a: Auxiliary switch,T_{CC} :Total component count ,Prop#: Proposed Converter

VIII. PERFORMANCE ANALYSIS AND DISCUSSION

Soft-switched buck converter with closed loop control arrangement as shown in Fig.1 has been fabricated to validate the theoretical analysis and real time performance of the converter. The detailed specification and components used for laboratory scale hardware prototype are given in Table 1. The typical experimental observations as current and voltage waveforms of switching devices have been recorded to validate the soft switching transition of the switches. Fig.14(a) shows the simulated results wherein Fig.15(a) displays the experimental waveforms of voltage ($\boldsymbol{v_{S1}}$) and current ($\boldsymbol{i_{S1}}$) of the main switch along with corresponding gate pulses. It is observed that, the gate pulse ($\boldsymbol{G_{S1}}$) has been applied to the main switch ($\boldsymbol{S_1}$) while its body diode has been in conduction, impressing zero voltage across main power switch ($\boldsymbol{S_1}$) and the current ($\boldsymbol{i_{S1}}$) rises slowly from zero. This establishes ZV-ZCS turn on of the main switch. Turn-off of this switch is clearly evident to occur under ZVS condition, as the impressed voltage ($\boldsymbol{v_{S1}}$) develops slowly after removal of the gate pulse. The switching behaviour of the auxiliary switch ($\boldsymbol{S_2}$) in simulation and experimentation depicted in Fig. 14(b) and Fig.15 (b) respectively. When the gate trigger pulse ($\boldsymbol{G_{S2}}$) is applied to switch ($\boldsymbol{S_2}$), the current ($\boldsymbol{i_{S2}}$) increases slowly and the switch ($\boldsymbol{S_2}$) turns on with ZCS. Voltage ($\boldsymbol{v_{S2}}$) across auxiliary switch ($\boldsymbol{S_2}$) develops slowly on removal of its gate pulse and thus ZVS turn off is established.

Dynamic performance of the prototype model in response to sudden changes in supply voltage and loading conditions have also been tested in closed loop with the type III compensator and the important observations are exhibited. Fig.16 and Fig 17 show the simulated as well as experimental results respectively, describing changes in output voltage against step change in supply voltage from 60V to 48V and again back to 60V along with step changes in loading conditions. In Fig.17 (b), the load current changes from nominal load 4A to full load current 6A along with the variation of input supply voltage (V_S). The recorded output voltage (V_O) remains constant with permissible amount of undershoot and overshoot. Correspondingly, Fig.17 (a), Fig.17(c) validates the simulated result of Fig.16(a) and 16(c) and also establishes effectiveness of the controller in tight regulation of the output voltage and fast dynamic response against step disturbance in supply voltage (V_S) and load (R). The salient attributes of proposed converter in terms of electrical parameters are compared with other references and detailed in Table 5. A highly appreciable line and load regulation and output accuracy with moderate ripple voltage makes the proposed converter much superior to other options. The laboratory experimental setup is presented in Fig.18.

From the parameters of Table 2, the theoretical efficiency of the proposed converter has been computed at various loading conditions (20% to 110% of full load) with a nominal input voltage of 48V and an efficiency comparison of the proposed converter with some other conventional buck converters has been plotted in Fig. 19.

Based on the data in Table 3, the theoretical efficiency at full load is 97.24% whereas the maximum efficiency of 97.09% is recorded at full load.

The efficiency computed at different input voltages and output power levels have been shown in Table 6. A maximum efficiency of 96.50% at 33.33% load and 97.30% full load efficiency establishes supremacy of proposed converter. The efficiency is relatively greater at high input voltage because of lesser conduction loss due to low duty cycle and

TABLE 5. Comparison of electrical parameters between proposed buck converter and other references.

Output Parameters	[8]	[28]	[1]	[23]	[27]	Proposed converter
Load regulation	7.5%	1.8%	9%	1.45%	2.5%	0.4%
Line regulation	6.25%	0.32%	Not performed	Not performed	Not performed	0.63%
Output accuracy	±2.08%	±2%	±1.12%	±1.4%	±1%	± 0.5%
Output voltage ripple	$> 120\ mV_{P-P}$	$< 50\ mV_{P-P}$	$140\ mV_{P-P}$	$< 130\ mV_{P-P}$	$100\ mV_{P-P}$	$< 90\ mV_{P-P}$
Feedback voltage	24V /Voltage controlled	5V/Current mode control	Open Loop	3.3V/Peak current control	100V/RESO control	23.22V/Voltage controlled
Transient response (Settling time)	1ms	0.075ms	Open Loop	27µs	100ms	5ms

TABLE 6. Input voltage vs efficiency data.

Input Voltage (V_S) (V)	Output Power (P_O) (W)	Efficiency (η) (%)
60	48	96.50
48	48	95.20
40	48	95.00
60	144	97.30
48	144	97.24
40	144	97.05

FIGURE 18. Experimental set up of proposed soft switched buck converter.

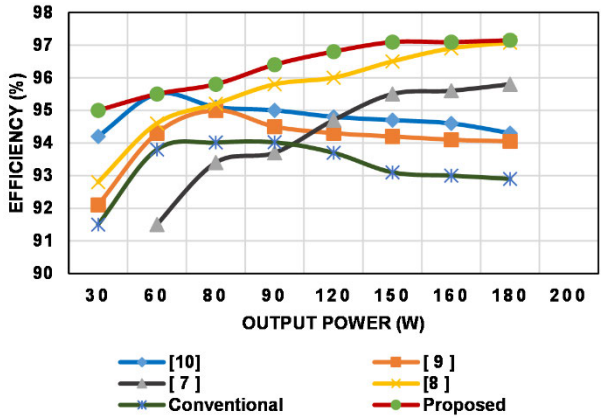

FIGURE 19. Comparison of efficiency with other step down structures.

minimum circulating current through body diode compared to low input voltage. It is evident that efficiency is reasonably high throughout the entire operating range.

IX. CONCLUSION

This article has proposed a soft switched DC/DC buck converter, which uses an auxiliary network to aid soft switching transition of the semiconductor devices over a wide load power range. The superior advantages of the proposed scheme are:

1) High efficiency at low power application.
2) The ZV-ZCS turn on and ZVS turn off of main switch with no additional current stress are achieved for wide load variation, while the auxiliary switch realizes ZCS turn on and ZVS turn off.
3) The quasi-resonant charging discharging cycle within the network L and C elements does not create any additional voltage and current stress especially in the main switch responsible for power transfer.
4) The auxiliary and other power diodes which supports this process were also made sure to undergo soft commutation.
5) Simple restructurable auxiliary cell with complete design with easy single loop voltage control for practical application.
6) The requirement of variable inductors (that increase the volume, cost and overall complexity) with DC current control to ensure soft transition of switches with wide load variations is eliminated.
7) Negligible power loss in the auxiliary components, while the resonant capacitor recycles power to the source.
8) Decoupled auxiliary circuit dynamics.

Steady-state dynamic behaviour of the converter in different modes has been described through mathematical expressions and the small signal model has been developed from the dynamic equations considering all the modes. Besides, it has been observed that the dynamic profile of this apparent higher order converter actually takes after a second order dynamics which in due course demanded a design of type III compensator based on pole-zero cancellation technique so as to sustain stability while negotiating external disturbances.

Finally, a 150W laboratory scale hardware model of proposed topology of the soft-switched buck converter has been developed for real time performance verification.

The experimental results have clearly validated soft-switching behaviour of the semiconductor devices and satisfactory transient response against step changes in supply voltage and load current. Hence, the converter exhibits considerably higher efficiencies at all the loads and maximum experimental efficiency of 97.09% at full load.

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