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RESEARCH ARTICLE

Advanced DPWM Method for Switching Loss Reduction in Isolated DC Type Dual Inverter With Open-End Winding IPMSM

HYUNG-WOO LEE, (Student Member, IEEE), SUNG-JIN JANG, (Student Member, IEEE), AND KYO-BEUM LEE, (Senior Member, IEEE)

Department of Electrical and Computer Engineering, Ajou University, Suwon 16499, South Korea

Corresponding author: Kyo-Beum Lee (kyl@ajou.ac.kr)

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ABSTRACT This paper proposes an advanced discontinuous pulse-width modulation (DPWM) scheme for a dual inverter to reduce switching loss. A dual inverter is used to drive an open-end winding interior permanent magnet synchronous motor (OEW-IPMSM). It is composed of double two-level inverters with large switching loss owing to the use of 12 switching devices. When a current phase changes, the switching loss cannot be minimized by using a conventional DPWM scheme. As the conventional DPWM scheme uses reference voltage for switching, the switching loss cannot be minimized due to the difference between the phases of the stator current and phases of reference voltages. However, the proposed DPWM scheme with additional calculations of the current phase can minimize switching loss. When the current phase changes, the proposed DPWM is switched to $\pm 30^{\circ}$ of the maximum point of the current. Furthermore, the effectiveness of the proposed switching loss reduction ability is verified through simulations and experimental results.

INDEX TERMS Dual-inverter, open-end winding interior permanent magnet synchronous motor (OEW-IPSM), discontinuous pulse width modulation (DPWM).

I. INTRODUCTION

Interior permanent magnetic synchronous motors (IPMSMs) are widely used in various industrial fields, such as electric vehicles and home appliances, owing to their high power density, high torque density, and high efficiency [1], [2], [3], [4], [5]. A general motor drive system has disadvantages in terms of weight and volume because it includes a boost converter to expand its operating range [6], [7]. To overcome these disadvantages and increase the voltage utilization rate, open-end winding interior permanent magnet synchronous motors (OEW-IPMSM) drives operated via a dual inverter have been widely researched [8], [9], [10], [11], [12]. A dual inverter comprises two 2-level inverters, with the configuration offering several advantages. The rated voltage of the dual inverter doubles when the same switch device is utilized, which is significant for high-voltage and high-power applications [13]. In addition, the dual inverter has a three-level effect with advantages such as the absence of neutral-point control. Moreover, because of the boosting influence of the voltage, the OEW-IPMSM can achieve higher speed and power density then a single 2-level inverter [14]. In addition, the fault tolerance is improved owing to the phase currents of the OEW-IPMSM being independently controlled [15].

Depending on the connection status of each inverter, the OEW-IPMSM system fed by the dual inverter can be classified into three topologies comprising two isolated DC source types: one being an isolated voltage source and floating capacitor type, and the other as common voltage source type. A dual inverter with a common DC power source offers advantages related to cost and volume of the system. A zero-sequence current (ZSC) is formed in this system such that the torque ripple and switching loss are increased [16], [17]. Further, a dual inverter with the floating capacitor can extend the speed range of the OEW-IPMSM and

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supply the machine with a multilevel pulse-width modulated (PWM) voltage, thereby reducing the current ripple for PM motors exerting a small synchronous inductance [18]. In addition, the dual inverter can be used as a power factor compensator for the main inverter, which can transfer the maximum active power to the motor [19]. Using two isolated DC sources, the dual invertor can easily control the OEW-IPMSM, and the ZSC is zero as the sources are electrically isolated. Thus, an additional control method was not required. However, the use of an isolated source increases the cost and volume of the system because of the two isolated DC sources [20], [21]. Moreover, as the dual inverter comprises 12 power semiconductors, the switching loss are higher than the single 2-level inverter. To reduce switching loss, a discontinuous pulse width modulation (DPWM) method has been proposed [22], [23], [24]. The DPWM method locks certain power semiconductors as ON or OFF in a specific interval. Hence, it is advantageous in terms of efficiency compared to space vector PWM (SVPWM) in high-power and high-switching frequency applications [25]. Further, the 30°, 60°, and 120° DPWM methods have been proposed, which are clamped to the top and bottom. The DPWM avoided switching transition in the 30° range before and after the phase current peaks, thereby reducing the switching loss by an average of 33% [26]. In addition, using the DPWM considering the phase difference between current and voltage reduces switching loss even when the power factor (PF) changes [27]. Therefore, the DPWM can reduce switching loss and improve the system efficiency.

This paper proposes a DPWM scheme that considers the current phase of the dual inverter to reduce switching loss. The proposed DPWM scheme is suitable for high power applications since it has advantage in reducing switching losses. In case of a change in the current phase, switching loss cannot be minimized using the DPWM scheme. However, the proposed DPWM scheme combines with additional calculations of the current phase can minimize switching loss. When the current phase changes, the proposed DPWM scheme changes the reference voltage, such that discontinuous modulation occurs based on the current. Moreover, the proposed DPWM does not switch at ±30° from the maximum point of the current. The accuracy for current measurement should be ensured for the application of the proposed DPWM technique. The performance of the proposed switching loss reduction ability is verified through appropriate simulations and experimental results.

II. OEW-IPMSM DRIVING SYSTEM MODELING

A. MODELING OF DUAL-INVERTER WITH ISOLATED DC SOURCE AND OEW-IPMSM

The dual inverter is composed of two 2-level inverters as shown in Fig. 1. The two-level inverter has eight switching states. Vector diagrams of inverters 1 and 2 are shown in Fig. 2. If the two isolated DC voltages of the dual inverter are different, the same power source should be used as common

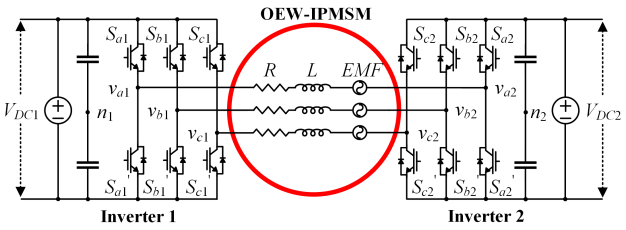

FIGURE 1. OEW-IPMSM and dual-inverter with two isolated power sources.

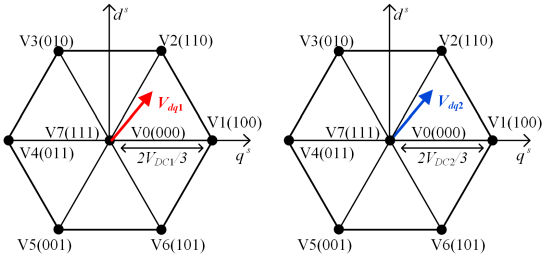

FIGURE 2. Space voltage vectors of dual inverter with isolate DC source.

mode voltage (CMV) occurs in all vectors, except when inverters 1 and 2 output zero vectors. Further, owing to the same DC link voltages of inverters 1 and 2, the dual inverter has 64 switching states. If the switching states of the upper and lower switches on the same leg are complementary, then S_{a1}, S_{b1}, S_{c1}, S_{a2}, S_{b2}, and S_{c2} are used to indicate the switching state. The phase voltage of the stator winding in the dual inverter can be expressed as the difference between the phase voltages of inverters 1 and 2. The phase voltage of the dual inverter can be described as

$$\begin{aligned}\begin{bmatrix} v_{a12} \\ v_{b12} \\ v_{c12} \end{bmatrix} &= \begin{bmatrix} v_{an1} - v_{an2} - v_{an1n2} \\ v_{bn1} - v_{bn2} - v_{bn1n2} \\ v_{cn1} - v_{cn2} - v_{cn1n2} \end{bmatrix} \\ v_{xn1\,(x=a,\,b,\,c)} &= V_{DC1}\left(S_{x1\,(x=a,\,b,\,c)} - 0.5\right) \\ v_{xn2\,(x=a,\,b,\,c)} &= V_{DC2}\left(S_{x2\,(x=a,\,b,\,c)} - 0.5\right) \end{aligned} \tag{1}$$

where v_{an1}, v_{bn1}, and v_{cn1} are the a-, b-, and c-axis terminal voltages of inverter 1, and v_{an2}, v_{bn2}, and v_{cn2} are the a-, b-, and c-axis phase voltages of inverter 2, respectively. Further, V_{DC1} and V_{DC2} are the DC-link voltages of inverters 1 and 2, respectively.

The OEW-IPMSM opens the neutral point of the conventional Y-connected IPMSM. An OEW-IPMSM driven by a dual inverter with an isolated DC source is shown in Fig. 1. The model of the OEW-IPMSM with the d-q synchronous rotating reference frame can be expressed using the Clarke and Park transformations as

$$\begin{aligned}\begin{bmatrix} u_{de} \\ u_{qe} \end{bmatrix} &= \begin{bmatrix} L_d \frac{di_{de}}{dt} + R_s i_{de} - \omega_r L_q i_{qe} \\ L_q \frac{di_{qe}}{dt} + R_s i_{qe} + \omega_r L_d i_{de} + \omega_r \lambda_f \end{bmatrix} \\ T_e &= \frac{3}{2}\frac{P}{2}\left(\lambda_f i_{qe} + \left(L_d - L_q\right) i_{de} i_{qe}\right) \end{aligned} \tag{2}$$

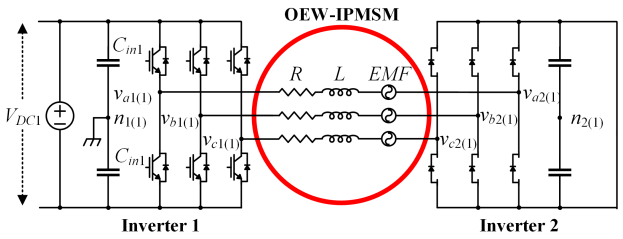

FIGURE 3. When V_{DC2} is 0 V, dual inverter circuit using superposition principle (Case 1).

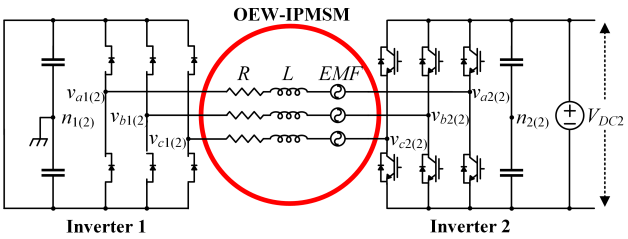

FIGURE 5. When V_{DC1} is 0 V, dual inverter circuit using superposition principle (Case 2).

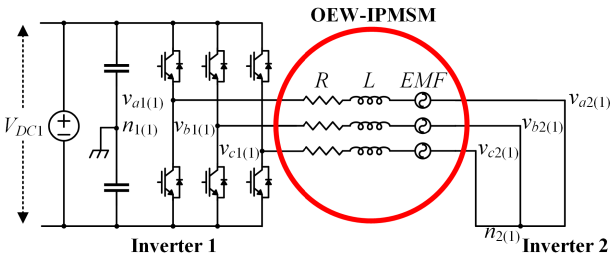

FIGURE 4. Equivalent dual inverter circuit of Case 1.

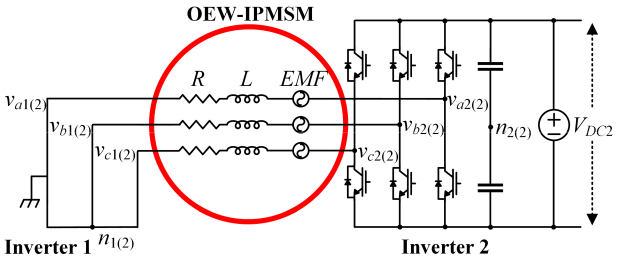

FIGURE 6. Equivalent dual inverter circuit of Case 2.

where u_{de} and u_{qe} are the d-q axis voltages of the stator, T_e is the electromagnetic torque, P is the number of poles, I_{de} and I_{qe} are the d-q axis currents of the stator, R_s is the stator resistance, L_d and L_q are the d-q axis stator inductance, ω_r is the electrical angle if the velocity, electrical angle of the motor, and λ_f is the fundamental flux linkage. Simulations were performed via modelling using equation (1) and equation (2).

B. ANALYSIS OF DUAL INVERTER PHASE VOLTAGE

The dual inverter is a topology that drives the load of the OEW structure. The Y-connection load has a neutral point of load, whereas the OEW-connection load does not. Therefore, the relationship between the terminal, phase, and line voltages of the dual inverter was analyzed using the superposition principle. Because the dual inverter has two isolated power sources, the phase voltage of the OEW load was analyzed in Case 1 and Case 2. In Case 1, the input voltage of inverter 2 (V_{DC2}) was zero. The dual inverter in Case 1 is shown in Fig. 3. Assuming that the diode is an ideal switch, the a-, b-, and c-phase output voltages of inverter 2 ($v_{a2(1)}$, $v_{b2(1)}$, $v_{b2(1)}$) had the same voltage regardless of the direction of the output current. The equivalent circuit of Case 1 is shown in Fig. 4. The phase voltage output from inverter 1 was a sinusoidal wave. The a-axis phase voltage of Case 1 can be expressed as equation (3)

$$\begin{aligned} v_{a12(1)} &= v_{a1(1)} - v_{a2(1)} = v_{a1(1)} - v_{n2(1)} \\ &= A\sin(\omega t) \end{aligned} \tag{3}$$

Case 2 is when V_{DC1} is zero. The dual inverter in Case 2 is shown in Fig. 5. Assuming that the diode is an ideal switch, the a-, b-, and c-phase output voltages of inverter 1 ($v_{a2}(1)$, $v_{b2(1)}$, $v_{c2(1)}$) had the same voltage regardless of the direction of the output current and were zero. The equivalent circuit for Case 2 is shown in Fig. 6. The phase voltage output from inverter 2 was a sinusoidal wave. The a-axis phase voltage of Case 2 ($v_{a12(2)}$) is expressed as equation (4).

$$\begin{aligned} v_{a12(2)} &= v_{a1(2)} - v_{a2(2)} = 0 - v_{a2(2)} \\ &= B\sin(\omega t) \end{aligned} \tag{4}$$

The a-axis phase voltage of the OEW load is the sum of the a-axis phase voltages of Cases 1 and 2, and is expressed as equation (5)

$$\begin{aligned} v_{a12} &= v_{a12(1)} + v_{a12(2)} = v_{a1(1)} - v_{n2(1)} - v_{a2(2)} \\ &= (A+B)\sin(\omega t) \end{aligned} \tag{5}$$

The phase voltages of the OEW load are a sinusoidal wave, and no offset voltage appeared. However, the phase voltage can be boosted using the common-mode voltage ($v_{n2(1)}$) of the a-axis phase voltage component ($v_{a(2)}$) compared to a single inverter. Because the two DC sources of the dual inverter are isolated, no current path is followed by switching and the ZSV. As ZSC is not generated, the additional ZSC and reduction method is not required. In Case 1, the line voltage between the a-axis and b-axis of inverter 1 is expressed as equation (6).

$$v_{ab1(1)} = v_{a1(1)} - v_{b1(1)} \tag{6}$$

Further, in Case 2, the line voltage between the a-axis and b-axis of inverter 1 is, is expressed as equation (7).

$$v_{ab1(2)} = 0 \tag{7}$$

Thus, the line voltage of inverter 1 is the sum of equations (6) and (7), which is expressed as equation (8)

$$v_{ab1} = v_{ab1(1)} - v_{ab1(2)} = v_{a1(1)} - v_{b1(1)} \tag{8}$$

In addition, equation (9) is obtained using equation (3) as follows:

$$\begin{aligned} v_{ab1} &= v_{a12(1)} - v_{a2(1)} - v_{b12(1)} - v_{b2(1)} \\ &= v_{a12(1)} - v_{n2(1)} - v_{b12(1)} + v_{n2(1)} \end{aligned} \tag{9}$$

The line voltage output between the a- and b-axes of inverter 1 was a sinusoidal wave. The line voltage of the dual inverter is expressed as equation (10).

$$\begin{aligned} v_{ab1} &= A\sin(\omega t) - v_{n2(1)} - B\sin(\omega t - 120^\circ) + v_{n2(1)} \\ &= C\sin(\omega t + 30^\circ) \end{aligned} \tag{10}$$

Consequently, the offset voltages of inverters 1 and 2 have no effect on the OEW load (phase voltage) and line voltage. However, in case of the occurrence of overmodulation of the dual inverter owing to the offset voltage, an effect on the OEW load can be observed.

III. PROPOSED DISCONTINUOUS PULSE WIDTH MODULATION SCHEME

A. CONVENTIONAL DPWM

Case 2 represents a situation in which the DC-link voltage of inverter 1 V_{DC1} is zero. The dual inverter in Case 2 is shown in the DPWM scheme is used to reduce the switching loss and increase the efficiency of a high-power system with a high switching frequency. The DPWM method locks certain power semiconductors as ON or OFF at discontinuous modulation regions. The DPWM method can set discontinuous modulation regions according to the application used, but fundamentally selects points at which the magnitude of absolute value of the phase voltage is maximized to minimize the switching loss. The DPWM avoided switching transition thereby reducing the switching loss by an average of 33%. Hence, it is advantageous in terms of efficiency compared to space vector PWM (SVPWM). However, when there is phase difference between the phases of the stator current and reference voltages, the loss reduction effect by DPWM is reduced. In the conventional DPWM method, the discontinuous modulation region is simply determined by the phase of reference voltage, and thus, discontinuous modulation occurs for ±30° based on the maximum reference voltage. Hence, to improve the efficiency, the current phases must be considered. The offset voltage (V_{offset}) for 60° DPWM scheme is calculated using the reference a-, b-, and c-phase voltages (v_{as}, v_{bs}, v_{cs}) and V_{DC}, as expressed in equation (11)

$$\begin{aligned} V_{offset} &= \begin{cases} \frac{V_{DC}}{2} - v_{\max} & v_{\max} + v_{\max} > 0 \\ -\frac{V_{DC}}{2} - v_{\min} & v_{\max} + v_{\max} < 0 \end{cases} \\ v_{\max} &= \max(v_{as},\, v_{bs}^*,\, v_{cs}^*), \quad v_{\min} = \min(v_{as}^*,\, v_{bs}^*,\, v_{cs}^*) \end{aligned} \tag{11}$$

where max(·) and min(·) are the maximum and minimum values in brackets. The 60° DPWM scheme locks power semiconductors at the maximum point of the reference voltage. In case of same phases of the reference voltage and stator current, the switching loss can be reduced to the maximum with an average of 33%. In the OEW-IPMSM system, a phase difference between the reference voltage and current may occur, depending on the speed and control method. Fig. 8 and Fig. 9 show the phase of the stator current and reference voltage when the phase difference between the reference voltages of inverters 1 and 2. Therefore, the DPWM was not applied at the maximum point of the current, as shown in Figs. 8(b) and 9(b). Further, the switching loss did not reduce to a maximum, as shown in Figs. 8(a) and 9(b).

B. PROPOSED DPWM

The dual inverter is composed of double two-level inverters and has large switching loss owing to the 12 switching devices. To effectively reduce the switching loss for the dual inverter, a DPWM scheme was generated considering the current phase angle. A block diagram of the proposed DPWM scheme is shown in Fig. 7. The conventional DPWM was calculated using the reference phase voltages. The offset voltage of the proposed DPWM scheme is calculated using the phase angle (θ_i) of the d-q current and electrical angle (θ_r) of the motor. The proposed DPWM scheme determines a discontinuous modulation interval using a reference angle instead of reference phase voltages. The reference angle of the proposed DPWM scheme is calculated as follows:

$$\theta_i^* = \theta_i + \theta_r = \tan^{-1}\left(\frac{I_d^r}{I_q^r}\right) + \theta_r, \quad -\pi \le \theta_i^* \le \pi \tag{12}$$

The offset voltage of the proposed DPWM method was calculated using the reference angle of the proposed DPWM. The offset voltage of inverters 1 and 2 is shown in Table 1. where v_{as1}, v_{bs1}, and v_{cs1} are reference phase voltages of inverter 1, v_{as2}, v_{bs2}, and v_{cs2} are the reference phase voltages of inverter 2, and the offset voltages of inverters 1 ($v_{offset1}$) and 2 ($v_{offset2}$) are added to their phase voltages. The reference voltage is calculated as follows:

$$\begin{aligned} v_{xn1(x=a,\,b,\,c)} &= v_{xs1(x=a,\,b,\,c)} + v_{offset1} \\ v_{xn2(x=a,\,b,\,c)} &= v_{xs2(x=a,\,b,\,c)} + v_{offset2} \end{aligned} \tag{13}$$

The proposed DPWM scheme was applied at the maximum point of the current. Discontinuous modulation occurred at ±30° devices of the dual inverter were not switched during 60° period. The switching loss can be minimized. Further, the switching loss can be reduced to a maximum compared to the conventional DPWM scheme.

IV. SIMULATION RESULTS

Simulations of the dual inverter were performed using PSIM to demonstrate the efficiency of the proposed DPWM scheme. The circuit of the dual inverter used for the simulations is shown in Fig. 1, and the input voltage of

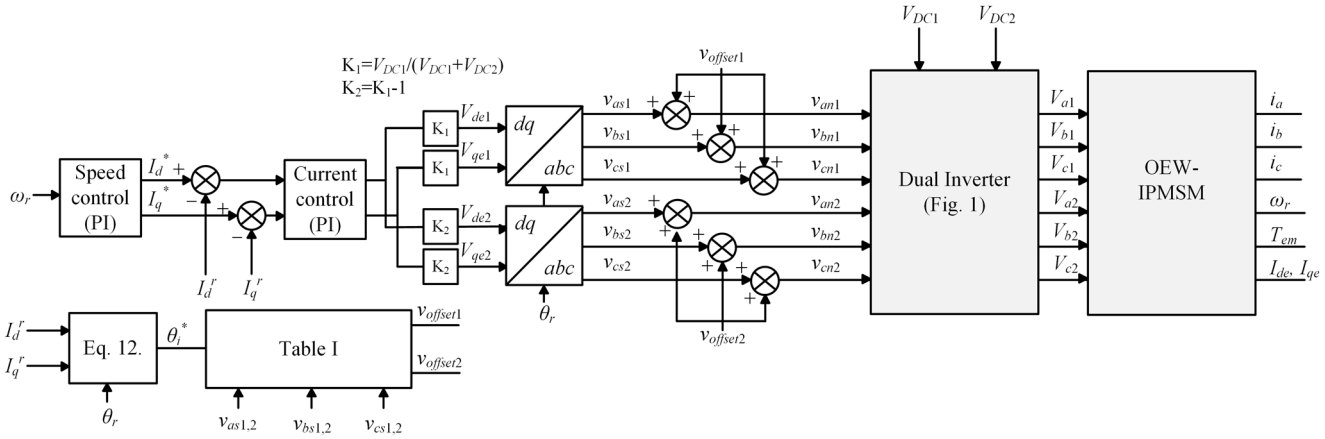

FIGURE 7. Block diagram of proposed DPWM method and dual inverter control method.

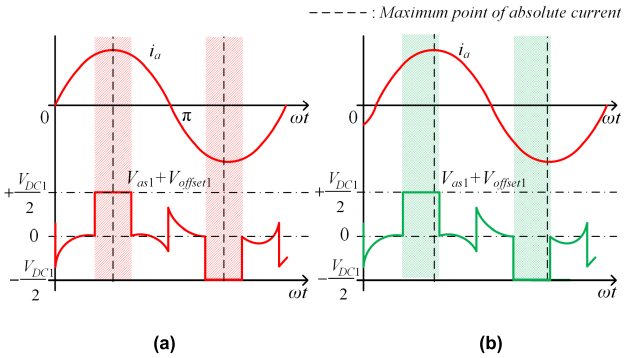

FIGURE 8. Stator current and reference voltage of inverter 1. (a) the proposed DPWM and (b) the conventional DPWM.

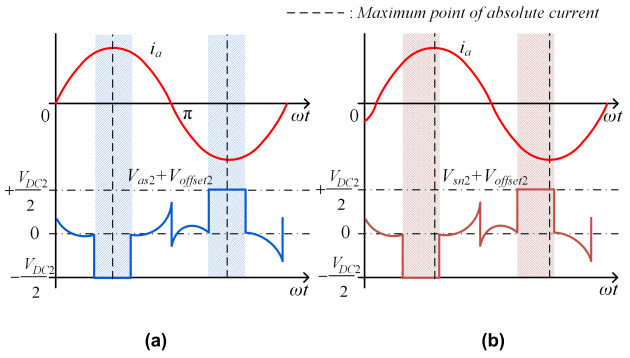

FIGURE 9. Stator current and reference voltage of inverter 2. (a) the proposed DPWM and (b) the conventional DPWM.

TABLE 1. Offset voltage of inverters 1 and inverter 2.

Reference angle(θ_i^*)	Offset voltage of inverter 1	Offset voltage of inverter 2
$-\pi/6<\theta_i^*\leq\pi/6$	$-v_{as1}+0.5V_{DC1}$	$-v_{as2}+0.5V_{DC2}$
$\pi/6<\theta_i^*\leq\pi/2$	$-v_{cs1}+0.5V_{DC1}$	$-v_{cs2}+0.5V_{DC2}$
$\pi/2<\theta_i^*\leq 5\pi/6$	$-v_{bs1}+0.5V_{DC1}$	$-v_{bs2}+0.5V_{DC2}$
$5\pi/6<\theta_i^*, \theta_i^*\leq -5\pi/6$	$-v_{as1}+0.5V_{DC1}$	$-v_{as2}+0.5V_{DC2}$
$5\pi/6<\theta_i^*\leq -\pi/2$	$-v_{cs1}+0.5V_{DC1}$	$-v_{cs2}+0.5V_{DC2}$
$\pi/2<\theta_i^*\leq -\pi/6$	$-v_{bs1}+0.5V_{DC1}$	$-v_{bs2}+0.5V_{DC2}$

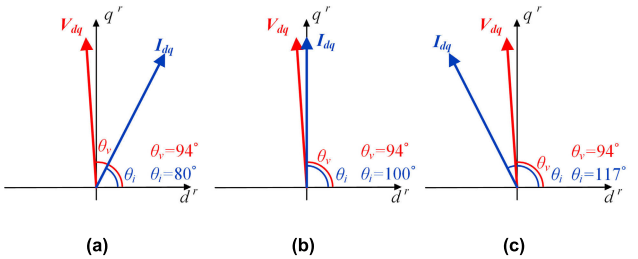

FIGURE 10. Current and reference voltage vector. (a) condition 1 (I_{de} = 0.5 A), (b) condition 2 (I_{de} = −0.5 A), and (c) condition 3 (I_{de} = −1.5 A).

inverters 1 and 2 was considered as 2 cases: same case and difference case. The simulation parameters are listed in Table 2. Simulations were performed using SVPWM, the conventional DPWM, and the proposed DPWM. To demonstrate the effectiveness of the proposed DPWM scheme, a synchronized d-axis current (I_{de}) was set to generate a phase difference between the reference voltage and the stator current.

When I_{de} of Condition 1 was set to 0.5 A, the phases of the voltage and current vectors were 94° and 80°, respectively, as shown in Fig 10(a). Further, when I_{de} of Condition 2 was set to −0.5 A, the phases of the voltage and current vectors were 94° and 99°, respectively, as shown in Fig. 10(b). Finally, when I_{de} of Condition 3 was set to −1.5 A, the phases of the voltage and current vectors were 94° and 117°, respectively, as shown in Fig. 10(c).

Even in case of the existence of phase difference, the proposed DPWM scheme occurred for ±30° based on the maximum stator current in the simulation results, as shown in Figs. 11 and 12. In Condition 1, Figs. 11(a) and 12(a) show the simulation results when applying the conventional

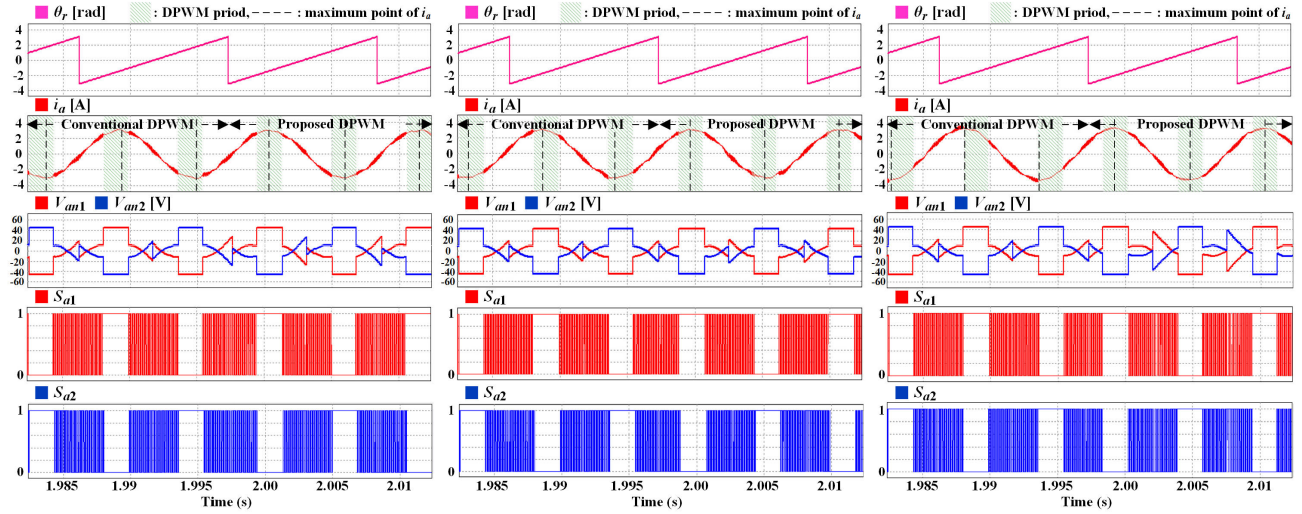

FIGURE 11. Simulation results under same case (V_{DC1} = 90 V and V_{DC2} = 90 V). (a) condition 1 (θ_i = 80° and θ_v = 94°), (b) condition 2 (θ_i = 100° and θ_v = 94°), and (c) condition 3 (θ_i = 117° and θ_v = 94°).

TABLE 2. Simulation and experiment parameters.

Parameters	Value
Stator resistance (R)	0.213 Ω
d-axis inductance (L_d)	1.60 mH
q-axis inductance (L_q)	2.18 mH
Permanent magnet flux (ϕ_f)	0.113 Wb
Number of poles (P)	12
Switching frequency(f_{sw})	10 kHz
Collector-emitter voltage (V_{ce})	0.5 V
Turn on time (T_{on})	1.2 μs
Turn off time (T_{off})	1.8 μs

TABLE 3. Total switch loss simulation of dual inverter with same magnitude of isolated DC source.

Condition	Modulation	Total	Inverter 1	Inverter 2
1 (I_{de} = 0.5 A)	SVPWM	22.48 W	11.24 W	11.24 W
	Conventional DPWM	14.32 W	7.16 W	7.16 W
	Proposed DPWM	14.12 W	7.06 W	7.06 W
2 (I_{de} = -0.5 A)	SVPWM	22.58 W	11.29 W	11.29 W
	Conventional DPWM	14.26 W	7.13 W	7.13 W
	Proposed DPWM	14.20 W	7.10 W	7.10 W
3 (I_{de} = -1.5 A)	SVPWM	25.08 W	12.54 W	12.54 W
	Conventional DPWM	16.52 W	8.26 W	8.26 W
	Proposed DPWM	15.76 W	7.88 W	7.88 W

and proposed DPWM schemes. Owing to the added I_{de} to verify the validity of the proposed method, the phase of the current was 6° behind the reference-voltage phase. When the conventional DPWM method was applied, switching occurred at the maximum current point owing to the phase difference. However, the proposed discontinuous modulation occurred at ±30°, based on the maximum stator current. In Condition 2, Figs. 11(b) and 12(b) show the simulation results when applying the conventional and proposed DPWM schemes. Because of I_{de}, the phase of the current was 6° ahead of the reference voltage phase, and the conventional DPWM method did not occur for ±30° based on the maximum point of the stator current. The proposed discontinuous modulation occurred at ±30°, based on the maximum stator current. In Condition 3, Figs. 11(c) and 12(c) show the simulation results when applying the conventional and proposed DPWM schemes. Because of I_{de}, the phase of the current was 24° ahead of the reference voltage phase, and the conventional DPWM method switched to the maximum point of the current. The proposed discontinuous modulation occurred at ±30° based on the maximum stator current. Thus, the proposed DPWM scheme occurred at the maximum point of the current.

In addition, the switching loss were compared to confirm the validity of the proposed scheme. The switching loss were calculated using PSIM, considering the collector-emitter voltage (V_{ce}), turn-on time (T_{on}), turn-off time (T_{off}), and switching frequency (f_{sw}). Even when the current angles were changed, the switching loss increased, as shown in Tables 3 and 4. When I_{de} was added to validate the proposed DPWM scheme, the output current increased. Consequently, the switching loss increased. When the output current was increased and changed, the proposed DPWM avoided

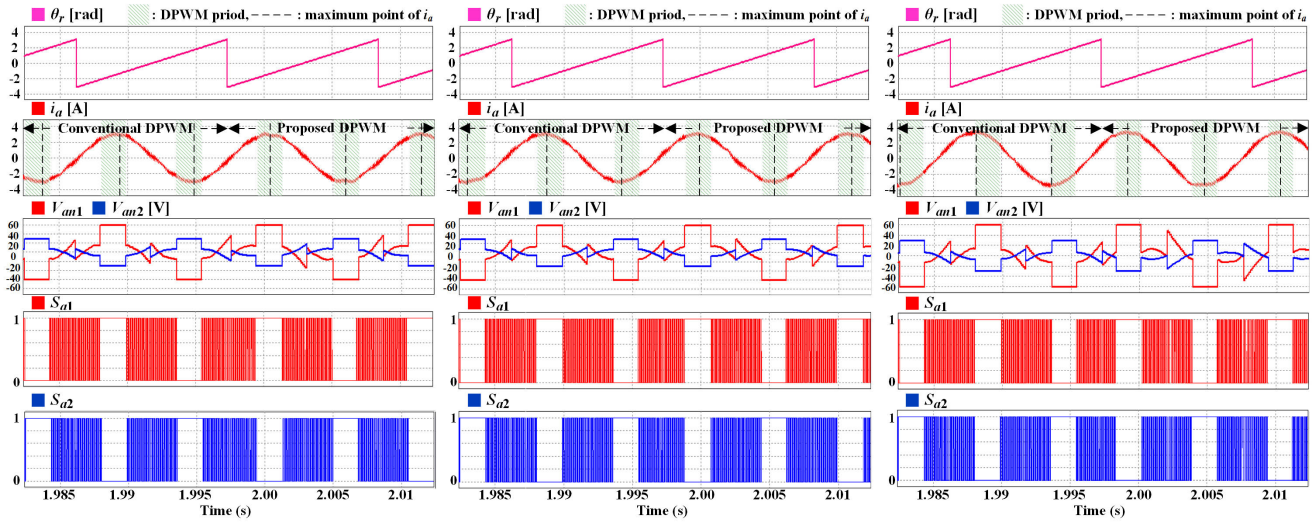

FIGURE 12. Simulation results under difference case (V_{DC1} = 120 V and V_{DC2} = 60 V). (a) condition 1 (θ_i = 80° and θ_v = 94°), (b) condition 2 (θ_i = 100° and θ_v = 94°), and (c) condition 3 (θ_i = 117° and θ_v = 94°).

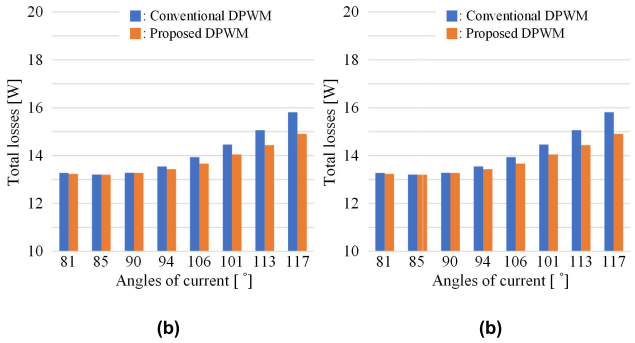

FIGURE 13. Total loss simulation (under V_{DC1} = 90 V and V_{DC2} = 90 V) for various angles of current. (a) inverter 1 and (b) inverter 2.

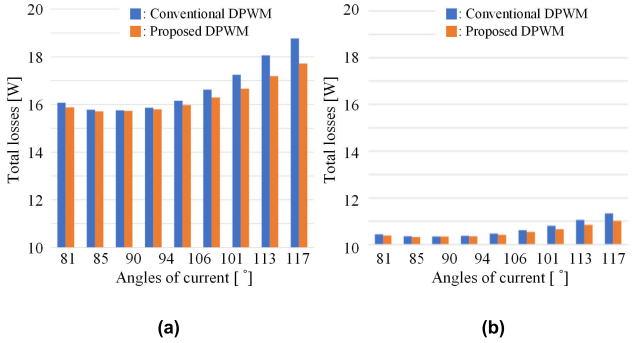

FIGURE 14. Total loss simulation (under V_{DC1} = 120 V and V_{DC2} = 60 V) for various angles of current. (a) inverter 1 and (b) inverter 2.

switching transition in the 30° range before and after the phase current peaks. This results in reduced the switching loss, as in Tables 3 and 4. When the input voltages of inverters 1 and 2 were the same, Fig. 13 shows the total switching loss of the conventional and proposed DPWM

TABLE 4. Total switch loss simulation of dual inverter with different magnitude of isolated DC source.

Condition	Modulation	Total	Inverter 1	Inverter 2
1 (I_{de} = 0.5 A)	SVPWM	22.48 W	14.04 W	8.44 W
	Conventional DPWM	14.33 W	8.61 W	5.72 W
	Proposed DPWM	14.11 W	8.46 W	5.65 W
2 (I_{de} = -0.5 A)	SVPWM	22.59 W	14.11 W	8.48 W
	Conventional DPWM	14.26 W	8.55 W	5.71 W
	Proposed DPWM	14.20 W	8.52 W	5.68 W
3 (I_{de} = -1.5 A)	SVPWM	25.08 W	15.67 W	9.41 W
	Conventional DPWM	16.52 W	9.96 W	6.56 W
	Proposed DPWM	15.76 W	9.45 W	6.31 W

methods according to the change in the phase of the stator current. Although the switching loss owing to the output current increased, the proposed method exhibited better switching loss reduction capability than the conventional DPWM method. When the input voltage of inverter 1 was twice as large as that of inverter 2, Fig. 14 shows the switching loss of the conventional and proposed DPWM methods according to the change in the current phase. Following analysis of switching loss, the efficiency according to the variation in the switching loss under each condition is shown in Tables 5 and 6. It can be seen from Tables 5 and 6 that the efficiency decreases with the increase in angles of current

TABLE 5. Total efficiency simulation of dual inverter with same magnitude of isolated DC source.

Condition	Modulation	Total	Inverter 1	Inverter 2
1 (I_{de} = 0.5 A)	SVPWM	92.10 %	92.10 %	92.10 %
	Conventional DPWM	94.97 %	94.97 %	94.97 %
	Proposed DPWM	95.05 %	95.05 %	95.05 %
2 (I_{de} = -0.5 A)	SVPWM	92.08 %	92.08 %	92.08 %
	Conventional DPWM	95.01 %	95.01 %	95.01 %
	Proposed DPWM	95.03 %	95.03 %	95.03 %
3 (I_{de} = -1.5 A)	SVPWM	91.21 %	91.21 %	91.21 %
	Conventional DPWM	94.22 %	94.22 %	94.22 %
	Proposed DPWM	94.49 %	94.49 %	94.49 %

TABLE 6. Total efficiency simulation of dual inverter with different magnitude of isolated DC source.

Condition	Modulation	Total	Inverter 1	Inverter 2
1 (I_{de} = 0.5 A)	SVPWM	92.11 %	92.59 %	91.13 %
	Conventional DPWM	94.97 %	95.46 %	93.99 %
	Proposed DPWM	95.06 %	95.54 %	94.07 %
2 (I_{de} = -0.5 A)	SVPWM	92.06 %	92.56 %	91.07 %
	Conventional DPWM	94.89 %	95.49 %	93.99 %
	Proposed DPWM	95.02 %	95.51 %	94.02 %
3 (I_{de} = -1.5 A)	SVPWM	91.19 %	91.74 %	90.09 %
	Conventional DPWM	94.21 %	94.76 %	93.11 %
	Proposed DPWM	94.48 %	95.03 %	93.38 %

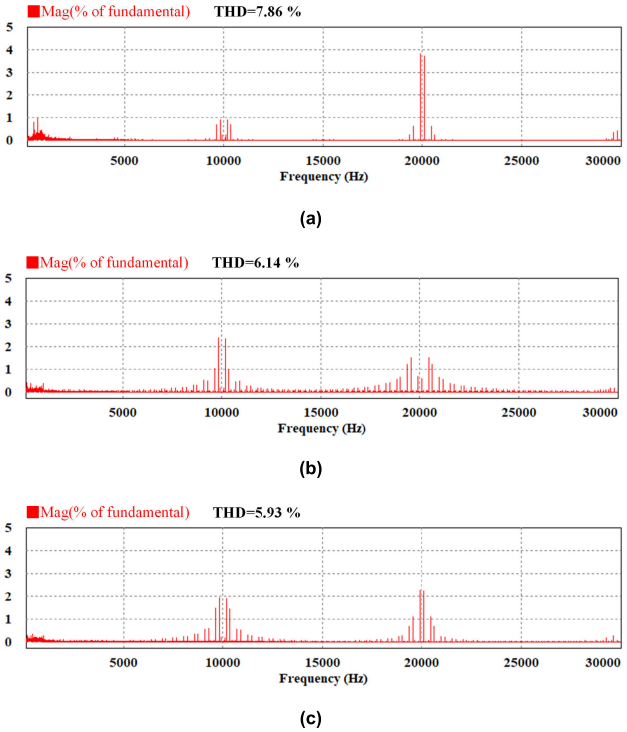

FIGURE 15. Total harmonic distortion simulation (under V_{DC1} = 120 V and V_{DC2} = 60 V). (a) SVPWM, (b) the conventional DPWM, and (c) the proposed DPWM.

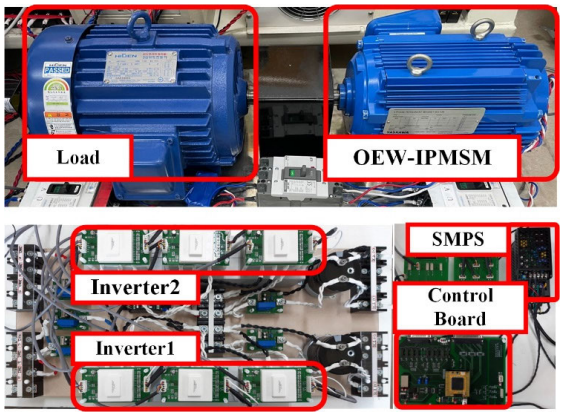

FIGURE 16. Experimental setup of OEW-IPMSM and the dual inverter.

by the tendency of the loss to increase according to angles of current.

The harmonic analysis of proposed DPWM method is represented in Fig. 15 and Table 7. Fig. 15 shows the results of performing fast fourier transform (FFT) analysis under conditions in which the effectiveness of the proposed method is noticeable among the conditions of the simulation. The FFT analysis in Fig. 15 was performed under Condition 3 of Table 4, and it can be confirmed that the proposed method has superior harmonic characteristics compared to the conventional methods. Table 7 shows the results of analyzing the total harmonic distortion (THD) of the stator current for Condition 3 of Table 3 and Table 4. The current THD under each condition reflects the tendency of the analysis of the previous switching loss and efficiency, and it was confirmed that the THD was reduced in the proposed method.

V. EXPERIMENTAL RESULTS

Fig. 16 shows the experimental setup of the dual inverter with an isolated DC source and OEW-IPMSM. The proposed algorithm was programmed on a digital signal processor (DSP) board with TMS320F28377S. The other parameters of the experimental setup are equal to those of the simulation, as shown in Table 2. The harmonic component of the current

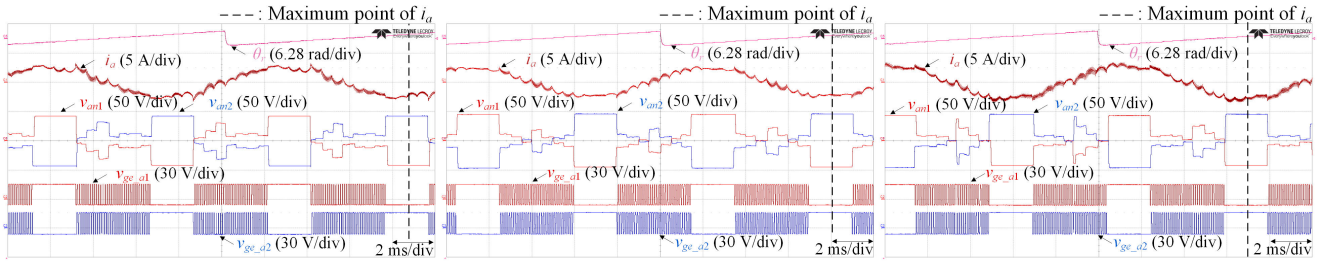

FIGURE 17. Experimental results of the proposed DPWM when V_{DC1} is 90 V and V_{DC2} is 90 V. (a) condition 1 ($\theta_i = 80°$ and $\theta_v = 94°$), (b) condition 2 ($\theta_i = 100°$ and $\theta_v = 94°$), and (c) condition 3 ($\theta_i = 117°$ and $\theta_v = 94°$).

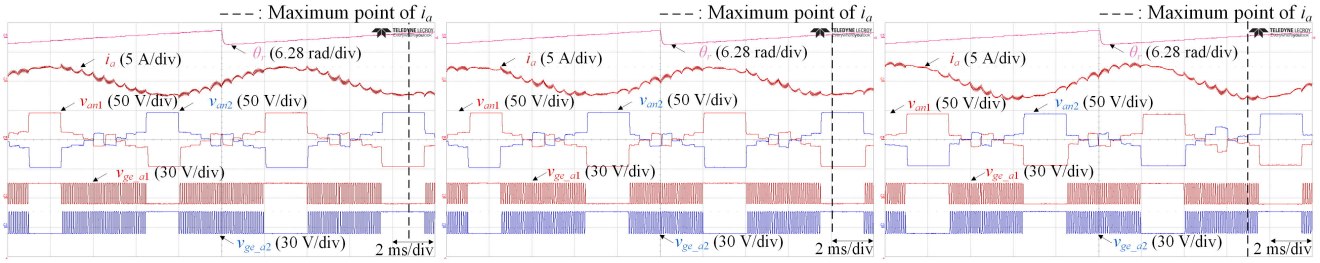

FIGURE 18. Experimental results of the conventional DPWM when V_{DC1} is 90 V and V_{DC2} is 90 V. (a) condition 1 ($\theta_i = 80°$ and $\theta_v = 94°$), (b) condition 2 ($\theta_i = 100°$ and $\theta_v = 94°$), and (c) condition 3 ($\theta_i = 117°$ and $\theta_v = 94°$).

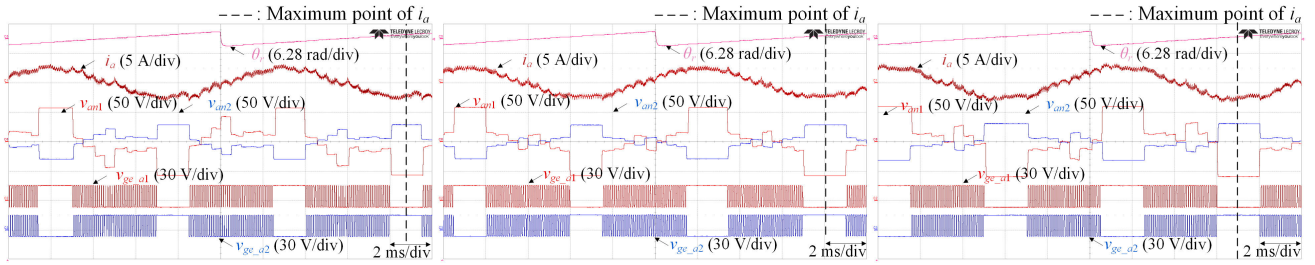

FIGURE 19. Experimental results of the proposed DPWM when V_{DC1} is 120 V and V_{DC2} is 60 V. (a) condition 1 ($\theta_i = 80°$ and $\theta_v = 94°$), (b) condition 2 ($\theta_i = 100°$ and $\theta_v = 94°$), and (c) condition 3 ($\theta_i = 117°$ and $\theta_v = 94°$).

tends to be larger in the experimental results compared to simulation results. These results are affected by various conditions. The harmonic component of the current increases when the inductance component of the motor winding is small, such as the motor used in this experiment. Compared to the simulation, the main reason for the increase in the harmonics of the output current in the experiment is the low inductance component of the stator winding. In addition, dead time and rising/falling time of the switches also cause differences between simulation and experimental results. d-axis stator current I_{de} was added to validate the proposed DPWM method, and conditions 1, 2, and 3 were divided according to the magnitude of I_{de}. For the experiment, I_{de} of condition 1, 2 and 3 were set to 0.5, −0.5, and −1.5 A, respectively.

Figs. 17 and 18 show the experimental results for the applications of the conventional DPWM and the proposed DPWM scheme when the input voltages of inverters 1 and 2 were the same as 90 V. The reference voltages of inverters 1 and 2 had the same command voltage with a difference of only 180°. As shown in Fig. 17, the proposed discontinuous modulation occurred for ±30° based on the maximum stator current under conditions 1 ($\theta_i = 80°$ and $\theta_v = 94°$), 2 ($\theta_i = 100°$ and $\theta_v = 94°$), and 3 ($\theta_i = 17°$ and $\theta_v = 94°$). Fig. 18 shows the experimental results obtained by applying the conventional DPWM scheme. Discontinuous modulation

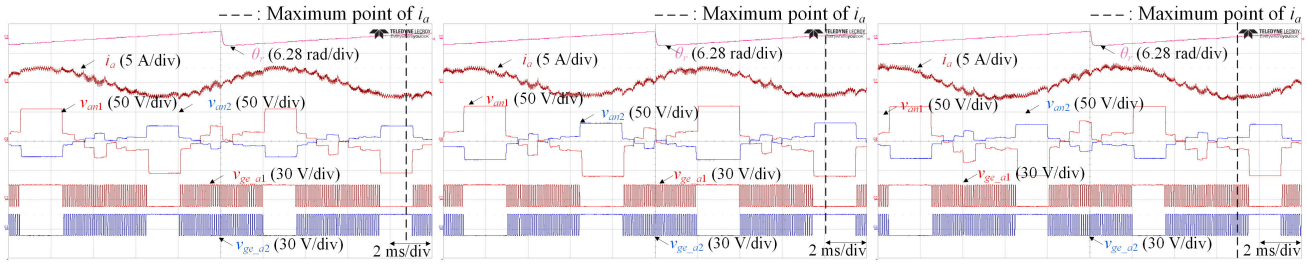

FIGURE 20. Experimental results of the conventional DPWM when V_{DC1} is 120 V and V_{DC2} is 60 V. (a) condition 1 ($\theta_i = 80°$ and $\theta_v = 94°$), (b) condition 2 ($\theta_i = 100°$ and $\theta_v = 94°$), and (c) condition 3 ($\theta_i = 117°$ and $\theta_v = 94°$).

TABLE 7. Total harmonic distortion simulation of dual inverter with isolated DC source.

Condition	Modulation	THD
1 (I_{de} =-1.5 A, V_{DC1}=90 V, V_{DC2}=90 V)	SVPWM	6.78 %
	Conventional DPWM	4.56 %
	Proposed DPWM	4.32 %
2 (I_{de} =-1.5 A, V_{DC1}=120 V, V_{DC2}=60 V)	SVPWM	7.86 %
	Conventional DPWM	6.14 %
	Proposed DPWM	5.93 %

did not occur for ±30°, based on the maximum stator current under conditions 1, 2, and 3.

Figs. 19 and 20 show the experimental results when the input voltages of inverters 1 and 2 were different. So, the reference voltages of inverters 1 and 2 had the different command voltage with a difference of only 180° The conventional modulation did not occur for ±30°, based on the maximum stator current under conditions 1, 2, and 3. The proposed discontinuous modulation occurred at ±30° based on the maximum current under conditions 1, 2, and 3. The switching loss reduction ability of proposed method was verified when V_{DC1} and V_{DC2} were different and same.

VI. CONCLUSION

This paper proposed an advanced DPWM scheme with switching loss reduction for a dual inverter with an isolated DC source. When the conventional DPWM method was applied, switching occurred at the maximum current point owing to the phase difference between the reference voltage and current. The proposed DPWM scheme used additional calculations of the current phase to reduce switching loss when the phases of the reference voltage and current were different. The proposed DPWM scheme exhibited a higher efficiency than the conventional DPWM scheme because the it was not switched at ±30° of the maximum point of the current. The efficiency gains from this loss reduction are maximized in high-power applications, so the proposed algorithm is effective in improving the efficiency of high-power applications. Moreover, based on the simulation and experimental results, the validity of the proposed DPWM scheme was verified.

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HYUNG-WOO LEE (Student Member, IEEE) received the B.S. and M.S. degrees in electrical and computer engineering from Ajou University, Suwon, South Korea, in 2020 and 2022, respectively, where she is currently pursuing the Ph.D. degree in electrical and computer engineering. Her research interests include dual inverters, electric machine drives, and power conversion.

SUNG-JIN JANG (Student Member, IEEE) received the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2019. He is currently pursuing the M.S. degree in electrical and computer engineering with Ajou University, Suwon, South Korea. His research interests include electric machine drives and dual inverters.

KYO-BEUM LEE (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from Ajou University, Suwon, South Korea, in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from Korea University, Seoul, South Korea, in 2003.

From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Jeonbuk National University, Jeonju, South Korea. In 2007, he joined the Department of Electrical and Computer Engineering, Ajou University. His research interests include electric machine drives, renewable power generation, and electric vehicle applications. He is currently an Editor-in-Chief of the *Journal of Power Electronics*. He is also an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS.