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RESEARCH ARTICLE

Design and Implementation of a Single Switch High Gain Boost Topology: Structure, Ripple Control and ZCS

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ABSTRACT The need for high gain DC-DC converters has lately increased in tandem with the utilization of renewable energy supplies. Particularly appealing are high gain converters that do not require the inclusion of extra power switches and/or other passive elements to the system. As a result, this study proposes a non-isolated single switch converter with ultra-high voltage gain (UHG) that is appropriate for most renewable energy conversion systems, like solar installations. With only a single MOSFET working within a suitable duty cycle region, the proposed converter provides significant voltage gain and around 95% efficiency. Moreover, the MOSFET in this UHG converter is turned on in zero current switching (ZCS) mode, resolving the diode recovery issue. The recommended UHG converter's working modes, steady-state parametric study, circuit variables like voltage stress on switching devices, and converter gain are all thoroughly explained. Comparisons have been done with comparable topologies presented in the literature, and lastly, experimental results depending on 200W (20V input, 320V output voltage) are given to validate the operation of the proposed UHG design.

INDEX TERMS Ultra high gain converter, DC-DC topology, three-windings coupled-inductor, soft switching, zero current switching, high gain step-up converter.

I. INTRODUCTION

In past years, there has been a significant growth in energy demand and usage. This expansion is projected to continue over the next many years (at least). Conventional fossil-fueled sources of energy are linked to two fundamental issues: finite resources and greenhouse gas emissions. As a result of these worries, companies have invested in environmentally acceptable energy resources such as photovoltaic (PV) devices [1], [2], hydrogen-based fuel cells [3], [4], and wind energy technologies.

In the majority of these novel energy methods, the produced power is either direct current (DC) or there is an intermediary DC connection in the energy conversion system [5]. Solar panels, as a standard strategy for PV systems, can be arranged in parallel or in series with one another and operate as the input for DC-DC topologies, the primary tasks of those are to control and step up the DC voltage on the DC-link for DC-AC conversion. In order to control the current rating of the switching devices and utilize the suitable modulation coefficients, the DC-link voltage of a DC-AC inverter must not be less than a particular specified value. In past research, several designs were created to increase the voltage level of PV panels to an acceptable amount for the DC-link voltage.

Combining coupled inductor (CI) and passive and active clamped approaches, high boosting capability can be accomplished [6], [18]. Despite these, the cost and dimensions of this converter, due to its two output DC-link capacitors and CI's enormous core size, do not appear to be appropriate for the entire power rating.

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Further approaches for achieving high voltage gain in switching mode converters include the use of a switched capacitor or a switched inductor [7], [15]. However, due to the intrinsic characteristic of these designs [7], [14], a high duty cycle value is required for active switch(s) to accomplish high voltage gain in several high gain step-up converters, that might raise switching losses. The active switched-inductor with a passive switched-capacitor based converter described in [24] increased voltage gain via a cascaded passive switched-capacitor network. But, the inductance in the high-side LC filter, that is utilized to minimize the discharge current spikes of capacitors, will result in a bulkier circuit based on the calculated inductance. The voltage gain of an active switched inductor converter is improved in [25] by using an extensive active-passive inductor unit. By expanding the amount of active-passive inductance cells, voltage stress on switches is diminished and critical inductance is lowered, but the semiconductor device drive circuit becomes more complicated due to the extra switches. Reference [8] introduces a unique resonant design with a double voltage arrangement and two sets of secondary windings to produce soft switching operation. The disadvantage of this converter is that it has a high number of active switching devices as compared to single-switch designs.

Another typical approach for improving voltage gain in DC-DC converters is to change the turn-ratio of specific magnetic elements, such as a transformer or CI [9], [12], [13], [14], [15]. In particular applications when isolation is not required, the CI is used by varying the turns ratio, that can yield significant voltage gain. Compared with an isolation transformer, the coupled inductor has a simple and efficient structure, but its use is restricted to applications that do not require electrical isolation [28], [29]. Considering its adaptability, the high voltage gain method has significant drawbacks, the majority of which are related to CI leakage [10], [11]. Using multiplier cells in a boost converter is another way to enhance voltage gain [16], [18], [20], [24]. The turns ratio of the CI is the most critical factor in increasing voltage gain and reducing voltage stress over the switches. The DC-DC design in [15] operates well in terms of voltage gain and voltage stress. But at the other hand, the current ripple is significantly larger on the input-voltage side. As a result, the power source's lifetime may be diminished, as well as its overall efficiency.

In [17], the researchers suggested a novel DC-DC converter design depending on 3 CI with high voltage gain. While the use of inexpensive elements with CI is a benefit of this design, the voltage gain is too low to be employed for a DC-DC-AC solar systems with a specific solar panel. Another three-winding CI-based converter has been suggested in [13], but it suffers from reverse-recovery issues due to their diodes. Reference [22] proposes a new configuration for a step-up DC–DC converter with a high voltage transfer gain and an appropriate duty cycle. However, due to the use of resistance in the power input path, the ripple of input current is higher than that of other step-up topologies, such as those described

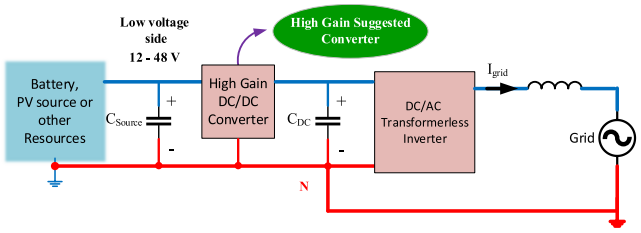

FIGURE 1. An example application of proposed converter.

in [19], [20], and [21], and the efficiency can be reduced. In addition, the diode voltage stress in the multiplier cell of this converter is equal to the output diode voltage, which can increase the overall price of the converter.

A non-isolated ultra-high gain (UHG) DC-DC configuration with three winding CI and a single power MOSFET switch is presented in this work. The main features of the proposed converter are:

- Very low Input current ripple.
- Low voltage Stress on semiconductors.
- High and appropriate voltage gain of the converter.
- Soft switching operation for main switch and diodes.
- Appropriate total efficiency of converter.

Fig. 1 shows an example application of proposed converter in a grid integration of energy resource. It should be noted that in grounded PV systems, the step-up converter should provide a shared ground between the PV ground and the grid neutral line to prevent common mode current. That's why there is a common input to output ground in the proposed topology.

The proposed converter can be used in PV applications under normal or partial shading conditions as well as other applications such as Fuel cells, DC microgrid and HID lamp ballast. For example, when partial shading occurs on a solar system, the maximum power point of that system may be formed at low voltage levels. Therefore, it is necessary to use a high gain step-up converter.

This work extends the proposed UHG converter topology which was previously presented at a conference [24], where more detail analysis has been done on device operation, evaluation of the current stress on semiconductor devices have been done, comparative study is extended, the component design procedure of the proposed converter has been explained and followed by numerical representation in the experimental setup development. Moreover, more detail efficiency analysis and losses evaluation have been performed to compare the proposed converter efficiency with most recent similar topologies available in the literature.

It is important to note that adding voltage gain using a large number of inductors will not happen easily, and significant challenges such as voltage stress on the switch(es) or diodes, Soft/Hard switching operation, losses of windings should be considered.

The remaining of this paper is organized as follows: Section II discusses circuit designing and operational analysis in the context of continuous conduction mode (CCM).

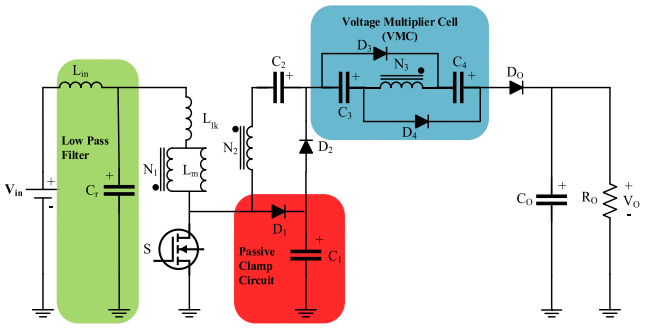

FIGURE 2. Suggested UHG DC-DC topology.

Section III obtains some critical topology characteristics (including voltage gain and voltage stress over the switching devices). There is the component design and efficiency analysis in Section IV. Section V includes a comparison between comparable high gain designs available in the literature. Lastly, Section VI discusses the paper's overall accomplishments depending on the experimental setup. While the closed-loop control can be achieved for different purposes (e.g. output voltage regulation using a conventional PI), this research concentrates on the design of the high gain boost converter along with the soft switching circuit assignment as well as low-ripple input current regulation.

II. SUGGESTED TOPOLOGY AND OPERATION PRINCIPLES

The suggested design comprises a voltage multiplier cell (VMC) and a CI to improve converter boosting capabilities. Figure 2 depicts the suggested UHG DC-DC converter associated power circuit. A passive clamping circuit consists of capacitor C1 and diode D1 is employed to relieve the voltage spike caused by the leakage inductor on the main MOSFET and recycle the leakage inductance energy. To improve the converter voltage gain, at the tertiary side of the CI, capacitors C3 and C4, and diodes D3 and D4 work as a VMC. The LC low-pass filter at the input makes the input current continuous with low ripple, which makes the proposed converter suitable for use in renewable sources such as solar cells.

The condition of switching devices in one entire switching period for the proposed UHG DC-DC converter is depicted in Fig. 3, wherein a switching period is split into six subintervals (mode 1 - mode 6). Figure 4 depicts the primary waveforms of currents and voltages during a single switching period. The following concepts are taken into account when performing the steady-state analysis:

- The switch and other semiconductors are ideal.
- CI is considered ideal with the turns-ratio of $n_2 = N_2/N_1$, $n_3 = N_3/N_1$, magnetizing inductor (L_m) and leakage inductor (L_{lk}).
- The grayed-out components are disabled.
- The suggested topology (Fig.2) works in (CCM).
- D denotes duty cycle of the switch and D' is equal to 1-D.

The following are the suggested design operating principles:

Mode 1: At the commencement of the first state, the MOSFET starts to conduct, diodes $D_1 - D_4$ are blocked, and only D_O is conducting. As the leakage inductance current, L_{lk}, slowly rises during this small time, the currents on the different sides of the CI (L_{N2} and L_{N3}) reduce gradually. According to Fig. 3(a), the existence of Lin and a leaky inductor causes MOSFET current to progressively rise and turning on in a ZCS condition. Whenever the leakage current reaches the magnetizing current, diode D_O switches off and diode D_2 turns on.

Mode 2: In Fig. 3(b), the MOSFET remains operating in the second mode, and diodes D_3, D_4, and D_O are blocked, whereas diode D_2 is turned on with a ZCS condition. The input, leakage, and magnetizing inductors are charged by the DC input voltage source, increasing their current (I_{Lin}, I_{Lm}, and I_{Lk}). The diode D_2 discharges the capacitor C_1 and charges the capacitor C_2.

These formulae can be determined by applying Kirchhoff's Voltage Law (KVL) to the design in this mode:

$$V_{Lm}^{D} = \left[\frac{L_m}{L_m + L_{lk}}\right] V_{Cr} = kV_{Cr} \quad (1)$$

$$V_{L_{lk}}^{D} = \left[\frac{L_{lk}}{L_m + L_{lk}}\right] V_{Cr} = (1-k)V_{Cr} \quad (2)$$

$$V_{Lin}^{D} + V_{Lm}^{D} + V_{L_{lk}}^{D} = V_{in} \quad (3)$$

$$V_{Lin}^{D} + V_{Cr} = V_{in} \quad (4)$$

$$V_{N2}^{D} = V_{C2} - V_{C1} = n_2 V_{Lm}^{D} = n_2 k V_{Cr} \quad (5)$$

k is the coupling factor and $V_{Lm}^{D}.V_{L_{lk}}^{D}.V_{Lin}^{D}$ are voltage of magnetizing, leakage and input inductances while MOSFET is on respectively. $V_{Cr}.V_{C2}.V_{C1}$ are voltage of capacitors C_r, C_2 and C_1 respectively, while MOSFET is turned on. This interval ends when the diodes D_3 and D_4 turn on and amplitude of I_{LN3} increases.

Mode 3: In this state, the MOSFET stays switched on, and diodes D_2, D_3 and D_4 conduct while diodes D_1 and D_O are turned off. Through the diode D_2, the capacitor C_1 is discharged, while the capacitors C_3, C_4, and C_2 are charged. Furthermore, because of the inverted voltage on windings N_3 and N_2, the currents on windings N_2 and N_3 (I_{N2} and I_{N3}) are gradually decreasing. Moreover, the voltages of capacitors C_3 and C_4 are determined in this situation using (6):

$$V_{N3}^{D} = V_{C3} = V_{C4} = n_3 V_{Lm}^{D} = n_3 k V_{Cr} \quad (6)$$

where $\boldsymbol{V_{N3}^{D}}$ is the voltage of tertiary windings whenever the MOSFET is on.

Mode 4: This short interval transition starts whenever currents of windings N_2 and N_3 is near zero and all diodes are blocked. As it can be found from Fig. 4, while the switch is completely off, this time interval ends.

Mode 5: In this situation, the power switch is switched off, and the input voltage charges the windings of N2 and N3. The energy from the leaking inductor is recycled to the capacitor C1, which is supplied through the diode D1. For

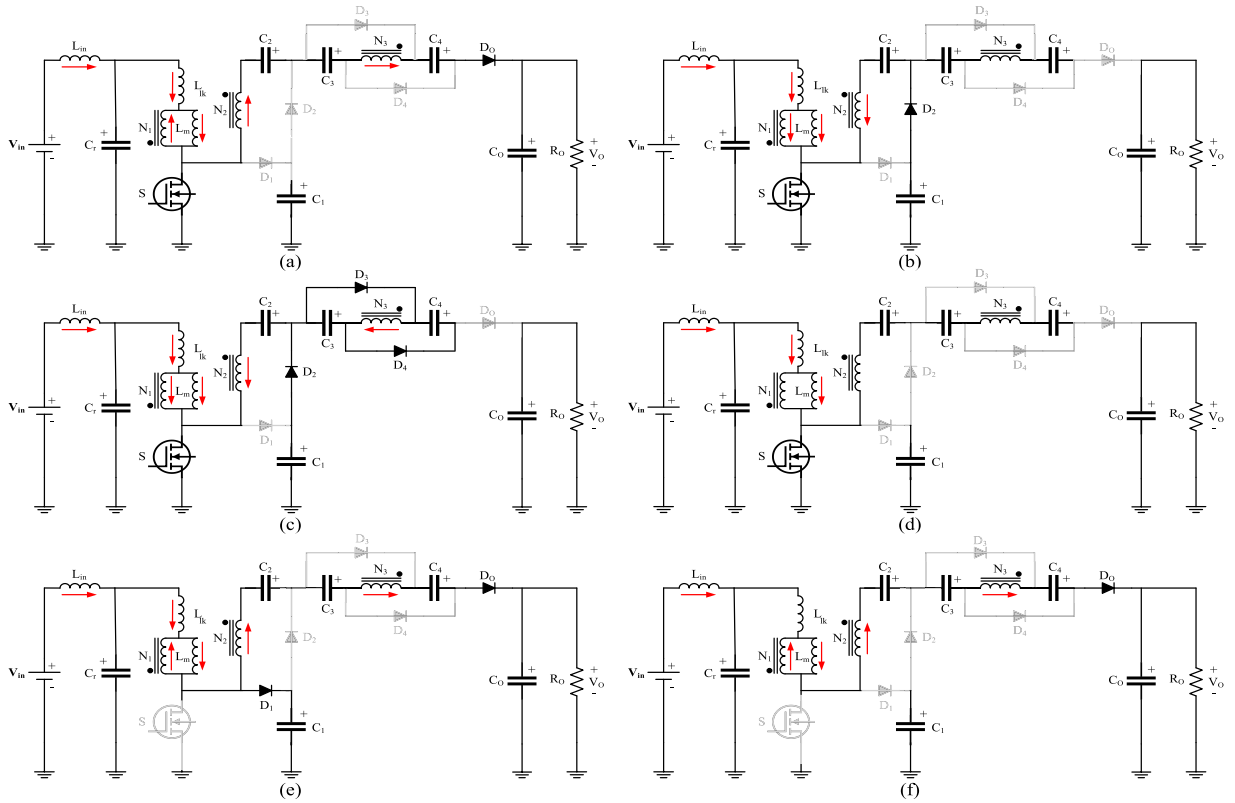

FIGURE 3. Current paths in the suggested UHG topology, (a) circuit status at Mode 1, (b) circuit status at Mode 2, (c) circuit status at Mode 3, (d) circuit status at Mode 4, (e) circuit status at Mode 5, (f) circuit status at Mode 6.

now, capacitors C2, C3, and C4 are discharged via the output diode. The following formula can be obtained by considering KVL in the loop of Fig. 3(e):

$$V_{Lin}^{D'} + V_{Lm}^{D'} + V_{Llk}^{D'} = V_{in} - V_{C1} \tag{7}$$

$$V_{Lm}^{D'} = k(V_{Cr} - V_{C1}) \tag{8}$$

$$V_{N2}^{D'} = n_2 V_{Lm}^{D'} \tag{9}$$

$$V_{N3}^{D'} = n_3 V_{Lm}^{D'} \tag{10}$$

$$V_{C1} - V_{N2}^{D'} + V_{C2} + V_{C3} - V_{N3}^{D'} + V_{C4} = V_O \tag{11}$$

where $\boldsymbol{V_{Lm}^{D'}}.\boldsymbol{V_{Llk}^{D'}}.\boldsymbol{V_{Lin}^{D'}}$ are voltage of magnetizing, leakage and input inductances while the MOSFET is off respectively.

Mode 6: The power switch is continuously blocked in this situation, and this state starts whenever the voltage of C_1 approaches its ultimate amount and D_1 goes off. As in the preceding state, capacitors C_2, C_3 and C_4 are discharged through the output diode in this mode (D_O). Whenever the MOSFET is switched on, Mode 6 comes to an end, and the next cycle begins.

III. STEADY-STATE ANALYSIS OF THE SUGGESTED DESIGN

A. VOLTAGE GAIN (M_{CCM}) CALCULATION

By utilizing the volt-second equilibrium axiom for both input inductor and magnetizing inductance, using (3) and (7), V_{c1} can be related to input voltage by:

$$V_{C1} = \frac{V_{in}}{D'} \tag{12}$$

According to (12) and by utilizing the volt-second equilibrium axiom for magnetizing inductance, using (1) and (8), V_{Cr} is obtained by:

$$V_{Cr} = D' V_{C1} = V_{in} \tag{13}$$

By substituting (12) and (13) into (5) the V_{C2} is obtained:

$$V_{C2} = n_2 k V_{in} + \frac{V_{in}}{D'} \tag{14}$$

By substituting (12) and (13) into (8) the $V_{Lm}^{D'}$ relation to input voltage can be obtained by:

$$V_{Lm}^{D'} = k(V_{Cr} - V_{C1}) = -\frac{D}{D'} V_{in} \tag{15}$$

By substituting (6), (9), (10), (12), (13), (14), and (15) into (11) the nominal M_{CCM} of proposed UHG topology is obtained:

$$\frac{V_o}{V_{in}} = \frac{1}{D'}\left(2 + n_2\left(D + kD'\right) + n_3\left(D + 2kD'\right)\right) \tag{16}$$

If the leakage inductance of the CI is not considered, the coupling factor k is 1, and the ideal M_{CCM} of the proposed topology is as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1}{D'}(2 + n_2 + n_3\left(D + 2D'\right)) \tag{17}$$

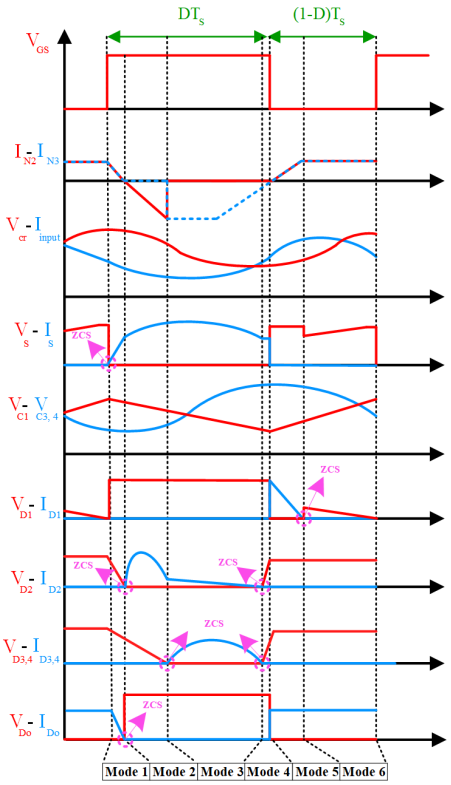

FIGURE 4. Essential waveforms of the suggested topology in CCM operation.

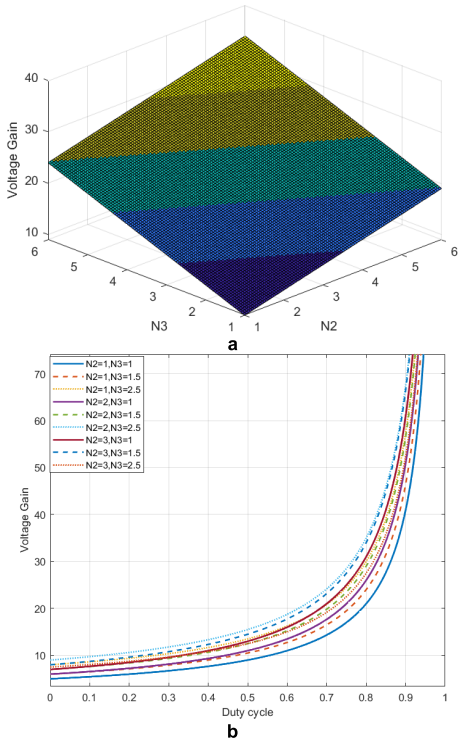

FIGURE 5. a) Voltage gain in different secondary and tertiary turns ratio (D = 0.5), b) M_{CCM} against duty cycle under various CI turns ratios ($N_1 = 1$).

Figure 5(a) shows the voltage gain of the converter in the different secondary and tertiary turns ratio when duty cycle is 0.5. As it is clear in this picture, in addition to the high turns ratio, in the lower turns ratio, using the suggested converter, a suitable voltage gain can be obtained. The suggested topology theoretical voltage gain in CCM, M_{CCM}, versus MOSFET duty cycle, D, for different CI, n_2 and n_3 turn ratios is illustrated in Fig. 5. (b). It can be shown that the CI turns ratios, N_2 and N_3, can be determined and changed to provide very high voltage gain without ever using and operating at an extremely high duty cycle.

Due to the significant increase in power switch conduction losses and the need for a larger heatsink at higher duty cycles, the appropriate duty cycle value of the MOSFET for this topology is less than 0.75, below the knee point of the curves shown in Fig. 5(b)

B. EVALUATION OF VOLTAGE STRESS ON SEMICONDUCTOR DEVICES

The voltage stress of switch and other semiconductors based on the topology operation are calculated as follows:

$$V_S = V_{D1} = V_{C1} = \frac{V_{in}}{D'} \tag{18}$$

$$V_{D2} = (n_2 + 1)\frac{V_{in}}{D'} \tag{19}$$

$$V_{D3} = V_{D4} = n_3\frac{V_{in}}{D'} \tag{20}$$

$$V_{DO} = (1 + n_2 + n_3)\frac{V_{in}}{D'} \tag{21}$$

where, V_s is voltage stress on MOSFET and V_{D1}, V_{D2}, V_{D3} and V_{DO} are voltage stress of Diodes D_1, D_2, D_3 and D_O respectively.

C. EVALUATION OF CURRENT STRESS ON SEMICONDUCTOR DEVICES

By using ampere-second balance law on all capacitors, C_1, C_1-C_4 and C_O, the average currents of all diodes are equal to the output current, I_O. Following the same procedure presented in [22], the peak current of the switch and diodes are calculated as follows:

$$I_{D1} = \frac{1}{D'}(1 + n_2 + n_3\left(D + 2D'\right))I_O \tag{22}$$

$$I_{D2} = I_{D3} = I_{D4} = 2\frac{I_O}{D} \tag{23}$$

$$I_{DO} = \frac{I_O}{D'} \tag{24}$$

$$I_S = \frac{1}{DD'}(1 + D(1 + n_2 + n_3\left(D + 2D'\right)))I_O + \frac{1}{2}\frac{V_{in}D}{L_m f_s} \tag{25}$$

Voltage and current stresses are important information for semiconductor devices selection.

Figures 6(a-c) show the normalized voltage stress on the diodes D_2, D_3 and D_O respectively when duty cycle is 0.5. Furthermore, the normalized current stress through the Diode

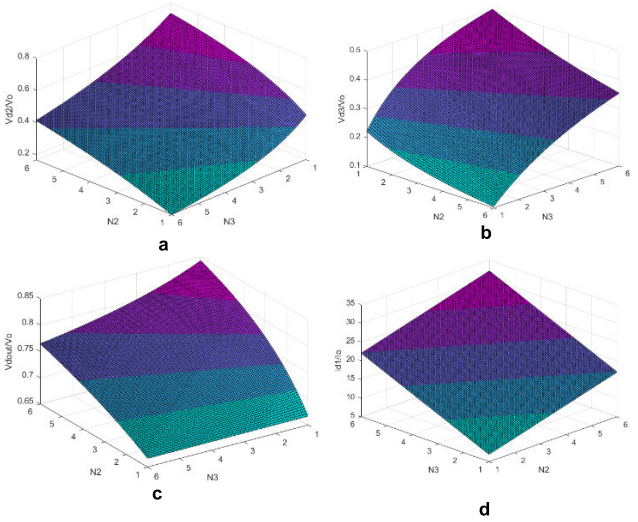

FIGURE 6. Normalized Voltage stress on: a)D_2, b)D_3, c)D_o in different secondary and tertiary turns ratio(D = 0.5, N_1 = 1), d)Normalized current stress of D_1.

D_1 is depicted in Fig. 6(d). By using these figures, the optimal values of turns ratio can be selected.

D. VOLTAGE AND CURRENT STRESS OF PASSIVE COMPONENTS

The voltage stress of passive components can be obtained using equations (6-10), (12-14), (17) as follows:

$$V_{C1} = \frac{V_{in}}{D'} \tag{26}$$

$$V_{C2} = (n_2 + \frac{1}{D'})V_{in} \tag{27}$$

$$V_{C3} = V_{C4} = n_3 V_{in} \tag{28}$$

$$V_{Co} = \frac{V_{in}}{D'}(2 + n_2 + n_3\left(D + 2D'\right)) \tag{29}$$

$$V_{Lm} = (1 - \frac{1}{D'})V_{in} \tag{30}$$

$$V_{N2} = (1 - \frac{1}{D'})V_{in}n_2 \tag{31}$$

$$V_{N3} = (1 - \frac{1}{D'})V_{in}n_3 \tag{32}$$

Furthermore, the current stress of passive components can be obtained using operation modes and by assuming efficiency around to %100 for nominal output power. Besides that, the RMS current of C_r is very low.

$$RMS(i_{C1} = i_{C2} = i_{C3} = i_{C4}) \sim i_o \tag{33}$$

$$i_{Lin,rms} \sim \frac{1}{D'}(2 + n_2 + n_3\left(D + 2D'\right))i_o \tag{34}$$

$$i_{lm,rms} \sim \frac{1}{DD'}(1 + D(1 + n_2 + n_3\left(D + 2D'\right)))I_O \tag{35}$$

IV. COMPONENT DESIGN

A. INPUT FILTER DESIGN (LIN)

By assuming the acceptable ripple on input inductance (ΔI_{in}), and knowing the switching frequency of the active switch (f_s), using (33), the size of input inductor can be obtained from the following equation:

$$L_{Lin} \geq \frac{V_{in}D}{\Delta I_{in} f_s} \tag{36}$$

B. CAPACITORS DESIGN

The following equation is used to calculate the size of capacitors except resonance capacitor.

$$C \geq \frac{P_O}{V_C \Delta V_C f_s} \tag{37}$$

C. COUPLED INDUCTOR MAGNETIZING INDUCTANCE DESIGN (L_m)

By assuming acceptable current ripple on coupled inductor magnetizing inductance (ΔI_{Lm}), the amount of the magnetic inductance can be obtained from the following equation:

$$L_m \geq \frac{V_{in}D}{\Delta I_{Lm} f_s} \tag{38}$$

Fig. 7 shows the boundary Region between DCM and CCM for different output power of suggested converter. Using $L_m = 140\ \mu$H the suggested design operates for most output powers in the CCM.

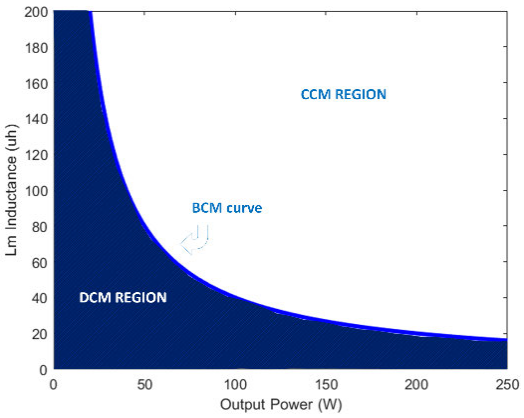

FIGURE 7. DCM and CCM region for different output power.

The average current of magnetic inductance (L_m) is determined as follow:

$$I_{Lm} = I_{in} = \frac{1}{D'}(2 + n_2 + n_3\left(D + 2D'\right))I_O \tag{39}$$

1) DESIGN OF RESONANCE COMPONENTS

To calculate the amount of C_r (resonance capacitor) and coupled inductor leakage inductance (L_{lk}), according to [22], these components are designed to operate in boundary-resonance or blow-resonance mode to reduce output diode switching losses and improve its reverse recovery problems. Also the amount of L_{lk} depends on how coupled inductor winding is wrapped and thus the following equation can be used for design purpose:

$$\pi\sqrt{L_{lk}C_r} \leq DT_s \rightarrow C_r \leq \frac{D^2}{\pi^2 L_{lk} f_s^2} \tag{40}$$

TABLE 1. Comparison of a proposed UHG DC-DC converter with some other high step-up topologies.

Converters	Ref [12], 2019	Ref [13], 2015	Ref [14], 2019	Ref [15], 2017	Ref [16], 2016	Ref [17], 2019	Ref [18], 2020	Ref [19], 2018	Ref [20], 2016	Ref [21], 2018	Proposed Converter
N_C	4	4	4	3	3	3	4	5	4	3	6
N_S	1	1	2	4	1	1	1	4	2	1	1
N_D	4	4	2	0	2	3	3	5	4	3	5
N_{IND}	1CI(3W)	1CI(3W)	1+1CI(2W)	1CI(2W)	1+1CI(2W)	1CI(3W)	1+1CI(2W)	2CI(2W)	1CI(3W)	1CI(3W)	1+1CI(3W)
Common input to output Ground	✓	✓	✓	✓	✓	✓	✓	✓	×	✓	✓
Efficiency & Voltage ratio	96% At(400W) 40V to 380V	95.2% At(200W) 90V to 400V	95.8% At(300W) 48V to 400V	94.8% At(200W) 25V to 200V	93.1% At(200W) 35V to 380V	94.2% At(200W) 20V to 300V	94.6% At(250W) 20V to 143V	95.7% At(150W) 72V to 400V	94.4% At(200W) 30-50V to	97.4% At(400W) 20V to 400V	95.8% At(200W) 17-20V to 320V
Input current ripple	Low	High	Very low	High	Very low	High	Low	High	High	High	Very low
Voltage Stress on output diode	$\frac{(n_3)V_o}{(1-D)(n_2-1)}$	$\frac{(n_2+1)V_o}{n_3+n_2+2-(1+n_2)D}$	V_o	$\frac{n_2}{2n_2-1}Vo$	V_o	$\frac{(n_2+n_3)V_o}{n_2+n_3+D(n_3-1)}$	$\frac{n_2Vo}{2n_2-1}$	V_o	$\frac{n_3.Vo}{n_3+1+D}$	$\frac{n_2+n_3}{2n_2+n_3-1}Vo$	$\frac{(n_2+n_3+1)V_o}{n_2+n_3(2-D)+2}$
Voltage Stress on main switch	$\frac{(n_2-1)V_o}{n_3+2n_2-1}$	$\frac{V_o}{n_3+n_2+2-(1+n_2)D}$	$\frac{V_o}{n_2}$	$2Vo$	$\frac{V_o}{n_2+1}$	$\frac{(n_3-1)V_o}{n_2+n_3+D(n_3-1)}$	$\frac{(n_2-1)Vo}{2n_2-1}$	$\frac{V_o}{1+n_2}$	$\frac{Vo}{1+n_3+D}$	$\frac{n_2-1}{2n_2+n_3-1}Vo$	$\frac{V_o}{2+n_2+n_3(2-D)}$
Voltage Gain	$\frac{n_3+2n_2-1}{(1-D)(n_2-1)}$	$\frac{n_3+2-D+n_2(1-D)}{1-D}$	$\frac{n_2}{1-D}$	$\frac{2n_2-1}{(n_2-1)(1-D)}$	$\frac{n_2+1}{1-D}$	$\frac{n_2+n_3+D(n_3-1)}{(n_3-1)(1-D)}$	$\frac{2n_2-1}{(n_2-1)(1-D)}$	$\frac{1+n_2}{1-D}$	$\frac{1+n_3+D}{1-D}$	$\frac{2n_2+n_3-1}{(1-D)(n_2-1)}$	$\frac{2+n_2+n_3(2-D)}{1-D}$

* Note: S/D/C/CI+L= Quantity of Switches/Diodes/Capacitors/CIs + Inductors, LICR=Low Input Current Ripple.

V. COMPARATIVE STUDY WITH SIMILAR TOPOLOGIES

This section provides an extensive comparison between the suggested converter with available similar topologies in the literature. It is meant to identify the merits and demerits of the proposed topology, comparing with other available alternatives and help the engineers to select proper topology among many available varieties.

Table 1 shows the essential properties of the offered converter and comparable CI-based converters with an active switch that have recently been discussed in [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21]. It includes voltage gain, normalized voltage stress (NVS) of the switch and diode, grounding approach, and component count. As shown in Table 1, the proposed topology achieves a considerably greater voltage gain and has less voltage stress on the power MOSFET than previous converters. Also, the smaller number of switches in the proposed converter than the converters provided in [14], [15], [19], and [20] makes the suggested converter easier to control. As a corollary, with appropriate design, the suggested topology can be able to use switch part with lower voltage ratings to obtain better efficiency. Another point that can be obtained from Table 1 is the fluctuation of the input current in the proposed converter versus the compared converters. Unlike the converters described in [13], [15], [17], [19], [20], and [21], the suggested converter has a small input current ripple for wide load conditions.

Comparison of voltage gain from multiple high gain topology is shown in Fig. 8. In order to make a fair comparison between these converters, the number of secondary turns (N_2) for two windings CI based converters was considered equal to 5 (equals the sum of the secondary and tertiary turn ratios in triple-winding converters). It can be found that with $n_2 = 2.5$ and $n_3 = 2.5$, the suggested topology has a higher voltage conversion than the converters provided in [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21] for all duty cycle values.

As shown in Fig. 9(a), the NVS of active MOSFET in the recommended topology is less than that of the topologies described in [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21] for all duty cycle numbers. This feature causes the power MOSFET to be selected at a lower cost, which affects the overall cost of the converter.

Furthermore, Fig. 9(b) depicts the NVS of the output diode of the proposed topology and high step-up converters described in [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21]. As it can be found from this Fig. 9(b), the NVS

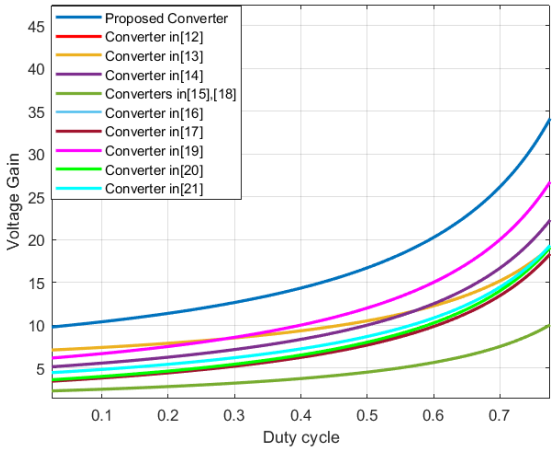

FIGURE 8. Comparison of voltage gain from multiple boost converters. ($n_2 = 2.5$, and $n_3 = 2.5$ for three windings CIs and $n_2 = 5$ for two windings CIs).

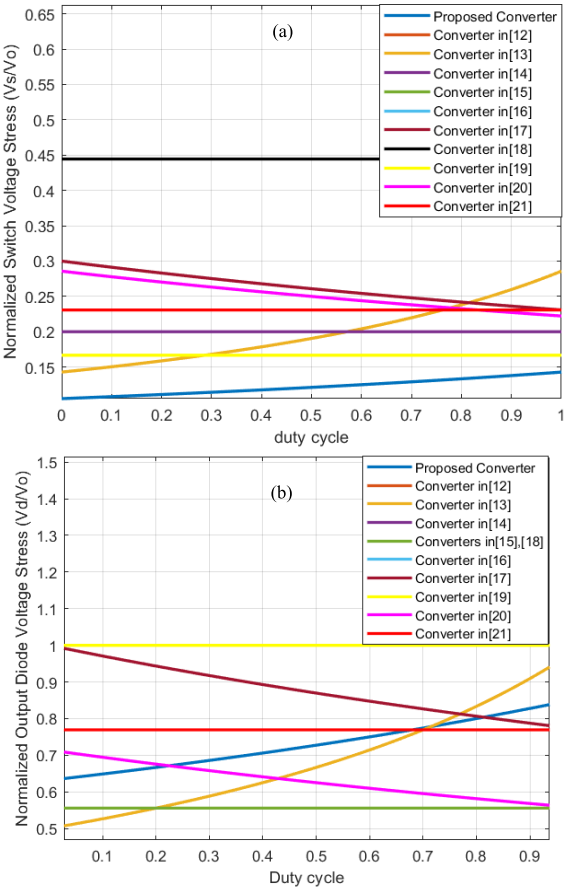

FIGURE 9. Features of high-gain topologies: (a) NVS of MOSFET, and (b) the output diode's NVS. ($n_2 = 2.5$, and $n_3 = 2.5$ for three windings CIs and $n_2 = 5$ for two windings CIs).

on output diode for suggested topology stays lower than output voltage for whole range of duty cycle. Furthermore, converters with lower voltage stress on their output diode than the suggested UHG topology often have weaker voltage boosting ability.

According to the comparative results, the suggested design has a much larger voltage gain than previous high step-up converters owing to the integration of three-winding CI, voltage lift capacitor (C_2), and voltage multiplier unit. Furthermore, using a three-winding CI in the proposed scheme allows for easier voltage gain control and optimization of MOSFET and other semiconductor active component construction.

TABLE 2. Voltage ripple and the minimum value of the capacitors except resonance capacitors.

	C_1	C_2	C_3	C_4	C_O
Voltage ripple	2%	4%	4%	4%	0.1%
Minimum value	15.62 μF	3.47 μF	6.25 μF	6.25 μF	39.06 μF

TABLE 3. Current ripple and the minimum value of the inductors.

	L_{in}	L_m
Current ripple	15%	50%
The minimum value	121 μH	128 μH

VI. EXPERIMENTAL RESULTS

To evaluate the effectiveness and confirm the theoretical study of the suggested UHG converter, the outcomes of a 200 W built power circuit of the suggested converter are reported.

The peak to peak ripple of the output capacitor (and other capacitors in the converter circuit) is suggested to be kept under 5% [27]. In our work we have tried to design the converter by compromising the performance and cost factors. By substituting voltage ripple of Table 2 into (37) and assumed capacitors average current equal to I_O, the minimum size of capacitors are listed in the Table 2. (The ESR of the capacitors are ignored due to their small sizes):

The peak to peak ripple lower than 50% of the maximum inductor current gives a good compromise between the size of the inductor, that's proportional to weight and cost, and the RMS currents [27]. Similar to the calculation of capacitors, the inductors' size are obtained by assuming the acceptable current ripples as they are reported in Table 3:

The experimental model of the specified converter is seen in Fig. 10, and the characteristics for every element are listed in Table 4.

The outcomes of the topology working in CCM are shown in Fig. 11. Blue lines show voltage waveform and red lines represent current waveform in all of the figures.

Figure 11(a) depicts the voltage and current of diode D_1. This diode, as shown in the image, has a ZCS circumstance,

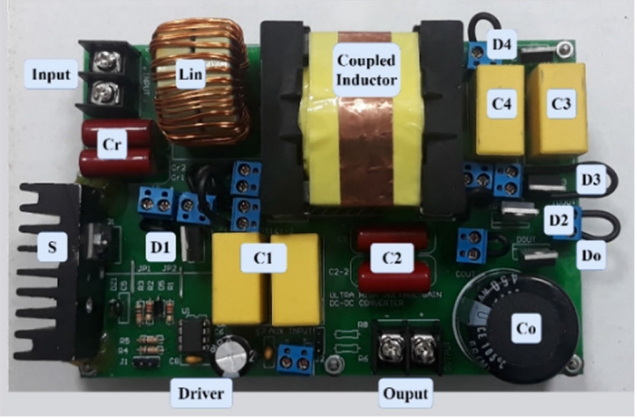

FIGURE 10. Experimental circuit of suggested UHG topology.

TABLE 4. Main parameters of experimental setup.

Parameters	Description/ Value
S	NCEP85T14, 3.6 mΩ on-resistance, V_{DS} =85V, I_D =140A
Diodes	
D_1, D_2, D_3, D_4	V30202C Schottky diode, V_F=0.69 V
D_O	SBR40U300CT, V_F=0.84 V
Magnetically Coupled Inductor (MCI)	Turns ratio: ($N1$: $N2$: $N3$=1: 2.5: 2.5) Core: ETD 49/25/16 ferrite core Magnetizing inductance: 140 μH Leakage inductance: 1.2 μH
Inductors	100 μH
L_{in}	Core: double T131-52 iron powder core
Capacitors	
C_1	2*8.2 μF, 63 V
C_2	2*2.2 μF, 400 V
C_3, C_4	8.2 μF, 63 V
C_O	330 μF, 450 V
C_r	2*2.2 μF, 400 V
Switching Frequency	50 kHz
Output Power	200 W
Input Voltage	17-20 V
Output Voltage	320 V
Nominal Gain	16

and its voltage waveform verifies the study provided in (18). As it can be found from Figure 11(a) after the current of diode D_1 reaches a maximum, its current decreases slowly. So soft switching occurs when the current reaches zero (According to Mode 5 and Mode 6 in section II).

The voltage and current waveforms of diode D_2 are depicted in Fig.11(b). Because the current of this diode varies with a tiny slope (Not suddenly with a steep slope) when it is turned on and off, it has a ZCS characteristic both when it is turned on and when it is turned off.

The waveforms of diode D_3 are shown in Fig.11(c). This diode, like diode D_2, has a ZCS behavior in both turning on and off. This diode's voltage waveform confirms the theoretical computations given in (20). As can be found from this figure After the voltage applied to the diode is zero, the current starts to increase with a low slope. Therefore, the overlap between voltage and current will be very low when the state of diode is changed (According to Mode 3 in section II).

Fig.11(d) is related to the output diode D_o. As it can be found, this diode is turned off in ZCS situation which will reduce the reverse recovery losses significantly. It can decrease the total cost of the system since its voltage stress is smaller than the output voltage.

The voltage and current of input inductor L_{in} are shown in Fig. 11(e). The continuation of the input current is a crucial aspect in several uses, particularly the utilization of solar panels. The average input current in Fig. 11(e) is 10 A, with a ripple of 150 mA. The voltages and currents in the CI primary and secondary windings are shown in Figs. 11(f) and 11(g), accordingly. The maximum voltage and current of L_{N1} are 35V,12A respectively. The maximum voltage and current of L_{N2} are 100 V and 3A respectively.

The drain-to-source voltage and drain current of the MOSFET are shown in Fig.11(h). The zoomed-in picture shows that this switch has a smooth switching action and that the switching losses are so low that they can be disregarded (According to explanations of Mode 1 in section II). If the rated current of the desired switch is less than that of the converter, or in order to increase the power of the proposed converter, several MOSFETs can be paralleled and increase the power of the converter.

The nominal and experimental prototype output voltages are shown in Fig. 12 to examine the correctness of the derived ideal voltage gain and compare it to actual voltage gain. Since one of the main advantages of this converter is to achieve high voltage gain in low duty cycle values, in this figure, the duty cycle is not considered higher than 0.6. Also, when duty cycle is high, the efficiency drops form our desired level and the conductive losses of the switch increase.

The output voltage, input current and their ripples are shown in Figure 13. As it can be found from this figure, the input current and output voltage ripple of suggested converter is very low. Furthermore, these figures meet the requirements set in Tables 2, 3. This converter is suitable for applications that require a low current ripple on the input side such as fuel cell and PV applications.

The waveform of the output voltage of the proposed converter with transient step load change is shown in Figure 14. As it can be seen, the proposed converter has an appropriate transient response when load is changed from %100 to %50 of its nominal power. In this figure the voltage overshoot is about 30V and the response time is around 250 ms. Due to the presence of only one active switch in the proposed converter, the closed loop state can be implemented with analog or digital circuits.

A. EFFICIENCY ANALYSIS

According to Table 4, in order to accurately evaluate the performance of the converter, it's better to analyze the converter losses by calculating the converter efficiency at 200 Watts. In general, the converter losses can be divided into 4 groups:

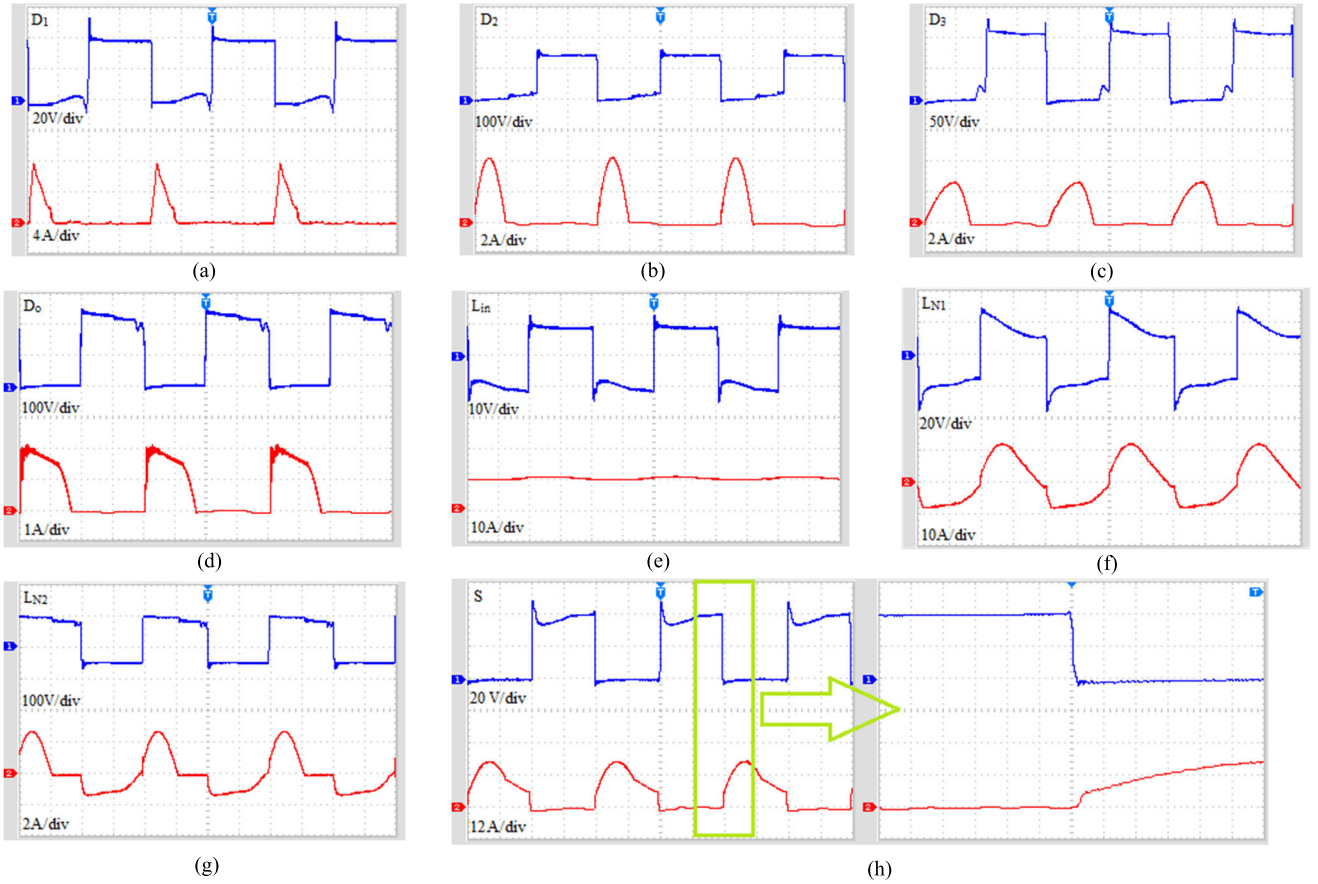

FIGURE 11. Experimental results of UHG Converter. Voltage and current in: (a) D1 (b) D2 (c) D3 (d) Do (e) Lin (f) L_{N1} (g) L_{N2} (h) Active switch, time: 5μs/div.

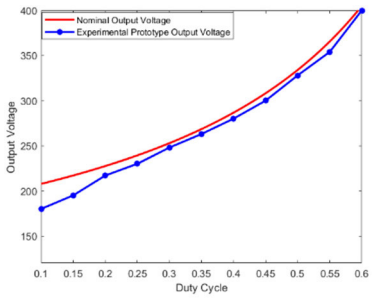

FIGURE 12. Nominal and experimental prototype output voltages.

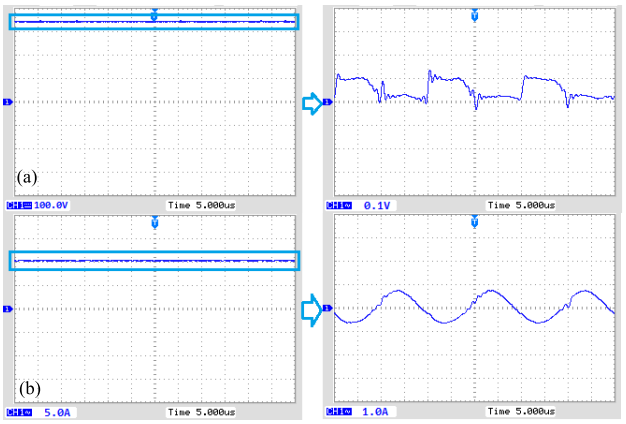

FIGURE 13. (a) Voltage ripple of output capacitor (b) Current ripple of input inductor L_{in}.

1) SWITCH LOSSES

Switch losses are divided into two categories: switching losses and conduction losses. Because of the soft switching of the topology at the moment when the switch is turned on, its switching losses only include losses during turning off. To calculate conduction losses and switching losses the following equation is needed:

$$P_{loss\ (turn\ OFF)} = \left(\frac{1}{2} * V_{ds} * I_{ds} * t_{turn-off\ \ fall\ \ time}\right) * f_s = 0.34 \tag{41}$$

where $t_{\text{turn}-\text{off fall time}}$ of the MOSFET in our experimental set-up is about 20 nano-seconds in $I_{DS} = 17$A.

$$P_{loss(conduction)} = R_{ds(on)} \times I^2_{ds(RMS)} = 1.04\,W \tag{42}$$

$$P_{loss(switch)} = P_{loss(turnOFF)} + P_{loss(conductionswitch)} = 1.38\,W \tag{43}$$

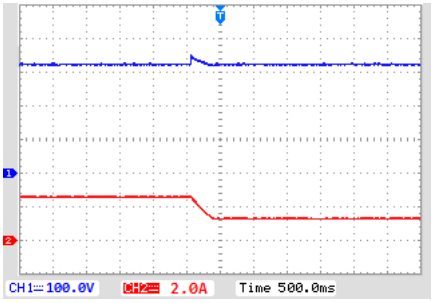

FIGURE 14. Converter response when output load changes from %100 to %50 (blue curve: output voltage, red curve: output current).

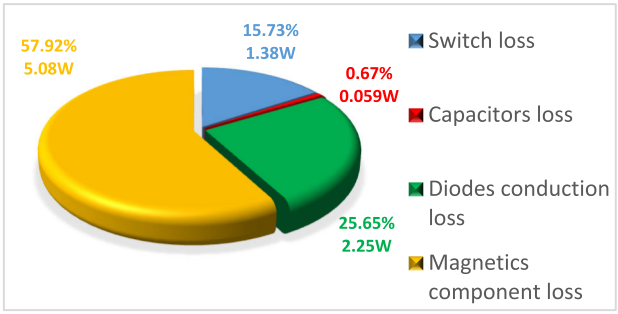

FIGURE 15. Comparison of voltage gain from multiple boost converters. (N2 = 2.5, and N3 = 2.5).

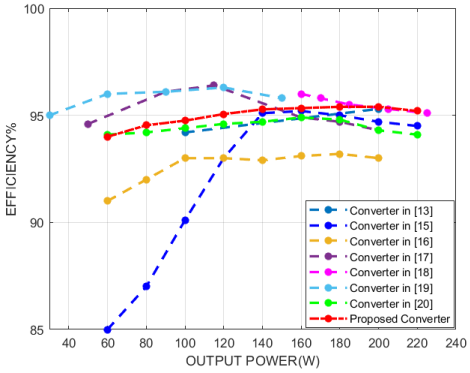

FIGURE 16. Comparison of efficiency in different loads.

2) DIODE LOSSES

In the case of diodes, the ohmic losses of the diodes and the reverse recovery loss of the diodes in this topology are ignorable and the main losses of the diodes are related to the voltage drop of the diodes in its average currents (conduction losses). For this reason, the following equation can be considered:

$$P_{loss(diode)} = V_{forward\ diode} \times I_{D(average)} = 2.25\,W \quad (44)$$

3) CAPACITOR OHMIC LOSS

In order to calculate the internal resistance loss of capacitors, the following equation can be considered:

$$P_{loss(capacitor)} = ESR \times I^2_{COUT(RMS)} = 0.059\,W \quad (45)$$

Only the output capacitor is considered because the rest of capacitors have a small ESR due to their material (MKT and Polyester). $I_{cout(rms)}$ is RMS current of output capacitor and it is approximately to I_O.

4) MAGNETIC LOSSES

According to T131-52 iron powder core datasheet the core loss of input inductor is considered 125 mW/cm^3 and the volume of each inductor is 13.68 cm^3. The same as input inductors, according to ETD49/25/16 datasheet the core loss of CI is considered 139 mW/cm^3 and the volume of each inductor is 24.3 mW/cm^3. The ohmic loss is equal and due to the large number of primary wire (they are wrapped in litz wire) the ohmic loss is negligible. Therefore, to calculate the core loss we can consider:

$$P_{loss(core)} = 3.38 + 1.7 = 5.08\,W \quad (46)$$

According to the equation of losses in previous sections, the efficiency of topology can be calculated as follows:

$$\eta = \frac{P_O}{P_O + P_{loss}} = \frac{200}{200 + 8.77} = 95.80\% \quad (47)$$

The total losses shown by (41)-(47) is illustrated as a pie chart in Fig. 15 for the implemented converter, where V_{in} is 18V and the output load is 200 W. This pie plots show that switch losses is low due to its low voltage ripple.

Fig. 16 depicts an efficiency comparison between the suggested topology and the converters based on CIs described in [13], [15], [16], [17], [18], [19], and [20] for different loads levels. The main reason for improving the efficiency is the ability to use the MOSFET with a small R_{ds} due to lower voltage stress on the switch and the ZCS operation of the main switch in the on state. Also, alleviating the reverse diode recovery issue and ZCS operation of diodes in this topology help to improve the overall efficiency of the converter.

VII. CONCLUSION

This work presents an ultra-high voltage gain (UHG) DC-DC structure depending on three windings coupled inductor (CI) and voltage multiplier cell (VMC). The crucial benefits of the proposed configuration are:

- ultra-high gain in a significant low turn ratio of CI and suitable zone of duty cycles, recycled energy of inductor. Comparison with similar topologies showed this superiority.
- Efficiency improvements due to soft switching process for main switch and other diodes. Comparison with similar converters showed appropriate converter efficiency.
- Low normalized voltage stress (NVS) on MOSFETs and other electronic components. The investigation of voltage stresses on components and experimental results confirmed this superiority.
- Low input current ripple, which causes less stress on the input source than the high current ripple converters. The experimental results verified this capability.

The principle of operation of the converter and its steady-state assessment under CCM situations have been comprehensively described.

Furthermore, the proposed UHG converter has two intrinsic characteristics that make it suited for use as a solar panel side DC-DC converter in Photovoltaic system. First, the input current is continuous and has a very small ripple. The second characteristic is its common ground, that can avoid common mode leakage current. Input current continuous simplifies the installation of maximum power point tracking (MPPT) controls, and the common ground characteristic can reduce the requirement for complicated leakage current control in PV system applications [25], [26].

Some other practical applications of the suggested converter are as follows:

- DC microgrid application.
- LED lightning.
- Automobile headlight (HID).
- Robotics.

The closed loop analysis and transient response of the suggested converter in different conditions can be studied in more detail in the future works.

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