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RESEARCH ARTICLE

An X-Band High-Accuracy GaAs Multifunction Chip With Amplitude and Phase Control

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ABSTRACT This paper presents a high-accuracy multifunction chip (MFC) with amplitude and phase control in X-band. The MFC is designed with a common leg structure and incorporates a 6-bit attenuator (ATT), a 6-bit phase shifter (PS), two gain compensation amplifiers (GCAs), three single pole double throw switches (SPDTs), and fourteen logic control circuits. The interstage matching networks (IMNs) are inserted to compensate for the insertion phase and attenuation changes from the design due to the mismatches occurring when cascading the separately designed PS and ATT blocks. The receive and transmit modes switching is achieved by using four SPDTs. In addition, the resistance feedback is used in GCAs to compensate for passive losses and provide gain to the MFC. The proposed MFC is fabricated in 0.15-μm GaAs pseudomorphic high-electron-mobility transistor (pHEMT) process. In the range of 8-11 GHz, the measured maximum root-mean-square (RMS) amplitude error of the MFC is less than 0.28 dB, and the maximum RMS phase error is less than 3.3°. Moreover, the MFC is achieved with a size of 4.3 mm $\times$ 2.85 mm. Excellent performance and compact size make the MFC great potential in spaceborne phased array applications.

INDEX TERMS Attenuator, GaAs, monolithic microwave integrated circuit (MMIC), multifunction, phase shifter, phased array.

I. INTRODUCTION

Active phased arrays are widely used in satellite communications due to the capacities of high-gain radiation and fast beam scanning. An active phased array often contains thousands of antennas with one independent transmit/receive (T/R) module per element. In aerospace, the T/R modules are required to be miniaturized and light-weighted to reduce cost. In order to increase the integration of T/R modules, one common way is using the multifunction chip (MFC), which combines as many functions as possible on a monolithic microwave integrated circuit (MMIC). Consequently, the size of T/R modules can be considerably reduced [1]. Moreover, the reliability of T/R modules is also enhanced due to the simplicity of the RF interconnection structures [2].

Although CMOS and Bi-CMOS processes are often utilized to design MFC because of their high integration characteristic [3], [4], the inherent weak anti-radiation performance of transistors limits its applications in aerospace. Therefore, the extra anti-radiation reinforcement package is needed, but at the cost of expense and volume. Fortunately, the GaAs process is more widely used in aerospace applications for its better anti-radiation performance, low noise, and power handling ability [5], [6]. Furthermore, the digital logic circuits can also be integrated on-chip using enhancement-mode (E-mode) and depletion-mode (D-mode) transistors like CMOS circuits to simplify the DC management circuits in T/R modules [7].

The MFCs applied to RF front ends typically integrate several blocks including phase shifter (PS), attenuator (ATT), logic control circuit (LCC), and gain compensation amplifier (GCA) [8]. Some MFCs with transceiving function also introduce circuits like single pole double throw switch (SPDT) to change the working state between transmit (Tx) and receive (Rx) [9]. High accuracy is required for MFCs used in phased arrays, but it is a challenge due to the large

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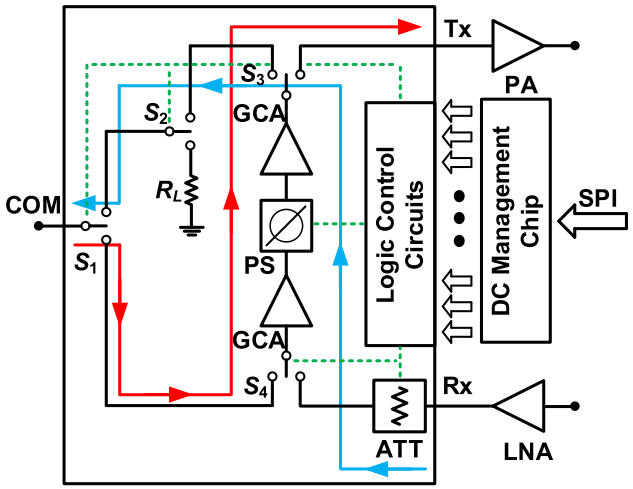

FIGURE 1. Block diagram of the 8-11 GHz MFC with common leg structure.

scale of the circuit. There are many studies on ATTs and PSs in [10], [11], [12], [13], [14], [15], and [16], and they all exhibit excellent attenuation and phase shift accuracy. However, cascading between blocks in the MFC changes the terminal impedances of the ATT and PS, causing deterioration in accuracy. Taking the ATT as an example, a 7-bit ATT is introduced in 6-18 GHz GaAs MFC in [17]. The ATT has a root-mean-square (RMS) amplitude error of less than 0.6 dB when operating independently, but degrades to 0.9 dB after cascading. Reference [18] designed a two-channel transceiving MFC with a 6-bit ATT RMS amplitude error of 0.45 dB, which almost reaches the minimum attenuator step. The RMS amplitude errors of the ATTs in [4], [19], [20], [21], and [22] exceed the minimum attenuator cell, causing overlap in some attenuation states.

In this paper, an 8-11 GHz MFC with high accuracy is proposed. The extra tunable interstage matching networks (IMNs) are designed in 6-bit ATT and PS to minimize the deterioration of the accuracy after cascading. The measured maximum RMS errors of amplitude and phase are respectively less than 0.28 dB and 3.3°. In spite of the extra introduction of IMNs, it still achieves a compact size with an area of only 4.3 mm × 2.85 mm, which is comparable to the Tx or Rx-only MFC in [20]. Apart from the ATT and PS, the MFC integrates GCA, SPDT, and LCC. In addition, The MFC also provides good gain flatness using resistance feedback techniques in the GCAs.

This paper is organized as follows. Section II introduces the architecture of the MFC. The analysis and design of each circuit building block are presented in Section III. Section IV describes the measurement of the MFC, including transmit and receive modes. Finally, the conclusion is summarized in Section V.

II. MULTIFUNCTION CHIP ARCHITECTURE

The MFC is designed and fabricated by using the PL15-12 process of WIN semiconductor [23], which is an InGaAs 0.15-μm pseudomorphic high-electron-mobility transistor (pHEMT). The cut-off frequency of the 0.15-μm gate length high-electron-mobility transistors (HEMTs) is up to 120 GHz, enabling its competence in the design of microwave circuits such as amplifiers, phase shifters, attenuators, etc., in the X-band. In addition to the common on-chip passive components, the adopted process also provides two gate lengths (5 μm, 10 μm) of E-mode and D-mode transistors, which can achieve the on-chip integration of the logical control circuits (LCCs).

The block diagram of the proposed MFC is shown in Fig. 1. It consists of a 6-bit ATT, a 6-bit PS, two GCAs, four SPDTs (S_1-S_4), and fourteen LCCs. The common leg structure is adopted to reduce the number of PS and GCAs, where the PS and GCAs are reused in transmit and receive mode, and the ATT only works in receive mode. The LCCs are applied to convert 0/+5 V to −5/0 V to control ATT, PS, and SPDTs. Among the fourteen adopted LCCs, twelve LCCs are used to control the working state of the 6-bit ATT and 6-bit PS, and the other two LCCs are employed to control SPDTs to switch the operating modes (Tx or Rx) of the MFC. Noteworthily, a 50-Ω load R_L is connected to the circuit for better matching performance when the channel is turned off. The GCAs are introduced to compensate for the passive losses caused by ATT, PS, and SPDTs, and to provide a gain of the MFC to satisfy the demand of the transceiver chains. The GCAs are supplied by +5V. Compared with the directly cascading structure, the input 1-dB power compression point (IP1dB) of the MFC is enhanced by separately placing the two GCAs at each end of the PS.

The MFC has been verified by the design of the individual block and is finally manufactured monolithically. These blocks are described in the following sections.

III. CIRCUIT BLOCKS OF THE MULTIFUNCTION CHIP

A. 6-BIT DIGITAL ATTENUATOR

The 6-bit digital attenuator is designed with a passive switching structure. This structure uses switches to change attenuation or reference states and utilizes the amplitude difference between two states to realize attenuation. Fig. 3 shows the 6-bit ATT with cells of 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, and 16 dB, covering the attenuation range of 0-31.5 dB.

For 0.5-dB and 1-dB attenuation, a simplified switched-T structure is adopted, as shown in Fig. 3(a). In this structure, the series resistors are ignored due to the small values, which significantly simplifies the circuits of the 0.5-dB and 1-dB attenuator cells. However, this structure deteriorates the impedance matching and is inapplicable for the design of larger attenuator cells. The switched-π structure has excellent matching performance for middle attenuation and thus is used to design 2-dB, 4-dB, and 8-dB attenuator cells, as shown in Fig. 3(b). For the 16-dB attenuator cell, the switched-π structure shows a low attenuation accuracy. Some studies [13], [25] intend to cascade two identical 8-dB attenuator cells. Nevertheless, this method needs a larger area

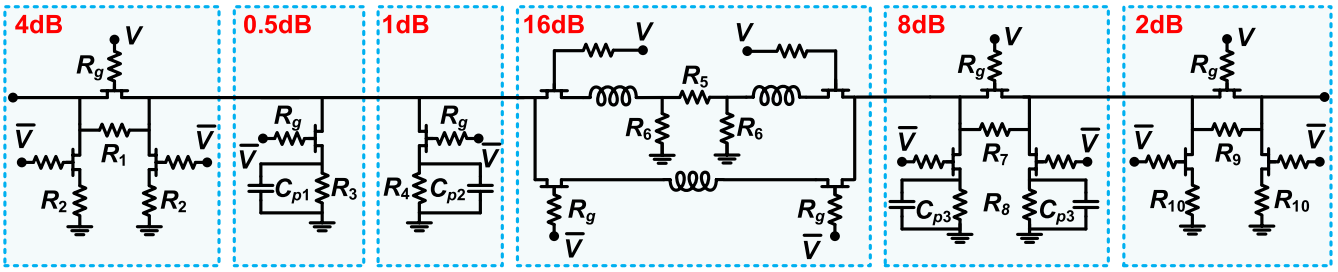

FIGURE 2. Schematic of the cascaded 6-bit digital attenuator.

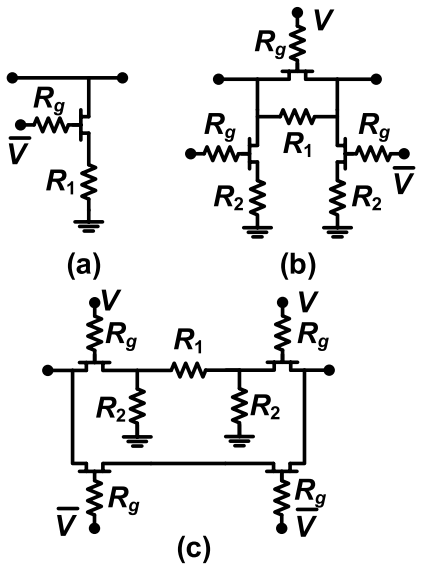

FIGURE 3. Schematics of the (a) 0.5 dB, 1 dB (b) 2 dB, 4 dB, 8 dB, and (c) 16 dB.

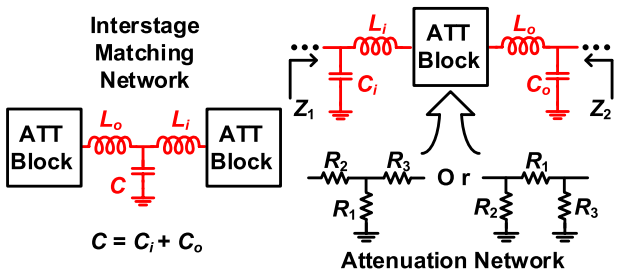

FIGURE 4. Typology diagram of the designed interstage matching network.

and increases the complexity of the circuit. Compared with the cascade structure, the switched-path structure can achieve large attenuation with a simpler circuit and thus is more suitable for 16-dB cell design, as shown in Fig. 3(c).

Due to the presence of the turn-off capacitances of the switching HEMTs, the transmission phase between the attenuation state and reference state is different, bringing about the insertion phase shift (IPS). In order to decrease the IPS, the shunt compensating capacitances C_p are introduced in the 0.5-dB, 1-dB, and 8-dB attenuator cells. When the attenuation is determined, the value of the IPS can be reduced by adjusting C_p. Fig. 5(a) shows the simulation results of IPS at different C_p. It can be seen that a suitable C_p can remarkably improve the IPS. The tuning methods for these topologies can be found in previous work [10].

The schematic of the cascaded 6-bit digital attenuator is shown in Fig. 2. The 2-dB and 4-dB cells are placed at both ends for better matching performance. The extra transmission lines are introduced in the 16-dB cell to balance the IPS. A good performance with high attenuation accuracy and low IPS is realized. However, the values of the resistances in each ATT cell are calculated based on 50 Ω terminal impedance, and it will introduce the imaginary part after the ATT is cascaded with other blocks in the MFC. Consequently, the attenuation values of 64 states are deviated due to impedance mismatching, leading to a significant deterioration of the accuracy. The simulated attenuation values of the three topologies used (represented by 1 dB, 8dB, and 16 dB) before and after cascading are respectively given in Fig. 5(b). It can be seen that the error introduced by the mismatch is mainly indicated in the attenuation flatness, which is difficult to be compensated by adjusting the resistances inside the ATT because it mainly affects the real part of the impedances.

Although the flatness can be improved by adjusting the terminal matching of the ATT, the narrow tuning range results in the inability to optimize the 64 states. In order to overcome this problem to obtain high accuracy of the attenuation, the extra tunable IMNs are introduced between each attenuator cell to enhance the tunability of the ATT after cascading. The topology diagram of the designed IMNs is shown in Fig. 4, which contains a capacitor and two inductors. Thereinto, L_i, and L_o denote the series inductances at the input and output terminals of the ATT cell, respectively. The parallel capacitance C is split into C_i and C_o to tune the impedance of the two adjacent cells. The improvement of the attenuation flatness can be expressed as an optimization problem. Fig. 5(c) illustrates the process of tuning L_i, L_o, C_i, and C_o to optimize the attenuation value of the 16-dB cell. The simulated results of the RMS amplitude errors of ATT in three states are given in Fig. 5(d). It can be seen that the introduction of IMNs significantly improves the attenuation accuracy of the ATT, and the RMS amplitude error after cascading is reduced by a maximum of 0.35 dB compared to that without IMNs. In addition, the IMNs are located in

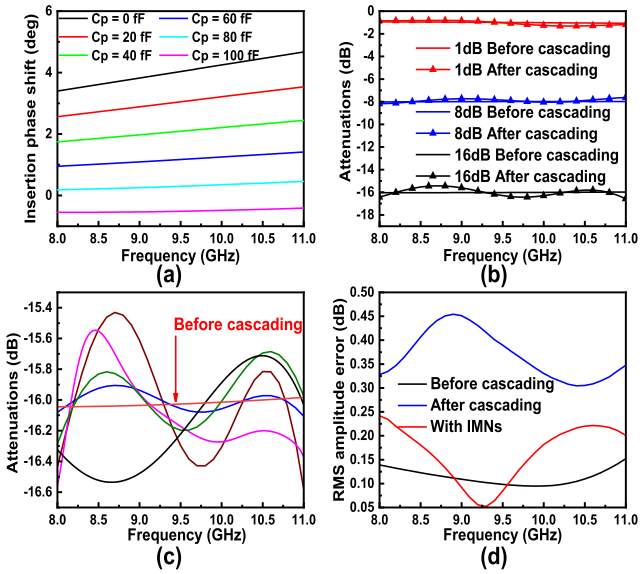

FIGURE 5. Simulated results of the (a) IPS at different C_p values, (b) the attenuation values of 1-dB, 8-dB, and 16-dB cells, (c) the process of optimizing the amount of attenuation values by tuning IMNs, and (d) the RMS amplitude errors of the ATT in three cases.

the common path between each ATT cell, thus there is no deterioration in the IPS.

B. 6-BIT DIGITAL PHASE SHIFT

The 6-bit digital phase shifter is designed with a passive switching structure to reduce DC power consumption. This structure uses switches to change phase shifting or reference states and utilizes the phase difference between two states to realize phase shift. The 6-bit PS with cells of 5.625°, 11.25°, 22.5°, 45°, 90°, and 180° covers the phase shift range of 0°-354.375°, as shown in Fig. 6. The turn-off capacitances need to be taken into account in the PS design because its value is similar to the capacitances used and has an impact on the phase shift.

The switched-LC structure can achieve small phase shift values with a compact size and thus is used to design the 5.625° cell, as shown in Fig. 6(a). However, the defect in bandwidth causes the switched-LC structure's performance to deteriorate as the phase shift increases. Compared with the switched-LC structure, the switched-all-pass structure has a wider bandwidth, as shown in Fig. 6(b). Besides, the inductances in the circuit and turn-off capacitances of M_1, M_2, and M_3 are reused both in reference and phase shifting states, making this structure also compact in size. Therefore, the switched-all-pass structure is used to implement the design of 11.25° and 22.5° cells. For 45° and 90° cells, the switched-all-pass structure exhibits a poor phase-shift flatness, and thus the switched-high/low-pass structure is used, as shown in Fig. 6(c). The similar phase-frequency characteristics of the high-pass and low-pass networks allow this structure to have excellent phase-shift flatness in broadband. Since on-chip inductances tend to introduce coupling effects causing potential deterioration of the phase shifting accuracy, π-type

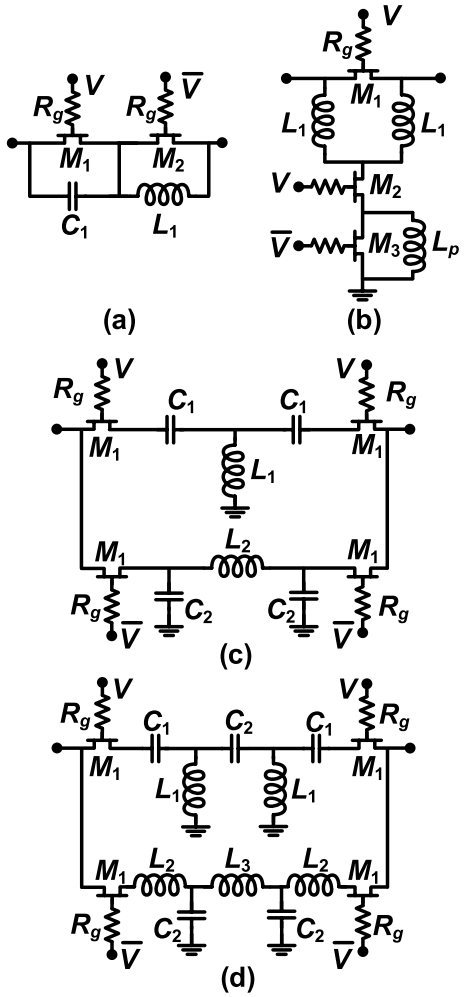

FIGURE 6. Schematics of the (a) 5.625°, (b) 11.25°, 22.5°, (c) 45°, 90°, (d) and 180°.

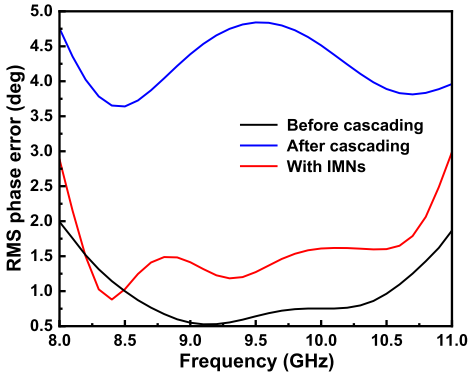

FIGURE 7. Simulated results of the RMS phase errors of the PS in three cases.

low-pass and T-type high-pass networks are used to decrease the number of inductances. Additional filters are designed in 180° cell to raise the values of phase shift to the required level, as shown in Fig. 6(d). The description of the operations for each topology is given in [24].

The schematic of the cascaded 6-bit digital phase shifter is shown in Fig. 8. Since the 5.625° cell phase shift is sensitive

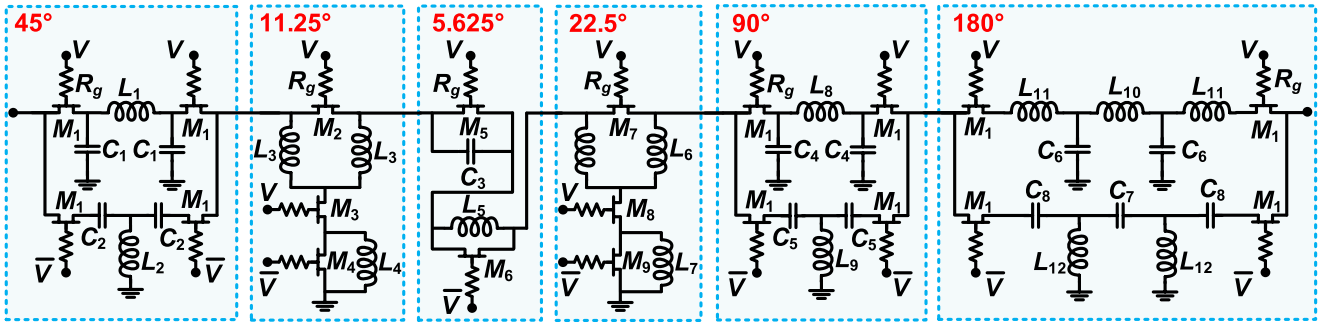

FIGURE 8. Schematic of the cascaded 6-bit digital phase shifter.

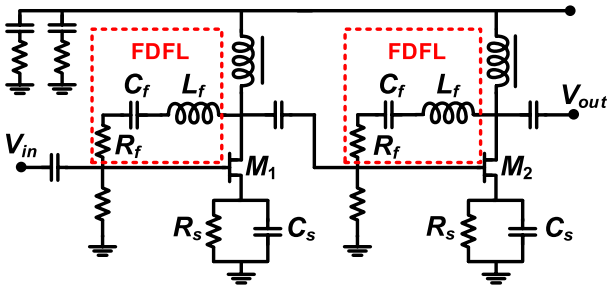

FIGURE 9. Schematic of the two-stage gain compensation amplifier with FDFL.

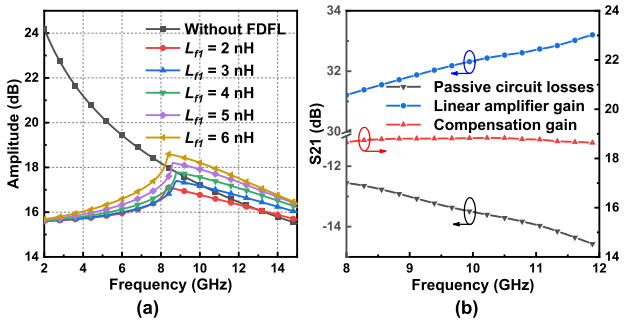

FIGURE 10. (a) Simulated results of the amplitude of amplifier with FDFL for different L_f. (b) Illustration of compensating for passive losses by adjusting the amplifier gain slope.

to external impedance changes, it is placed between stages. The 45° and 180° cells are placed at both ends because of their excellent matching ability. Similarly, the phase shifts also show a large in-band fluctuation after cascading with other blocks. Therefore, the IMNs are also used in PS to overcome this problem. The values of all lumped components and the size of the switching FETs are optimized to provide the best performance after cascading. Fig. 7 gives the simulated results of the RMS phase error in three states. It can be seen that the RMS phase error deteriorates to a maximum of 4.8° after cascading compared with the PS before cascading, but it can be optimized to less than 3° due to the introduction of the IMNs.

C. GAIN-COMPENSATED AMPLIFIER

The gain-compensated amplifiers are used to compensate passive losses resulting from the phase shifter, attenuator as

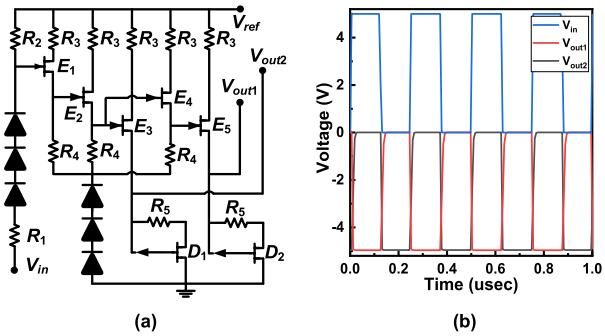

FIGURE 11. (a) The schematics of designed LCC. (b) The time domain transient simulated results of the LCC.

well as switches and to provide power gain for the MFC. The schematic of the two-stage GCA is shown in Fig. 9. The two GCAs are separately placed at each end of the PS in order to avoid saturation of the post-amplifier, as shown in Fig. 1. Inside GCA, the source self-biased structures are introduced to simplify the DC supply circuits. Since the passive loss increases with frequency, the GCAs should have positive-slope gain with respect to the frequency for improving the gain flatness of the MFC. Considering this requirement, the frequency-dependent feedback loops (FDFLs) are introduced. Due to the presence of the L_f, the low-frequency gain will be suppressed, as shown in Fig. 10(a). Therefore, by adjusting R_f and L_f, the gain of the GCA can be controlled to compensate for the passive losses in the MFC, as shown in Fig. 10(b).

D. LOGIC CONTROL CIRCUITS

The GaAs process-based switching HEMTs require negative voltages (lower than −3.3 V) to turn off. However, the 6-bit ATT, 6-bit PS, and switches in the proposed MFC need a total of fourteen pairs of complementary controlled voltages. This means fourteen extra 0 V and −5 V off-chip DC supply lines are requisite, respectively, complexing the T/R modules. Therefore, fourteen on-chip logical control circuits are introduced based on the integrated direct-coupled FET logic (DCFL) structure, as shown in Fig. 11(a). The LCC consists of voltage shifters and inverters composed of E-mode and D-mode HEMTs. When the reference voltage V_{ref} is set to −5 V, the circuit can convert the input 0/5 V pulse into

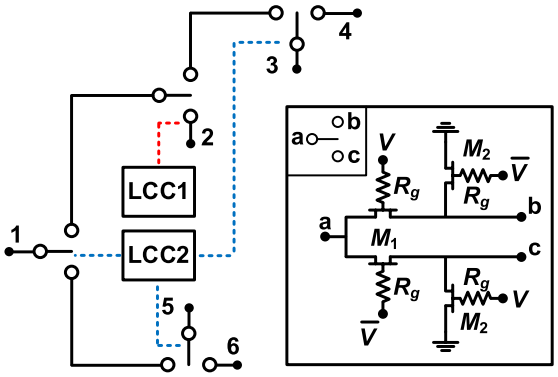

FIGURE 12. Topology diagram of the total SPDTs integrated in the proposed MFC.

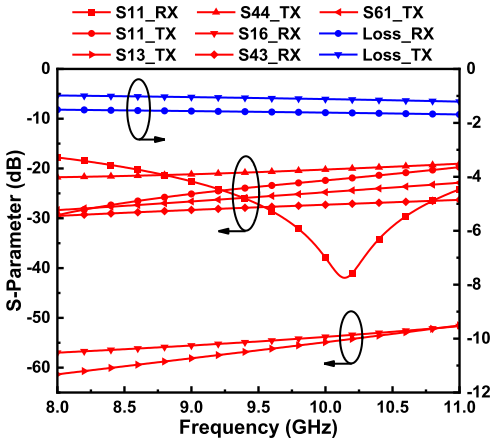

FIGURE 13. Simulated results of the SPDTs in TX and RX modes including reflection coefficients.

a pair of complementary −5/0 V V_{out1} and V_{out2} outputs, which achieves the control of ATT, PS, and switches with only half of the DC supply lines. The time domain transient simulated results of the LCC are given in Fig. 11(b).

E. SINGLE POLE DOUBLE THROW SWITCHES

Four SPDTs are integrated into the proposed MFC. The topology diagram of the total SPDTs is given in Fig. 12. Each SPDT contains four switching FETs and gate resistances (R_g) used to improve isolation and is controlled by a pair of logical complementary voltages supplied by an LCC. Two LCCs are applied to operate the SPDTs. One is applied to S_2 to control whether the MFC is switched to the load path, and the other is used for S_1, S_3, and S_4 to switch the transmit and receive paths. Fig. 13 gives the simulated results including the reflection coefficients, insertion losses, and isolations of the total SPDTs in Tx and Rx modes, respectively. It can be seen that the total SPDTs achieve good performance with reflection coefficients of less than −18 dB, insertion losses of less than 1.8 dB, and isolations of better than 51 dB.

IV. SIMULATION AND MEASUREMENT RESULTS

The designed X-band MFC is fabricated in 0.15-μm GaAs pHEMT process. The microscope photograph is shown in

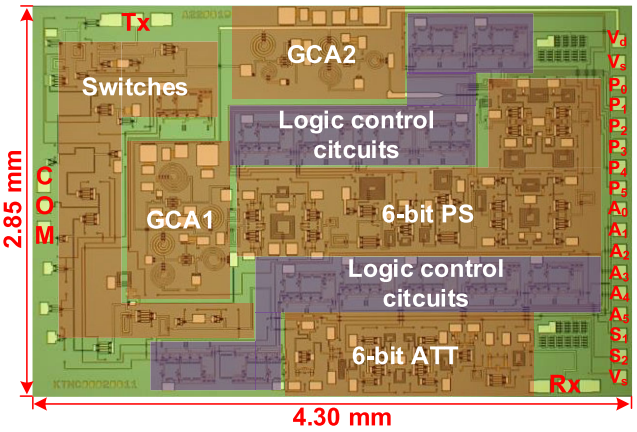

FIGURE 14. Micrograph of the designed X-band multifunction chip.

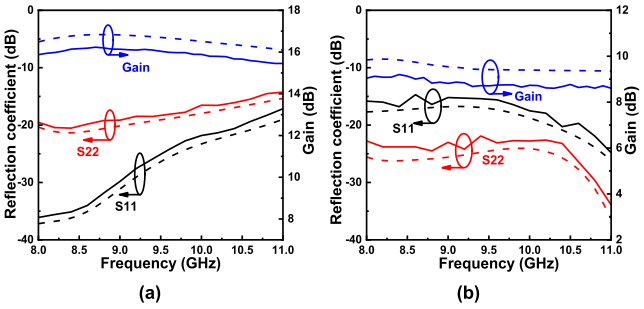

FIGURE 15. Measured (solid line) and simulated (dashed line) results of the gain and reflection coefficients in (a) transmit mode and (b) receive mode.

Fig. 14 with an area of 4.3 mm × 2.85 mm, and the chip is measured on-wafer by using a Keysight N5245A microwave network analyzer and a Cascade Summit 1200M probe station. Fig. 15 shows the simulated and measured results of the gain and reflection coefficients in transmit and receive modes for the reference state. The measured gains are approximately 1 dB lower than the simulated gain, which is mainly due to the model errors that lead to larger losses in the fabricated components. In addition, the repeated usage of the GSG probe also has a slight impact on the measured gain. However, it still shows a good performance in the operating band. The measured reference gains are higher than 15.5 dB and 8.6 dB in transmit and receive modes, respectively. The reflection coefficients of the transmitting mode are lower than −15 dB, and those of the receiving mode are lower than −15.2 dB. Since 6-bit ATT and 6-bit PS need to be separately measured in the transmit and receive modes, the measured results are divided into the following three sections for better visualization.

A. THE MEASUREMENT OF ATTENUATOR IN RECEIVE MODE

The simulated and measured RMS amplitude errors and phase errors of the 6-bit ATT for 64 states in the receive mode are shown in Fig. 16 when the PS is set to the reference state. Due to the application of the IMNs, the attenuator has

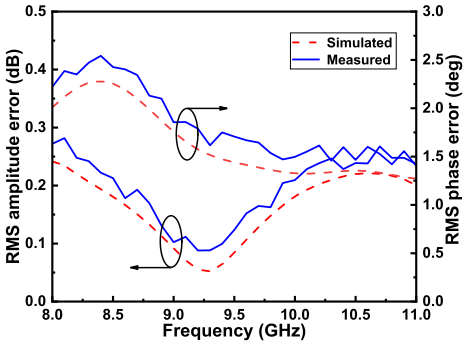

FIGURE 16. Measured (solid line) and simulated (dashed line) rms amplitude errors and rms phase errors of the 6-bit ATT for 64 states in receive mode.

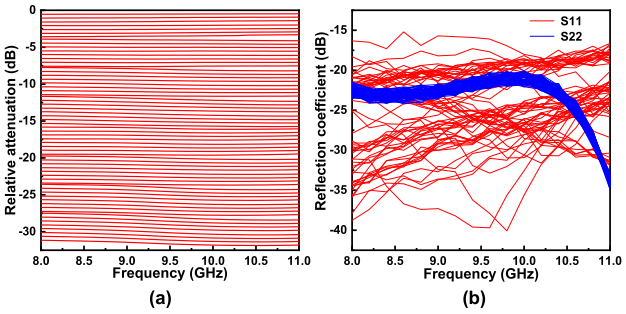

FIGURE 17. Measured results of the (a) relative attenuation and (b) reflection coefficient of the 6-bit ATT for 64 states in receive mode.

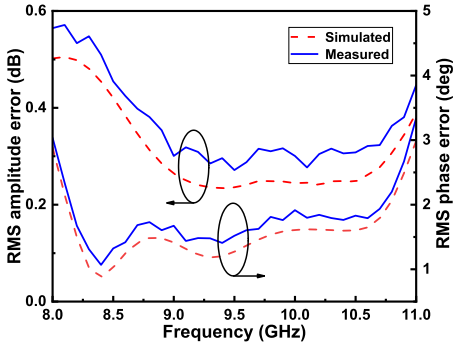

FIGURE 18. Measured (solid line) and simulated (dashed line) rms phase errors and rms amplitude errors of the 6-bit PS for 64 states in receive mode.

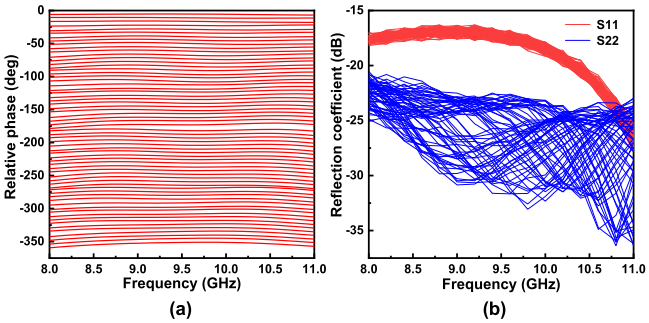

FIGURE 19. Measured results of the (a) relative attenuation and (b) reflection coefficient of the 6-bit digital phase shifter for 64 states in receive mode.

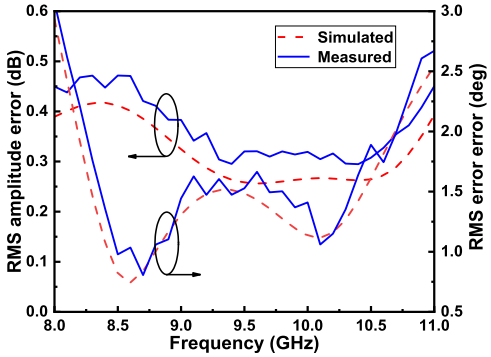

FIGURE 20. Measured (solid line) and simulated (dashed line) rms phase errors and rms amplitude errors of the 6-bit PS for 64 states in transmit mode.

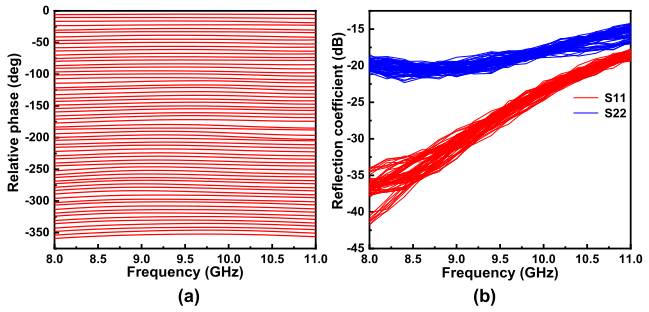

FIGURE 21. Measured results of the (a) relative attenuation and (b) reflection coefficient of the 6-bit PS for 64 states in transmit mode.

an excellent attenuation accuracy in 8-11 GHz with an RMS amplitude error of less than 0.28 dB. As the result of the phase shift compensation circuits, the attenuator has a low insertion phase shift with an RMS phase error of less than 2.6°. Fig. 17(a) shows the measured results of the relative attenuation for 64 states. It can be seen that the total attenuation of 0 to 31.5 dB is achieved with a step of 0.5 dB. In Fig. 17(b), the measured results of 64 states' reflection coefficients in receive and common ports are displayed. The input and output reflection coefficients are less than −15.2 dB and −24 dB, respectively.

B. THE MEASUREMENT OF PHASE SHIFTER IN RECEIVE MODE

The measured and simulated RMS amplitude errors and phase errors of the 6-bit PS for 64 states in the receive mode are shown in Fig. 18, when the ATT is set to reference state. It can be seen that the maximum RMS phase error is 3.3° and lower than 2° within 8.2-10.5 GHz, and the RMS amplitude error is lower than 0.58 dB. Fig. 19(a) shows the measured results of the relative phase for 64 states. The total phase shift of 5.625° to 354.375° is achieved with a step of 5.625°. In Fig. 19(b), the measured results of the 64 states' reflection coefficients in receive and common ports are displayed. The input and output reflection coefficients are less than −17 dB and −20.5 dB, respectively.

C. THE MEASUREMENT OF PHASE SHIFTER IN TRANSMIT MODE

Fig. 20 shows the measured and simulated results of RMS phase errors and amplitude errors of the 6-bit PS for 64 states

TABLE 1. Performance summary and comparison with other works.

Ref	Process	Freq (GHz)	$Gain_{MAX}$[1] (dB)		$OP1dB_{MAX}$[1] (dBm)		PS/ATT (# of bits)	RMS Amplitude Error (dB)	RMS Phase Error (°)	Chip Size (mm^2)	Return Loss (dB)
[17]	0.25-μm GaAs	6~18	12		26		-/7	0.9	-	20	<-21
[18]	0.25-μm GaAs	7.5~9	-		-		6/6	0.45	2	15.75	<-19
[19]	0.25-μm GaAs	6~18	20 Tx	23.5 Rx	17		4/4	0.5	8	25.8	<-9
[20]	0.18-μm GaAs	12~18	17.3		-		4/5	0.7	6.4	11.7	<-5
[26]	0.25-μm GaAs	7.6~9.1	-		-		6/6	0.6	5.5	-	<-10
This work	**0.15-μm GaAs**	**8~11**	**15.9 Tx**	**8.9 Rx**	**11.9 Tx**	**7.8 Rx**	**6/6**	**0.28**	**3.3**	**12.2**	**<-14.8**

[1] Maximum value over the operating band.

in the transmit mode. The measured results are slightly different from the receive mode which can be ascribed to the change in transmit and receive path impedance. Nevertheless, due to the presence of the IMNs, the PS also achieves good performance with the RMS phase errors and RMS amplitude errors of less than 3° and 0.47 dB, respectively. The measured results of the 64-state relative phase are shown in Fig. 21(a). The measured results of the transmit and common ports' reflection coefficients for 64 states are given in Fig. 21(b). It can be seen that the input and output reflection coefficients are lower than −14.8 dB and −18 dB, respectively.

In Table 1, the performance of the MFC proposed in this paper is summarized and compared with the previously reported GaAs MFCs. Integrating a 6-bit digital ATT, a 6-bit digital PS, two GCAs, four SPDTs, and fourteen LCCs in a compact size, the designed MFC achieves excellent accuracy due to the introduction of the IMNs. The measured RMS amplitude error is better than other works, and the RMS phase error is only lower than [18].

V. CONCLUSION

In this paper, a high-accuracy MFC operating in 8-11 GHz is proposed and fabricated in the WIN PL15-12 GaAs pHEMT process. The MFC integrates a 6-bit ATT, a 6-bit PS, two GCAs, four SPDTs, and fourteen LCCs. The extra IMNs are introduced in the ATT and PS to improve the accuracy after cascading with other blocks in the MFC. The measured results show that the RMS amplitude error of the ATT is less than 0.28 dB and the RMS phase error of the PS is less than 3.3°. The area of the MFC is 4.3 mm × 2.85 mm. The advantages of small footprint, anti-radiation capability, and high accuracy make this MFC suitable for potential application in spaceborne phased-array T/R modules.

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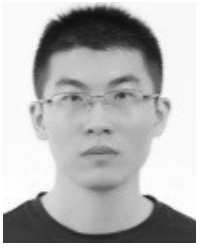

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