Guest Editorial Special Issue on Emerging Converter Topology, Operation, and Design Technologies

POWER electronics play a key role in the transition to carbon neutrality. To enhance the performances of power electronics systems, new theories and methods are entering the field of power converter research, leading to increasing diversity of the knowledge database regarding converter design and operation methods. In addition to the conventional case-bycase design methodology, new automated and generalized converter design philosophies integrating topology derivation and synthesis methods, optimal pulse-width modulation (PWM), and advanced control strategies are gaining attention in both academia and industry. By implementing these methods, the converter design process can be greatly improved while the potentials of various power converters can be fully explored, leading to elevated converter performances.

With the increasing research volume in power electronics, it is important to establish a comprehensive knowledge database in order to expand the frontiers of power electronics research. This special section serves this purpose with the objective to collect the latest innovations in converter topology, operation, and design methodologies.

In response to the call for articles, there is a total of 159 manuscripts submissions, including 97 original submission and 62 revisions. 41 articles were accepted for publication. The accepted articles can be generally classified into nine groups, where short summaries of the accepted articles in each group are included in the following sections.

A. Systematic Power Converter Topology Synthesis and Derivation

In [A1], Gonzatti et al. propose a singular basic switching cell complementary to the traditional canonical switching cell, which can constitute SEPIC, Zeta converters, and Z-source converters, and improve the understanding of the existing converter relationships and inspire insights for new topological developments and applications.

In [A2], Panigrahi et al. first quantify the number of converter choices available for a given input and output specification using the flux balance equation (FBE), and then illustrate that it is possible to find out the total number of possible FBEs. Once the FBEs are known, synthesizing a converter can be carried out as an inverse problem, and three different strategies to solve this inverse problem are presented with critical synthesis results summarized.

In [A3], Zhu et al. propose a non-isolated dc–dc high stepup converter with passive switched-inductor-capacitor network for the applications, such as battery-powered LED lighting systems and high-intensity mobile discharge lamps. The proposed circuit can produce higher gain voltage with small duty cycle, which decreases the voltage stress and conduction power loss on the active switches.

In [A4], Ambagahawaththa et al. show a simple yet powerful topology synthesis method based on the low-entropy equations that reveal the connection between the energy-storing elements and switches. The synthesis of multi-topology converters using low-entropy equations has been demonstrated.

In [A5], Zhang et al. analyze the topology construction principles and propose a systematic approach to derive multiple-input converters (MICs) and multiple-output converters (MOCs). A family of viable and optimized MICs and MOCs with various characteristics derived from the typical Buck converter is presented as an example.

B. Topology Study and Modeling of dc–dc, dc–ac, and ac–dc Power Converters

In [A6], Martin et al. develop a dynamic model for a low-inertia dc solid-state transformer formed by inductorless modular multilevel converters (MMCs) based on phaseshifted square-wave modulation. The developed model explicitly defines the circulating energy and retains its accuracy with an arm inductor-less operation. The predictive control is designed to achieve fast dynamic control with reduced computational burden.

In [A7], Deng et al. propose the generic analysis and design of zero-voltage-switching (ZVS) multi-phase ac-dc converters. Based on the proposed theory, a ZVS two-stage three-phase photovoltaic (PV) inverter is investigated, which is regarded as a five-phase converter. In addition, the extension of the ZVS multi-phase converter in different applications is introduced.

In [A8], Saha et al. give an analytical expression-based modulation scheme for half-bridge matrix-based dual-active-bridge (MB-DAB) converters, which is directly implementable on a microprocessor and is capable of achieving near full-cycle ZVS turn-on of all MOSFETs and unity power-factor (UPF) operation.

In [A9], Strajnikov et al. establish analytical guidelines for designing coefficients of PI controller, typically employed as voltage loop compensator of power factor correction rectifiers (PFCR). The proposed methodology allows concretizing the commonly used "5–10 Hz crossover frequency, 45° –70° phase

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margin" rule-of-thumb, typically utilized in application notes of commercial PFCR controllers.

In [A10], Strajnikov et al. build the analytical expressions linking the coefficients of the PI + Notch (PI + N) controller with the improved dynamic performance merits for a given value of dc-link capacitance. Corresponding dc-link voltage loop gain phase margin and crossover frequency expressions are derived, and the feasibility region of proposed design guidelines is clearly indicated.

In [A11], Gensior considers the parallel-connected twolevel voltage source converters that share the same ac and dc terminals. The converter currents are controlled using hysteresis controllers such that a desired current distribution among the parallel converters may be ensured. The proposed approach shows lower semiconductor losses and grid current harmonic distortion.

C. New Theories for Power Converter Topology Analysis, Evaluation, and Operation

In [A12], Li et al. summarize the milestones and general applications of the powerful mathematical tool, i.e., graph theoretical approaches, and illustrate its unique benefits in some emerging/challenging power electronics research topics, e.g., systematic converter derivation and modeling, advanced control, etc.

In [A13], Chen et al. propose a topology deduction method based on reinforcement learning to gain the benefits of both forward and inverse design. The proposed method uses a neural network for forward design and takes a set of simple rules to give rewards for reverse design. Thus, many existing topologies are deduced, and some new topologies can be found.

In [A14], Li et al. provide a systematic method to construct types of quadratic converters. Almost all of the known nonisolated quadratic converters with two inductors, two capacitors, two power switches, and two diodes can be re-developed by this method, but also many new topologies can be proposed. Further, the proposed method can be extended to generate cubic or nth-power converters.

In [A15], Bai et al. analyze the inherent limitation of the four-switch buck-boost converter through inconsistent frequency response and noncontinuous duty cycle operation region aspects. Then, a model predictive control (MPC) method characterized by tuning-free cost function is presented to achieve multi-mode control and smooth transition simultaneously.

D. New Multilevel Converter Topologies for Various Applications

In [A16], Paul et al. propose a reduced component staircase (STC) type nine-level inverter designed with only two dc sources, as well as it detailed performance analysis. The proposed topology has a much lesser number of conducting switches and higher efficiency, which can be extended to a generalized multi-module staircase (MM-STC) inverter with fewer dc sources.

In [A17], Zhu et al. present a new resonant modular multilevel dc-dc converter based on the conventional boost

converter. The proposed converter has the inherent-balancing capability of SM capacitor voltages without additional complex balancing control.

In [A18], Wang et al. propose a dual-T-type modular multilevel converter (TMMC) composed of stackable ad-dc-ac power cells, where each cell consists of two high-frequency T-type legs and one low-frequency switched common leg. A coordinated modulation method is also proposed to address the capacitor voltage balancing issue.

In [A19], Barzegarkhoo et al. propose a five-level gridconnected transformerless inverter composed of an integrated switched-boost module (SBM) as well as a switched-flying capacitor (SFC) cell. The SBM is used to generate the fivelevel output voltage with self-balanced capacitors, while the SFC cell can achieve a quadratic voltage conversion gain of the proposed converter.

E. Resilient Control and Fault-Tolerant Operation of Multilevel Converters

In [A20], Fan et al. propose an enhanced three-arm alternate arm multilevel converter (AAMC) for achieving dc fault ridethrough capability with reduced semiconductor power devices compared to the hybrid MMC. The closed-loop control system is designed to dynamically regulate the energy sharing between dc and ac stacks.

In [A21], Wang et al. present a coupled-dc power modulebased cascaded multilevel converter integrating utility-scale photovoltaic generations (CDPM-PV), and the proposed modulation strategy can not only ride through a larger range of module mismatches but also improve solar power utilization and system efficiency.

In [A22], Liu et al. present a new concept to evaluate the over-modulation risk for the MMCs, namely, dynamic modulation ratio (DMR), which can dynamically change according to the variation of operating conditions and can reflect the modulation characteristics more accurately.

In [A23], Wang et al. investigate the behavior of the modular multilevel matrix converter (M3C) under open-circuit faults, and propose a suitable fault detection criterion for the M3C by transferring the observation errors of circulating currents into specific values.

F. Multi-Physics Converter Analysis, Modeling, and Design

In [A24], Ranjram et al. propose a modeling approach that enables the circuit representation of a "coupled electronic and magnetic system" (CEMS) to be directly extracted. The proposed approach is suitable both for assessing the finer details of the variable inverter/rectifier transformer and other fractional-turn transformers, and as a framework for deriving and understanding new CEMS implementations.

In [A25], Loureiro et al. present a design methodology for creating a set of high-voltage gain dc–dc converters, which is based on ladder switched capacitor with coupled inductor. Detailed evaluations about the derivation of each topology and comparative analysis among the main features of eight high-voltage converters are included.

In [A26], Boles et al. systematically enumerate isolated and non-isolated dc-dc converter topologies and switching sequences capable of efficiently utilizing piezoelectric transformers as their only energy storage components. The proposed switching sequences maintain high-efficiency behaviors across wide voltage gain and load ranges.

G. Optimized PWM Strategies for Various Converter Topologies and Applications

In [A27], Won et al. study the multi-cell series-parallel converter and propose an optimized multi-carrier PWM strategy to avoid unwanted modes. By modifying the multi-carrier waveforms, the proposed PWM can ensure frequent parallel connectivity to improve balancing effect while preserving simple current control implementation.

In [A28], Li et al. propose a phase-disposition PWM (PDPWM)-enabled model predictive control (MPC) for a ninelevel inner-interleaved hybrid multilevel converter (9L-IHMC), which can achieve optimal current tracking, capacitor voltage balance, and the mitigation of circuiting currents simultaneously.

In [A29], Cheng et al. propose a modified carrier redistribution PWM (CRPWM) for a five-level stacked multicell converter (5L-SMC), based on exchanging the arrangement of the carriers of PDPWM. The proposed method can achieve natural balancing of both the dc-link and flying capacitors (FCs), with the same harmonic performance of the line-to-line voltage as the conventional PDPWM.

In [A30], Qin et al. propose a hybrid space vector modulation (SVM) for a three-level quasi-Z-source inverter. By properly categorizing and selecting the voltage vectors, the proposed method can reduce both the amplitude and frequency of the common-mode voltage (CMV), control the neutral-point voltage, and boost the dc-input voltage simultaneously.

In [A31], Ma et al. propose a dual-mode modulation scheme by combining the PWM and nearest level control (NLC) modulation for MMC, to address the dc current fluctuation issue under NLC modulation with the circuiting current suppression controller. The mechanisms of the dc current fluctuation of MMC under NLC modulation is also modeled and analyzed comprehensively in this article.

In [A32], Wu et al. propose a modified carrier-overlapped PWM (COPWM) for a four-level nested neutral-point-clamped converter to address the FC voltage fluctuation issue under low fundamental frequency. The proposed method can balance the FC voltages naturally over each switching period. A deadtime compensation method is also developed to eliminate the dead-time induced voltage spikes under this proposed COPWM.

H. Application of Wide Band-Gap Devices With Multilevel Converters

In [A33], Zhang et al. propose a low-voltage low-loss active reflected wave canceller (ARWC) for medium-voltage SiC-based motor drive with a generalized multilevel converter topology, where the example of a single-phase SiC-based three-level active neutral-point-clamped (3L-ANPC) inverter is used to elaborate the proposed ARWC.

In [A34], Guo et al. propose a self-voltage balanced 3L-ANPC inverter with hybrid Si/SiC configurations, where two switches operate at low switching frequency and four switches operate at high switching frequency. Besides, the problem of inrush currents during capacitor voltage balancing and the false-triggering issue of the high-frequency switches are discussed and addressed in this article.

In [A35], Han et al. propose a multilevel active power filter (APF) under a multi-carrier-based PWM to suppress the CMV in multilevel inverter systems, where a five-level ANPC type II converter with SiC MOSFETs is used for illustration. The proposed APF can inject an output voltage that is equal to the CMV generated in the multilevel inverter system, thus the overall CMV can be attenuated effectively.

I. Optimal Design and System Level Integration of Power Converters in Utility Grid, Distributed Energy Resources, Electric Vehicles, etc

In [A36], Shah et al. propose an integrated power converter (IPC) with driving/charging capabilities for four-phase switched reluctance motor (SRM) drive-based electric vehicle (EV) application. With the proposed IPC, only two current sensors are employed for measuring phase currents under all operating conditions.

In [A37], Pan et al. develop the power ramp-rate control (PRRC), power limiting control (PLC), and power reserve control (PRC) strategies for series-PV-battery systems, where the power ramp-rate/limiting/reserve constraints are maintained by the coordinated control of individual converters.

In [A38], Nair et al. propose a novel method for instantaneous neutral-point balancing for a six-phase stacked multilevel inverter-fed induction motor (IM) drive. The results ensure that the proposed method for zero instantaneous neutral point current is valid for both steady-state and transient conditions of a six-phase IM drive using the stacked multilevel inverter.

In [A39], Pourgharibshahi et al. illustrate the practical implementation of Y-Matrix Modulation for a medium voltage grid-tie switched-capacitor modular multilevel converter (SC-MMC) with a middle submodule. Y-Matrix generation is simplified using a less computationally demanding method and Y-Matrix modulation for a four-submodule SC-MMC with a middle submodule is demonstrated.

In [A40], Foray et al. investigate the design of a lowcost 800–12 V, 4-W-isolated dc/dc converter for automotive applications. In particular, a selected topology based on a multilevel FC stage is analyzed. The converter operating mode selection is studied and simulation results reveal the interest in operating at the limit of the ZVS mode.

In [A41], Badawi et al. investigate the utilization of the fourswitch three-phase inverter (FSTPI) active front end (AFE) in a medium-voltage regenerative cascaded H-bridge (CHB) drive. The challenges of this application, e.g., capacitor voltage balancing and input current harmonics in grid-connected scenarios, are analyzed in detail in this article. Solutions are also proposed to address those challenges. The Editorial Team hopes that this Special Issue will provide readers with new inspirations for research and will encourage them to make further progress in topics related to power converter topology, operation, and design methodologies. The Editorial Team believes that in the long term, extensive research in this field will strongly push innovation forward, accelerating the industrial applications of more advanced power converter topologies and their optimal control and operation schemes.

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APPENDIX: RELATED ARTICLES

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