Improved Capacitive Power Transfer With Non-Resonant Power Transfer Link Using Radio Frequency Push-Pull Inverter

Adrian Amler, Nikolai Weitz, and Martin März

***Abstract*— In recent years, research on wireless power transfer and switched-mode power supplies with a capacitive coupling link has been on the rise. While many researchers investigate resonant coupling links, often resulting in tough requirements for the involved inductors, this article focuses on the elimination of all inductive components in the coupling link and the rectifier through the use of a non-resonant capacitive link. We propose a converter with a resonant single-ended push-pull inverter operating at radio frequencies of, e.g., 13.56 MHz to directly drive the non-resonant capacitive power transfer (CPT) link. The ability of the converter to operate at a high frequency and facilitate a significant voltage change across the link capacitors improves the power transfer characteristics of the system compared to previously published systems with a non-resonant capacitive link. Said combination is also beneficial for the transient behavior, parameter variation robustness, an easy design process, simplified drive requirements, and a predictable and limited capacitor voltage stress. The presented converter transmits 122.9 W across an effective link capacitance of 120 pF, leading to the highest input voltage-normalized power transfer to link capacitance value of 13.7 W/(nF·V) among previously published CPT systems with a non-resonant link.**

***Index Terms*— Capacitive coupling, high-frequency power converters, resonant inverters, wireless power transfer (WPT).**

NOMENCLATURE

X	Symbols for dc signals.
x	Symbols for time-varying signals.
$\hat{x}$	Maximum value for time-varying signals.
$\bar{x}$	Average value for time-varying signals.
x_{ac}	ac component of time-varying signals.
X_{min}	Minimum permissible design/operating point value.
X_{opt}	Optimum design/operating point value.
X_{max}	Maximum permissible design/operating point value.
u_X	Voltage across component X [V].
i_X	Current through component X [A].
ω_{sw}	Operating frequency ($\omega_{\mathrm{sw}} = 2\pi f_{\mathrm{sw}} = 2\pi / T$) [Hz].
U_{in}	dc input voltage [V].
U_{out}	dc output voltage [V].
I_{in}	dc input current [A].
I_{out}	dc output current [A].
P_{in}	dc input power [W].
P_{out}	dc output power [W].
η	dc–dc efficiency.
$f_{\mathrm{inv,res}}$	Inverter resonant frequency [Hz].
$u_{\mathrm{cpl,in}}$	Link input voltage (at primary sides of $C_{\mathrm{cpl1/2}}$) [V].
$u_{\mathrm{inv,out}}$	Inverter output voltage ($u_{\mathrm{inv,out}} = u_{\mathrm{cpl,in}}$) [V].
$u_{\mathrm{cpl,out}}$	Link output voltage (at secondary sides of $C_{\mathrm{cpl1/2}}$) [V].
$u_{\mathrm{rec,in}}$	Rectifier input voltage ($u_{\mathrm{rec,in}} = u_{\mathrm{cpl,out}}$) [V].
$u_{\mathrm{rec,in,0}}$	Initial condition for $u_{\mathrm{rec,in}}$ at the beginning T [V].
D	Duty cycle for ON-/OFF-control operation.
R_L	Load resistance [Ω].
$C_{\mathrm{cpl1/2}}$	Link capacitances [pF].
$C_{\mathrm{cpl,\Sigma}}$	Effective total link capacitance ($C_{\mathrm{cpl,\Sigma}} = \frac{C_{\mathrm{cpl1}} C_{\mathrm{cpl2}}}{C_{\mathrm{cpl1}} + C_{\mathrm{cpl2}}}$) [pF].
L_{dc}	Inverter input choke [nH].
$L_{\sigma 1/2}$	Inverter resonant inductors ($L_{\sigma 1/2} = L_{\sigma}$) [nH].
$C_{\mathrm{sw1/2}}$	Switch capacitances ($C_{\mathrm{sw1/2}} = C_{\mathrm{sw}}$) [pF].
C_{inv}	Effective inverter switch capacitance [pF].
C_{rec}	Effective rectifier input capacitance [pF].

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The authors are with the Department of Electrical Engineering, Institute of Power Electronics, Friedrich-Alexander-Universität Erlangen-Nürnberg, 90429 Nuremberg, Germany (e-mail: adrian.amler@fau.de; nikolai.weitz@fau.de; martin.maerz@fau.de).

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I. INTRODUCTION

WIRELESS power transfer (WPT) and isolating switched-mode power supplies (SMPSs) both require a power transfer link across galvanic isolation. In the past, most such systems relied on a magnetic field instead of an electric field, namely inductive power transfer (IPT), as the power density in capacitive power transfer (CPT) systems was insufficient [1]. With progress on fast switching wide bandgap semiconductors enabling efficient power converters at increased switching frequencies while maintaining high power levels, applications based on CPT have become more attractive.

For WPT, CPT shows some advantages over IPT in a broad range of applications. In biomedical implants, the use of CPT can result in a lower absorption rate in tissues [2]. Cost, losses, and alignment behavior of distributed sensor networks can be improved [3]. In wireless charging applications [4], [5], when transferring energy through a track [6], [7], [8], and in fixed [9] and rotating assemblies [10], [11], [12], [13], CPT

provides the implementation of a lightweight, cost-effective, and alignment-insensitive solution compared to IPT. Thus, CPT has found its way into various energy transfer systems, for example, for drones [14], [15], robots [16], EVs [17], [18], [19], [20], railway, maritime, and aviation applications [21], [22], [23], [24].

For SMPS, high switching frequencies are desirable as they offer improved dynamic behavior and allow for miniaturization following the reduction of stored energy in passive components. At high operating frequencies in the MHz range, problems related to the design, materials, and losses of inductive couplers can be avoided by switching to capacitors as the main element of the power transfer link [25]. A power transfer across galvanic isolation can be realized and can be safety certified using discrete Class Y capacitors [26], [27], [28], [29], [30]. The coupling capacitor values are only limited by normative restrictions for the common mode currents (e.g., [27]).

In this article, we investigate CPT with a non-resonant link. While most previously published CPT circuits integrate the coupling capacitances into their own resonant network (e.g., [10], [12], [13], [15], [16], [17], [18], and [20]), there are some downsides to the use of such a resonant link. A resonant circuit needs time to settle and may require precise tuning or an extensive number of inductive elements to achieve insensitive behavior. An unintentional excitation of a resonant coupling link may violate the link capacitor voltage limit, which, in WPT systems, is set by the permissible field strength between the link plates and, in SMPS applications, is defined by the breakdown voltage of the used capacitors [31]. A non-resonant coupling link avoids these issues. It is advantageous as the link capacitor voltage stress is limited by the breakdown voltage of the directly connected inverter and the rectifier semiconductors. It will be shown later that it provides a rapid settling time and tolerance against link and load variations. In the topology presented in this article, no further inductors are required beyond the inductors needed for the inverter operation. This enables the elimination of all inductors in the link and the rectifier, and compact designs are achievable, especially on the secondary side.

Despite the mentioned advantages, non-resonant CPT links, as considered in this article, have up to now not seen widespread use because of their major drawback, which is the low power to capacitor value ratio. It results from the missing compensation compared to a resonant link [32] and from restrictions of the implemented topologies, which are, for example, low operating frequencies (e.g., [19] and [33]) or the implementation of the link capacitors as dc blocking capacitors with large capacitor values needed to minimize their influence on the converter behavior (e.g., [34]). This article looks at the theoretical limits of a non-resonant capacitive link. At radio frequency (RF) switching frequencies in the HF-band (3–30 MHz), a significant amount of power in the watt-to-kilowatt range can be transmitted across directly driven non-resonant capacitive link elements. We address the challenge of finding a suitable topology and present a CPT system with a non-resonant link based on a current-mode Class D (CMCD)-like resonant push-pull inverter with inherent soft switching to mitigate the beforementioned topology issues. The inverter used in this article can directly drive the non-resonant capacitive link at RF frequencies and can tolerate load and link capacitance variations while maintaining efficiency. We improve the power-to-link capacitance ratio for non-resonant links by directly charging and discharging the link capacitors by the inverter instead of implementing them as dc blocking capacitors.

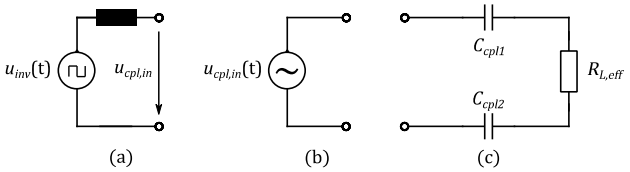

Fig. 1. (a) Abstract model of a series resonant, and (b) directly driven (c) CPT link.

In this article, Section II investigates the properties of non-resonant CPT. The operation of the mentioned topology is analyzed and modeled in Section III and experimentally verified in Section IV. An SMPS and a WPT implementation are shown, and the transmission of 122.9 W across an effective coupling capacitance of 120 pF is demonstrated. Section V discusses the presented ideas and results, and compares them to other proposals of non-resonant CPT in the literature. Section VI concludes this article.

II. Non-Resonant CPT

To estimate the power transfer of a capacitive system, the abstract model shown in Fig. 1 can be used. The transferred power is identical, whether the transfer link [see Fig. 1(c)] is driven by a square voltage source (e.g., bridge inverter) combined with a resonant inductive tank [see Fig. 1(a)] or by a sine voltage source [see Fig. 1(b)], as long as the input voltage of the transfer link $u_{\mathrm{cpl,in}}$ is identical. The resonant tank of the bridge inverter requires a sufficiently high quality factor so that the link current is approximately a sine wave. For a given operating frequency ω_{sw}, the capacitor values $C_{\mathrm{cpl1/2}}$, and a peak link input voltage $\hat{u}_{\mathrm{cpl,in}}$, the maximum transmittable power is calculated by

$$P_{\max} = \frac{\omega_{\mathrm{sw}} C_{\mathrm{cpl1}} C_{\mathrm{cpl2}}}{4\left(C_{\mathrm{cpl1}} + C_{\mathrm{cpl2}}\right)} \hat{u}^2_{\mathrm{cpl,in}} = \frac{1}{4} \omega_{\mathrm{sw}} C_{\mathrm{cpl},\Sigma} \hat{u}^2_{\mathrm{cpl,in}}. \quad (1)$$

It is reached when the effective load resistance

$$R_{L,\mathrm{eff,opt}} = \frac{C_{\mathrm{cpl1}} + C_{\mathrm{cpl2}}}{\omega_{\mathrm{sw}} C_{\mathrm{cpl1}} C_{\mathrm{cpl2}}} = \frac{1}{\omega_{\mathrm{sw}} C_{\mathrm{cpl},\Sigma}} \quad (2)$$

matches the coupling capacitor reactance. The resulting division of $\hat{u}_{\mathrm{cpl,in}}$ among $C_{\mathrm{cpl},\Sigma}$ and $R_{L,\mathrm{eff,opt}}$ contributes to the factor of 1/4 in (1).

C_{cpl1} and C_{cpl2} can be summarized as an effective link capacitance $C_{\mathrm{cpl},\Sigma}$, which equals the series connection of both capacitors. While $u_{\mathrm{cpl,in}}$ and $C_{\mathrm{cpl},\Sigma}$ are usually limited by the application and the component properties, an increased frequency $\omega_{\mathrm{sw}} = 2\pi f_{\mathrm{sw}}$ allows for a higher output power at a given $u_{\mathrm{cpl,in}}$ and $C_{\mathrm{cpl},\Sigma}$. Fig. 2 shows an evaluation of (1) for a coupling capacitor range that is typically achievable in

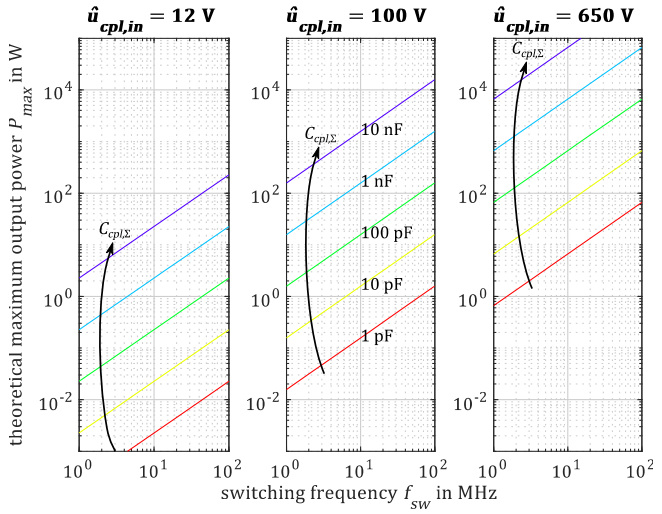

Fig. 2. Theoretical limit of CPT at a given effective capacitance and a given capacitor voltage strain.

applications such as consumer devices or vehicle charging (single to triple digit pF for WPT and high pF to low nF for SMPS). At lower MHz switching frequencies, sufficient power levels are reached for these applications. For example, at a switching frequency of 13.56 MHz within the ISM frequency band of raised EMI limits, at a 650 V peak inverter output voltage (i.e., a voltage, where the stress of two series connected capacitors does not exceed the typical stress of Class Y capacitors under their intended operation as filter capacitors), and with a 100 pF effective total capacitance, about 900 W can be transmitted.

To implement a CPT system with a non-resonant link and a sufficiently high power level, a topology that is capable of high switching frequencies and generates a high coupling link input voltage is needed. It should only produce soft voltage transients, as the capacitive link current is directly proportional to the voltage gradient at the capacitors. Topologies found in the literature can be divided along the type of inverter into bridge converters, PWM-based quasi-resonant converters, and resonant inverter-based converters [31]. Of the three, resonant inverters are the best choice for the following reasons.

Bridge converters have high power transfer abilities while keeping the semiconductor stress low but require either a dc choke [35] or matching networks in the coupling link, of which the simplest L-compensation is susceptible to parameter variations, and others, such as *LLC* or double-*LC*, become increasingly complex because of the increased number of components [31]. Driving high side switches at high frequencies is critical due to timing, level shifting, and gate waveform quality [25], making bridge inverters not preferred for the intentions pursued in this article and are, therefore, not further considered.

PWM-based converters can also demonstrate low semiconductor stress, are insensitive to parameter variations, offer various control mechanisms, and usually realize a non-resonant CPT but are problematic at high frequencies as soft switching is not inherent [36]. Normally, the power-to-link capacitance

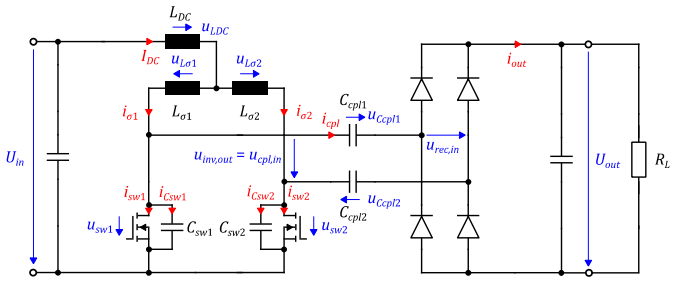

Fig. 3. Proposed converter topology.

ratio is very low [37], [38], rendering them impractical for driving a non-resonant CPT link.

Converters based on single-ended resonant power amplifiers as inverters, i.e., resonant topologies with a common ground referred control of all active switches, avoid driving high side switches, most parasitics are integrated into the circuit, and soft switching is intrinsic, but efficiency over a wide output voltage range is usually low and sensitivity toward component value variations, and semiconductor strain is high [25], [36]. Resonant inverters for CPT have been enhanced toward better parameter variation tolerance and lower device stress through the development of autonomous [39], [40] or Class ϕ_2 push-pull topologies [34], but, in the case of the mentioned autonomous push-pull inverters, the coupling capacitors are still integrated into a resonant link, and in the case of [34], where the coupling capacitors are dc blocking capacitors and, thereby, in accordance with the definition of non-resonant coupling capacitors, there is still a resonant tank within the coupling link and the load. The CMCD [41], [42], [43], [44], [45], [46] inverter has up to now not been used for CPT. While its efficiency is lower when compared to the Class E or Class ϕ_2 inverters, it is easy to design and tune, and offers smaller inductor values and a higher resilience toward load variation while maintaining ZVS [45], [46].

III. Investigated Converter Topology

The topology considered is shown in Fig. 3. We propose to drive a non-resonant capacitive interface directly by a resonant push-pull inverter. The inverter structure is similar to that of a CMCD with a center-tapped inductor, but its behavior differs, as it is adapted to driving a non-resonant capacitive load. In particular, the switch currents do not resemble the characteristic block currents, and the link behavior is not resistive. The rectifier is a bridge rectifier. Due to the non-resonant link, its conduction states are time-dependent, and the link input voltage depends on the inverter and link capacitor voltages. This causality influences the inverter behavior. In Section III-A, we discuss the qualitative behavior of the inverter and introduce necessary simplifications. In Section III-B, the power transmission is described in the time domain. A method for calculating the waveforms in the time domain is presented in Section III-C. In Section III-D, properties of the preliminary design criteria, as assumed in Section III-A, are looked at, and conclusions to their improvement are drawn. The influence of

applicational requirements and parasitic effects are described in Section III-E.

A. Inverter Behavior

To simplify the description and the modeling of the converter, the following assumptions are made.

1) The semiconductors show ideal behavior, the forward voltages are zero, MOSFETs contain antiparallel diodes, their parasitic capacitances are assumed linear, and the rectifier diodes are free of parasitic capacitances. The output capacitor is large enough so that its impedance compared to the impedance of the coupling capacitors is negligible for high-frequency currents.
2) Passive reactive components are assumed loss-free. Practically, the quality factor of the inverter is sufficiently high so that semiconductor losses can be neglected for modeling purposes.
3) The push-pull branches are symmetrical; the values of $L_{\sigma 1}$ and $L_{\sigma 2}$, C_{sw1} and C_{sw2}, and C_{cpl1} and C_{cpl2}, respectively, are identical. The values of the components are preliminarily chosen in a way that the inverter maintains ZVS at the secondary idle (SI) and the secondary side short (SS) circuit states. It is shown later that, ideally, the inverter resonant frequency $f_{\mathrm{inv,res,SS}}$ at SS matches the switching frequency f_{sw}.
4) The switches of the inverter are driven complementary with a duty cycle of 0.5. f_{sw} is constant and preferably within the ISM frequency bands. The current and voltage waveforms of both branches are set off by half a period but identical otherwise.
5) The main inductance L_{dc} is large compared to the resonant inductances $L_{\sigma 1}$ and $L_{\sigma 2}$ so that the input current ripple is low, and its influence on the inverter behavior is negligible. As L_{dc} is comparatively large, the current sum $I_{\mathrm{dc}} = i_{\sigma 1} + i_{\sigma 2}$ is approximately constant. Any high-frequency ac current component in either branch will be visible in an inverted manner in the other branch, $i_{\sigma 1,\mathrm{ac}} = -i_{\sigma 2,\mathrm{ac}}$. At SI and SS states, the assumption of ideal components results in $I_{\mathrm{dc}} = 0$, and therefore, $i_{\sigma 1} = -i_{\sigma 2}$. Furthermore, as the average voltage across inductors is zero, the average switch voltages are $\bar{u}_{\mathrm{sw1}} = \bar{u}_{\mathrm{sw2}} = U_{\mathrm{in}}$.

First, we assume a secondary open loop, idle condition (SI), where no current flows into a load. Therefore, there is never a current flow across the link and into the rectifier. In the steady state, following the previous assumptions, only the switches S_1 and S_2 with their capacitances C_{sw1} and C_{sw2} and the inductances $L_{\sigma 1}$ and $L_{\sigma 2}$ are involved in the behavior of the inverter. At the beginning of a new period, S_1 switches OFF, and S_2 switches ON. The effective equivalent circuits for the following half of a switching period are displayed in Fig. 4. $L_{\sigma 1}$ and $L_{\sigma 2}$ are magnetized in the direction of $i_{\sigma 1}$, as marked in Fig. 3. As soon as S_1 switches OFF and S_2 switches ON, the current $i_{\sigma 1}$ commutates to the switch capacitance in a ZVS switch-OFF. The equivalent circuit of Fig. 4(b) is valid. The current driven by $L_{\sigma 1}$ charges the switch capacitance C_{sw1} until the inductor is demagnetized. As there is now a voltage across $L_{\sigma 1}$ and $L_{\sigma 2}$ (in positive $u_{L\sigma 1}$ and negative

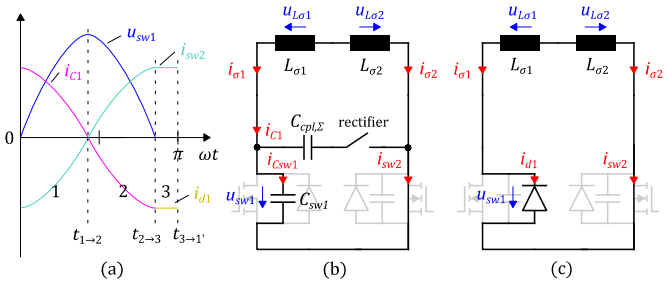

Fig. 4. (a) Time intervals, and (b) and (c) related equivalent circuits during a half period in which S_2 is ON. (circuit (b) is valid during intervals 1 and 2, and circuit (c) is valid during interval 3).

TABLE I
CHARACTERISTIC PROPERTIES OF THE INVERTER

Parameter	*Secondary idle state (SI)*	*Secondary short circuit state (SS)*	*Relation*
Characteristic impedance Z_0	$\sqrt{\frac{2L_\sigma}{C_{sw}}}$	$\sqrt{\frac{2L_\sigma}{C_{sw}+C_{cpl,\Sigma}}}$	$Z_{0,SI} > Z_{0,SS}$
Inverter resonant frequency $f_{inv,res}$	$\frac{1}{2\pi\sqrt{2L_\sigma C_{sw}}}$	$\frac{1}{2\pi\sqrt{2L_\sigma(C_{sw}+C_{cpl,\Sigma})}}$	$f_{inv,res,SI} > f_{inv,res,SS}$
Switch voltage strain $\hat{u}_{sw}$	$\frac{f_{inv,res,SI}}{f_{sw}}\cdot\pi U_{in}$	$\frac{f_{inv,res,SS}}{f_{sw}}\cdot\pi U_{in}$	$\hat{u}_{sw,SI} > \hat{u}_{sw,SS}$
Inductor peak current $\hat{\imath}_\sigma$	$\frac{U_{in}}{4f_{sw}L_\sigma}\ \left(\sim\frac{f_{res}}{Z_0}\right)$	$\frac{U_{in}}{4f_{sw}L_\sigma}$	$\hat{\imath}_{\sigma,SI} = \hat{\imath}_{\sigma,SS}$

$u_{L\sigma 2}$ directions), $L_{\sigma 1}$ and $L_{\sigma 2}$ are magnetized in the opposite direction of the marked $i_{\sigma 1}$ until u_{sw1} at C_{sw1} is completely drained. As soon as u_{sw1} reaches zero, the antiparallel diode of S_1 begins to conduct. In consequence of all switch voltages being at zero, the stray inductances of the inverter are in a free-wheeling state. The equivalent circuit in Fig. 4(c) is valid. Now, the formerly switched-OFF S_1 can perform a ZVS switch-ON. The described sequence of states and the corresponding waveforms are depicted in Fig. 4(a). The behavior and the waveforms of the other branch during the second half of a switching period are identical to the previously described waveforms at the first branch during the first half of the switching period. The presented waveforms compose the push-pull behavior of the inverter. The characteristic properties of the inverter at SI are shown in Table I.

The inverter can be operated in an SI state, as shown, but also in an SS condition. The equivalent circuit of a secondary shorted coupling link and rectifier is the series connection of both link capacitances with an effective capacitance of $C_{\mathrm{cpl},\Sigma} = 1/2 \cdot C_{\mathrm{cpl}}$ with $C_{\mathrm{cpl}} = C_{\mathrm{cpl1}} = C_{\mathrm{cpl2}}$. Because always one switch is ON and the effective link capacitance $C_{\mathrm{cpl},\Sigma}$ acts as positioned laterally between the drains of both switches, the link acts always as in parallel to the switched-OFF switch. Therefore, during every conduction state of the rectifier, the switch capacitance and the effective link capacitance can be summarized into one effective total capacitance $C_\Sigma = C_{\mathrm{sw1/2}} + C_{\mathrm{cpl},\Sigma}$. Thus, the SS behavior is identical to

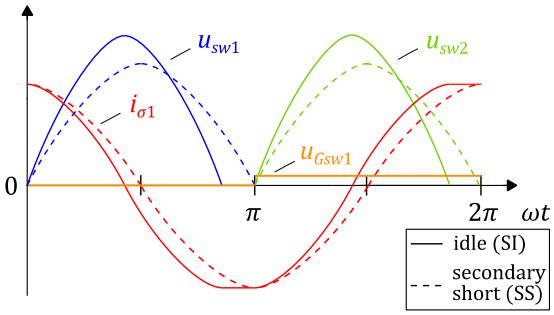

Fig. 5. Inverter waveforms during SI and SS states.

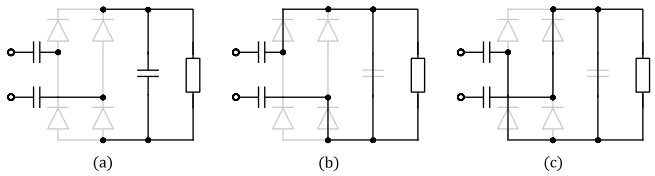

Fig. 6. High-frequency equivalent circuit of the coupling link and the rectifier in (a) nonconducting state, and (b) and (c) conducting state with (b) positive and (c) negative currents directed toward the inverter in the upper link.

the SI behavior with a difference only in the characteristic properties, as seen in Table I. Table I also shows the ratio of the values of the characteristic properties compared for both states. They are marked with the corresponding suffix in the index. As $f_{\text{inv,res}}$ is minimal at SS, f_{sw} is chosen to match $f_{\text{inv,res,SS}}$. On the one side, this keeps the duration of interval 3 to a minimum and eliminates it completely while in SS, which is favorable as, during interval 3, no power transmission takes place, and the circulating inverter currents cause losses. On the other side, ZVS is maintained for the complete load range, thus allowing operation in the complete output voltage range from SS to SI. The influence of the ratio of C_{sw}, C_{cpl}, and L_σ will be discussed later in Section III-D because an understanding of the power transfer and its consequences on the load range, established in Sections III-B and III-C, is necessary.

As S_1 and S_2 are connected to the input voltage U_{in} only by inductors, their average voltage must be $\bar{u}_{\text{sw1/2}} = U_{\text{in}}$. If the time interval in which the voltage is sinusoidal becomes shorter because of a higher $f_{\text{inv,res}}$, and the voltage is zero for a longer duration, the voltage stress of the switches increases to keep the condition for $\bar{u}_{\text{sw1/2}}$. The switch voltage stress during SI is higher than during SS because the maximum $f_{\text{inv,res}}$ is reached during SI. The minimum $f_{\text{inv,res}}$ is present in the SS state. In all other operating points, the relevant characteristic properties $f_{\text{inv,res}}$ and $\hat{u}_{\text{sw}}$ are in between their extremes in the SI and SS states. The different waveforms in the SS and SI states are displayed in Fig. 5.

B. Coupling Link and Rectifier Behavior

The behavior and description of the coupling link and the calculation of the power transmission are based upon the following general statements.

1) Under the assumption of an ideal bridge rectifier, the current only flows to the secondary side when the rectifier is in a conducting state. If the rectifier is not in conducting state, no current flows through the coupling capacitors, and therefore, their voltage does not change. If the link input voltage changes as a result of a voltage change at the switches $u_{\text{inv,out}} = u_{\text{sw1}} - u_{\text{sw2}}$, the rectifier input voltage $u_{\text{rec.in}}$ has to follow $u_{\text{inv,out}}$. Thus, for the duration of the nonconducting states, the waveforms of $u_{\text{rec,in}}$ and $u_{\text{inv,out}}$ are identical but are set off by an individual initial value $u_{\text{rec,in,0}}$, which allows for the residing charge of the link capacitors from the previous conduction state. It differs depending on U_{out} but remains constant for each switching cycle during the steady-state operation. In the nonconducting state of the rectifier, the link behaves like in SI and during the conducting state like in SS. Therefore, power transmission can be described by a succession of both states while adhering to the varying boundary conditions.
2) The load current equals the average rectified link current charging and discharging the coupling capacitors.
3) In Fig. 6, the high-frequency equivalent circuit of the rectifier during nonconducting and conducting states is shown. Both states are equivalent to either the SI or the SS states during their valid time periods.
4) The sum of the average voltages across the coupling capacitors $\bar{u}_{\text{Ccpl,}\Sigma} = \bar{u}_{\text{Ccpl1}} + \bar{u}_{\text{Ccpl2}}$ is zero as the mean of $u_{\text{inv,out}}$ is zero. The difference in potential between the primary side and the secondary side does not influence the operation of the converter and is automatically eliminated during the summation. The individual link capacitor voltages $u_{\text{Ccpl1/2}}$ split the sum $u_{\text{Ccpl,}\Sigma}$ along the values of the link capacitors like in a series connection.

As before, only the first half of a switching period is discussed. Two cases need to be set apart as different conduction phases arise depending on the output voltage. The difference in behavior is caused by $u_{\text{rec,in}}$ following $u_{\text{inv,out}}$. If the output voltage U_{out} is lower than half the peak inverter voltage $\hat{u}_{\text{inv,out}}$ not only one but two conduction phases occur each half period.

The relevant waveforms, the switch voltages $u_{\text{sw1/2}}$, the inverter output voltage $u_{\text{inv,out}}$, the link capacitor voltage sum $u_{\text{Ccpl,}\Sigma} = u_{\text{Ccpl1}} + u_{\text{Ccpl2}}$, the rectifier input voltage $u_{\text{rec,in}}$, and the currents at the inverter inductor $i_{\sigma 1}$, at the link i_{cpl}, at the switch channel i_{sw1}, at the switch capacitance i_{Csw1}, and at the switch reverse diode i_{d1} are depicted in Fig. 7 for both cases. The gate signal u_{Gsw1} is also included to hint at the ON- and OFF-states of S_1 and the complementary S_2.

At a high output voltage, if $U_{\text{out}} > 1/2 \cdot \hat{u}_{\text{inv,out}}$, there is only one conduction phase of the rectifier during each half period [see Fig. 7(a)]. At the beginning of the examined half period starting with an interval 1_{SI}, S_1 switches OFF, and u_{sw1} rises. The rectifier is in a nonconducting state. The inverter voltages and currents have been previously discussed. $u_{\text{rec,in}}$ follows, only set off by the charge left in the link capacitors from the previous conduction phase. The initial value of $u_{\text{rec,in}}$ at the beginning of the interval under consideration is $u_{\text{rec,in,0}}$. As soon as the conduction condition of the rectifier is reached ($u_{\text{rec,in}} = U_{\text{out}}$, beginning of interval 1_{SS}), $i_{\sigma 1}$ charges not only C_{sw1} but also $C_{\text{cpl,}\Sigma}$ until $L_{\sigma 1}$ and $L_{\sigma 2}$ are demagnetized. $i_{\sigma 1}$ is divided along the C_{sw}-C_{cpl}-ratio, as both

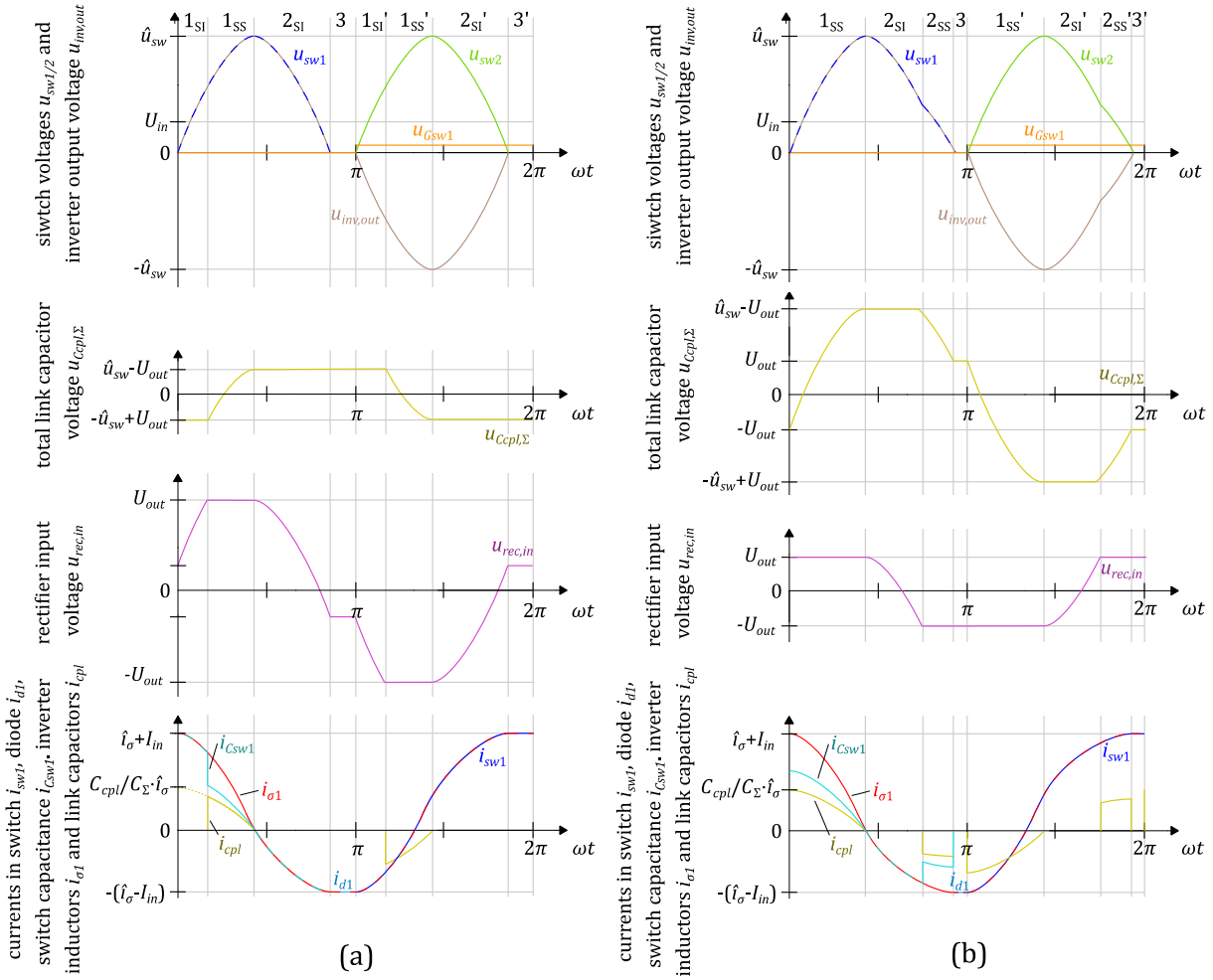

Fig. 7. Theoretical waveforms for the switch voltages $u_{\mathrm{sw1/2}}$, the inverter output voltage $u_{\mathrm{inv,out}}$, the link capacitor voltage $u_{\mathrm{Ccpl,\Sigma}}$, the rectifier input voltage $u_{\mathrm{rec,in}}$ and the currents in the switch i_{sw1}, the switch diode i_{d1}, the switch capacitance i_{Csw1}, the inverter inductor $i_{\sigma1}$, and the link capacitors i_{cpl} for one switching cycle in the case of (a) $U_{\mathrm{out}} > 1/2 \cdot \hat{u}_{\mathrm{inv,out}}$ and (b) $U_{\mathrm{out}} < 1/2 \cdot \hat{u}_{\mathrm{inv,out}}$.

capacitances act as in parallel. The rectifier stops conducting at the beginning of interval 2_{SI}, as i_{cpl} becomes zero, and the maximum charge of $C_{\mathrm{cpl},\Sigma}$ is reached with $\hat{u}_{\mathrm{inv,out}} - U_{\mathrm{out}}$. During interval 2_{SI}, C_{sw} is discharged in the same way as previously discussed for the inverter at SI. As no further conduction state occurs for the rest of the discussed half period, and $u_{\mathrm{inv,out}}$ drops from $\hat{u}_{\mathrm{inv,out}}$ to 0, $u_{\mathrm{rec,in}}$ follows from U_{out} to $U_{\mathrm{out}} - \hat{u}_{\mathrm{inv,out}}$. This voltage difference equals the (negative) dc offset of $u_{\mathrm{Ccpl,0}}$ at the beginning of the next half period. The initial state of $u_{\mathrm{rec,in}}$ at the beginning of a half period is, therefore, $u_{\mathrm{rec,in,0}} = \hat{u}_{\mathrm{inv,out}} - U_{\mathrm{out}}$. Interval 3 is identical to the free-wheeling state described before.

If $U_{\mathrm{out}} < 1/2 \cdot \hat{u}_{\mathrm{inv,out}}$, a second conduction phase additional to 1_{SS} arises during interval 2 in Fig. 7(b). The rectifier input voltage $u_{\mathrm{rec,in}}$, which tracks the changes of $u_{\mathrm{inv,out}}$ while the rectifier is nonconducting, reaches the opposite conduction boundary $-U_{\mathrm{out}}$. The rectifier becomes conducting for a second time within the same half period. Therefore, interval 2 needs to be divided into a nonconducting (2_{SI}) and a conducting phase (2_{SS}). The coupling capacitors are depleted from $\hat{u}_{\mathrm{inv,out}} - U_{\mathrm{out}}$ to U_{out} at the end of interval 2_{SS}. Because of this discharging, the conduction condition is already reached with $u_{\mathrm{rec,in,0}} = U_{\mathrm{out}}$ at the beginning of the next half period, and interval 1_{SI} is eliminated.

As, with a rising U_{out}, the conduction durations become shorter and the SI state dominates, the duration of the free-wheeling state increases, and with that, the peak inverter voltage $\hat{u}_{\mathrm{inv,out}}$ to maintain $\bar{u}_{\mathrm{sw1}} = \bar{u}_{\mathrm{sw2}} = U_{\mathrm{in}}$. $\hat{u}_{\mathrm{inv,out}}(U_{\mathrm{out}})$ can be approximated through linear interpolation between $\hat{u}_{\mathrm{inv,out,min}}$ and $\hat{u}_{\mathrm{inv,out,max}}$ or calculated through an iterative waveform evaluation, as described in Section III-C. This concludes the theoretical behavior of the converter and is the basis for the following calculation model.

C. Calculation Model

Although a design estimation based on (1) and the characteristic properties of Table I would be sufficient to build a functioning converter, a detailed calculation model is beneficial to gain insights into the load, power, and loss characteristics, as well as into optimization strategies of the converter and its design. The switch voltages $u_{\mathrm{sw1/2}}$ and the inductor currents $i_{\sigma1/2}$ can be calculated in the time domain as a sequence of the previously described time intervals. The differential

equation valid for the respective equivalent network of $C_{\mathrm{sw1/2}}$, $C_{\mathrm{cpl},\Sigma}$, and $L_{\sigma 1/2}$ is solved under consideration of the specific characteristic properties of each interval and the boundary conditions of each transition within one-half of a switching period. Again, assuming symmetry, calculating only one half of a switching period is sufficient, as the same waveforms arise in the other branch during the other half period. The following description applies to the half in which S_1 is switched OFF. An iterative solver is necessary to reach the condition for $\bar{u}_{\mathrm{sw1}}$ and, therefore, the correct value of $i_{\sigma 1}(0)$ at the beginning of a switching period. As seen in Fig. 4, the equivalent networks are passive, nondampened networks and can all be represented by the same differential equation for $i_{\sigma 1}$

$$-\frac{\delta^2 i_{\sigma 1}}{\delta t^2} = \omega^2 i_{\sigma 1}. \tag{3}$$

The effective resonant frequency ω for the nonconducting state (intervals 1_a and 2_a), the conducting state (intervals 1_b and 2_b), and the freewheeling state (interval 3) is

$$\omega = \begin{cases} 2\pi f_{\mathrm{inv,res,SI}} & 1_a, 2_a \\ 2\pi f_{\mathrm{inv,res,SS}} \quad \text{in intervals} & 1_b, 2_b \\ 0 & 3. \end{cases} \tag{4}$$

In the case of interval 3, ω is zero because both switches are conducting, thus shorting the inductors. In all cases, the equation is solved by

$$i_{\sigma 1}(t) = \hat{i} \cdot \cos\left(\omega\left(t - t^*\right)\right) \tag{5}$$

with $\hat{i}$ and t^* needing to fulfill the boundary conditions regarding the continuity of $i_{\sigma 1}$ and u_{sw1} at the transitions between the intervals of each half period. Based on $i_{\sigma 1}$, the switch current

$$i_{\mathrm{sw1}}(t) = \begin{cases} i_{\sigma 1}(t) & 1_a, 2_a, 3 \\ \frac{C_{\mathrm{sw1}}}{C_{\mathrm{sw1}} + C_{\mathrm{cpl},\Sigma}} i_{\sigma 1}(t) \quad \text{in intervals} & \\ & 1_b, 2_b \end{cases} \tag{6}$$

and the link current

$$i_{\mathrm{cpl}}(t) = i_{\sigma 1}(t) - i_{\mathrm{sw1}}(t) \tag{7}$$

can be derived, and the switch voltage

$$u_{\mathrm{sw1}}(t) = \frac{1}{C_{\mathrm{sw1}}} \int i_{\mathrm{sw1}}\left(t'\right) dt' + u_{\mathrm{sw1,0}} \tag{8}$$

can be calculated. A given output voltage U_{out} is needed to define the boundary conditions. The output power then is

$$P_{\mathrm{out}} = \mathrm{U}_{\mathrm{out}} \cdot |\bar{i_{\mathrm{cpl}}}|. \tag{9}$$

If the output voltage for a given load resistance R_L is to be calculated, an additional iteration for the output voltage U_{out} is necessary, until U_{out} and the calculated output current fit the given R_L.

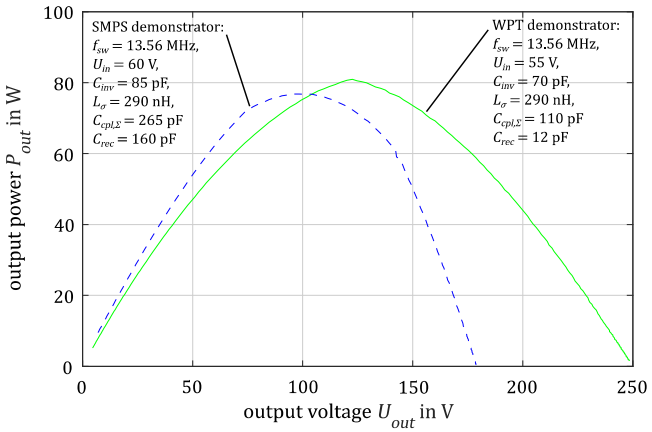

Fig. 8. Output voltage and power transfer characteristics calculated by the model for the designs of the demonstrators, including the influence of the rectifier capacitance.

D. Operating Behavior and Strategies

To find a suitable operating point, the output voltage, power, and load characteristics need to be considered. Fig. 8 shows the output power to output voltage curves exemplarily for the two designs later presented in the experimental verification section. The maximum power output is reached in a matched state between the reactance of the coupling capacitance and the resistance of the load in the same way as described for the general model in Section II. The general model predicts the shape of the characteristic curve and the magnitude of the transmitted power compared to the exact modeling of the converter waveforms quite well. As previously mentioned, operation in the SI and SS states is possible. Starting from the maximum power point, the output voltage sinks with a reduced load resistance, thus reducing the output power. For SS, a maximum output current limit exists. The behavior of the converter is similar to a current source. When increasing the load resistance, again starting from the maximum power point, the output power decreases as well. At SI, the output voltage reaches its maximum. The converter approximates voltage source behavior near SI.

A further evaluation of the characteristic properties of the inverter is of interest. The peak semiconductor voltage stress, which is present at idle, is calculated by

$$\hat{u}_{\mathrm{sw,max}} = \pi U_{\mathrm{in}} \cdot \frac{f_{\mathrm{inv,res,SI}}}{f_{\mathrm{sw}}} \tag{10}$$

and the maximum free-wheeling duration by

$$\frac{t_{\mathrm{FW,max}}}{T} = 1 - \frac{f_{\mathrm{sw}}}{f_{\mathrm{inv,res,SI}}} \tag{11}$$

with

$$\frac{f_{\mathrm{inv,res,SI}}}{f_{\mathrm{sw}}} = \frac{f_{\mathrm{inv,res,SI}}}{f_{\mathrm{inv,res,SS}}} = \sqrt{1 + \frac{C_{\mathrm{cpl},\Sigma}}{C_{\mathrm{sw}}}}. \tag{12}$$

Fig. 9 shows the dependencies of the maximum free-wheeling time and the peak switch voltage to input voltage ratio relative to the ratio of the switch capacitance $C_{\mathrm{sw1/2}}$ and the link capacitance $C_{\mathrm{cpl1/2}}$. The listed parameters are a measure of how the waveforms for SI and SS states, as presented

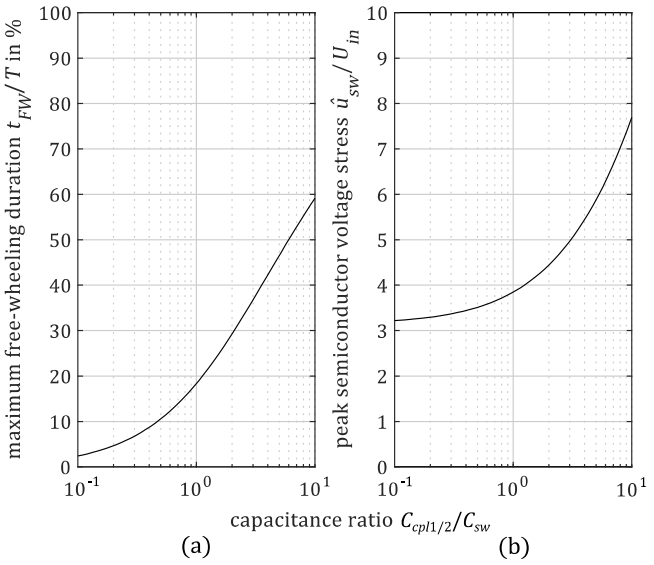

Fig. 9. (a) Maximum free-wheeling duration and (b) peak semiconductor steady-state voltage stress at the SI state when designed for the SS condition.

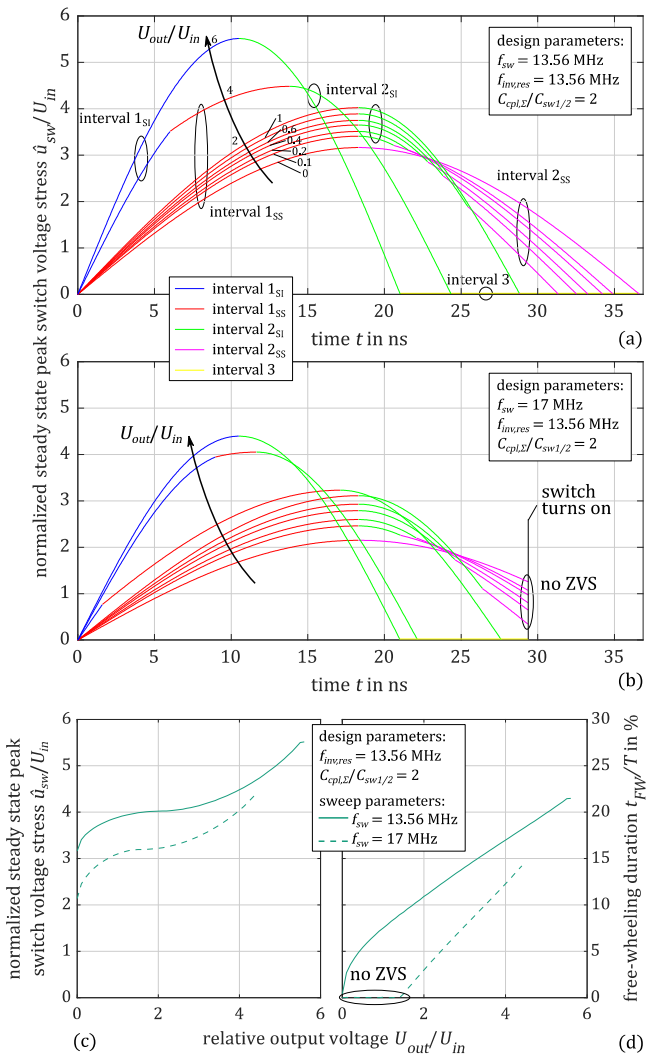

Fig. 10. Inverter voltage waveforms for (a) design for the complete load range and (b) limited output voltage range. (c) Peak switch voltages and (d) free-wheeling duration for both designs across the output voltage range.

in Fig. 5, differ from each other. The graphics are valid for a converter that is designed for the complete load range. While, following (1), a rise in C_{cpl} may increase the output power, the maximum peak switch voltage at SI also climbs. To not exceed the voltage limitations of the semiconductor, either the C_{cpl}-C_{sw}-ratio or the output voltage range should be limited, and therefore, the maximum semiconductor stress can be reduced. It is advisable to also reduce the free-wheeling duration t_{FW} (previously time interval 3) to avoid reverse conduction losses of the switches. A design with a limited output voltage range and an increased efficiency can either be reached through tuning of a design approximation based on (1) and (2) and Table I or through precise time-domain modeling, as described in Section III-C.

An increase in efficiency can be achieved by limiting the output voltage range by $U_{\text{out}} > U_{\text{out,min}}$, thus deviating from the initial design criterion $f_{\text{inv,res,SS}} = f_{\text{sw}}$ of the inverter of Section III-A. To avoid redesigning the converter, going forward, the switching frequency is altered. In all following cases, the converter is always operated in a fixed frequency and fixed duty cycle mode. Improvements to the converter efficiency through dynamic adjustment of the switching frequency or the duty cycle seem possible but require a different, more complex driving circuitry. The goal might be achieved using resonant inverters with autonomous control of the switches. Such circuits have been discussed elsewhere [39], [40] and shall, therefore, not be within the scope of this article. The inverter waveforms and characteristics for a full operating range design and a limited operating range design are presented in Fig. 10. They differ from each other only by the switching frequency. In Fig. 10(a), a design following the criteria of Section III-A is shown, while, for Fig. 10(b), the same component values are used, and the switching frequency is increased by 25%. The different intervals, as introduced in Sections III-A and III-B, are labeled and marked by color. If operated as in Fig. 10(a), the complete output voltage range is permissible. In the case of Fig. 10(b), for low $U_{\text{out}}/U_{\text{in}}$ values, ZVS is not achieved. Therefore, $U_{\text{out}} < U_{\text{out,min}}$ should be avoided (in the case of Fig. 10(b), $U_{\text{out,min}} \approx 1.5 \cdot U_{\text{in}}$). While this is unproblematic for transient events, continuous operation is inefficient in these operating points.

The semiconductor voltage stress, the free-wheeling time [see Fig. 10(c) and (d)], and the semiconductor reverse conduction losses increase with the output voltage but are reduced for the limited output voltage design. In the case of the original design criterion, in a fixed output voltage application, the efficiency is not as high as it could be because of the reverse conduction losses. If the switching frequency is raised (or the resonant frequency of the inverter lowered), the free-wheeling time for an intended output voltage can theoretically be reduced to zero, yielding the elimination of reverse conduction of the switches and the corresponding losses, higher efficiency, and lower semiconductor voltage stress at the cost of lost ZVS operation at output voltages lower than a minimum voltage and lower power output as

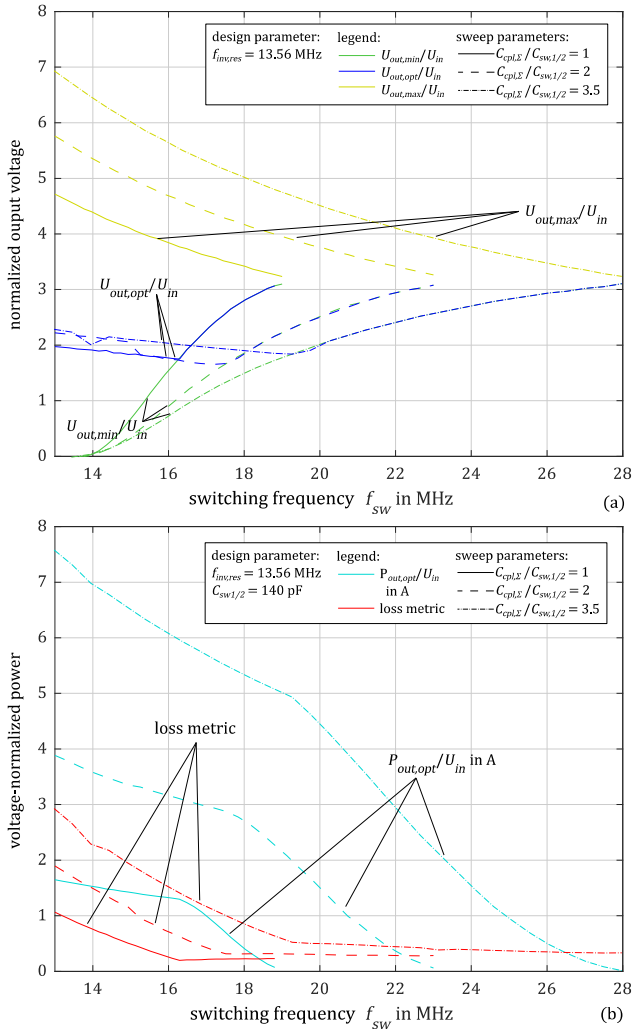

Fig. 11. Effects of limitation of the output voltage range through increase of the switching frequency on (a) peak switch voltage, minimum output voltage under ZVS criterion, and voltage at peak power and on (b) peak power and losses.

a direct result of the lower inverter peak voltage at the same load.

The mechanism between f_{sw} and the load range, as described in Fig. 10, is used to optimize the system design. Fig. 11 evaluates the system behavior for an operation of the same design at different f_{sw}'s. Fig. 11(a) shows the minimum permissible output voltage $U_{\mathrm{out,min}}$ below which the converter loses the ZVS operation. The maximum output voltage $U_{\mathrm{out,max}}$ is the output voltage at idle. The optimal output voltage $U_{\mathrm{out,opt}}$ is the voltage at which the converter reaches its maximum output power within the permissible range of U_{out}. The converter is designed for $f_{\mathrm{inv,res}} = 13.56$ MHz. Fig. 11(b) depicts the related output power at $U_{\mathrm{out,opt}}$ and a loss metric that is based on the data sheet of a GaN Systems GS-065-011-1-L GaN enhancement mode HEMT and represents the trend of the conduction losses. With a rising f_{sw}, $\hat{u}_{\mathrm{sw}}$ decreases at the same load resistance, leading to a lower $U_{\mathrm{out,opt}}$ and a reduced $P_{\mathrm{out,opt}}$. Losses are reduced disproportionally so that the inverter operation becomes more efficient. If $U_{\mathrm{out,opt}}$ and $U_{\mathrm{out,min}}$ meet, and f_{sw} is increased further, $U_{\mathrm{out,opt}}$ exits

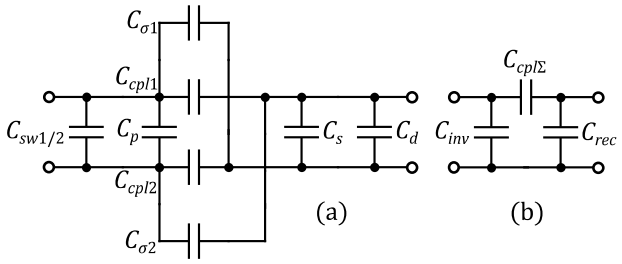

Fig. 12. (a) Parasitic elements of the coupling link. (b) Equivalent circuit.

the point of peak power in the transfer characteristics curve (see Fig. 8) because it is not within the permissible load range. The output power is greatly reduced while losses stay approximately constant for the permissible optimum at the given f_{sw}. Therefore, the most efficient operating point is reached when $U_{\mathrm{out,opt}}$ and $U_{\mathrm{out,min}}$ first join with each other. The greater the C_{cpl}-C_{sw}-ratio, the more the inverter waveforms vary, and the larger is the increase in f_{sw} before the most efficient point is reached.

E. Practical Operation Considerations

Practical applications usually require some kind of voltage or current control. An ON/OFF control (OOC), as used for a similar topology in [47], is proposed to realize a controlled operation of the discussed system. It is suitable and applicable because, at a sufficiently constant output voltage, only L_{dc} can cause transient oscillations. These settle quickly, and only the first pulse misses the soft switching condition. An OOC with a duty cycle D reduces the effective load resistance to

$$R_{\mathrm{Leff}} = D \cdot R_L \tag{13}$$

which can now be entered into the model presented in Section III-C. An applied OOC will be presented later in Section IV.

Among the parasitic effects, which are the losses and nonlinearity of the switches, the resistance of the inductors, the inductance of the coupling link, and all parasitic capacitances, the critical parasitics of the proposed topology are the capacitive properties of the rectifier input and any cross capacitances. The inverter switch capacitance, any cross-coupling between the two links, and the parasitic rectifier capacitance can all be integrated into the parasitic circuit, which can be further simplified to a π-equivalent circuit as a general model for the parasitic behavior of the coupling link, as shown in Fig. 12 and described in [48]. The main component of C_{inv} is per design C_{sw} of the currently turned-OFF switch. Any deviations and parasitics (C_p) may alter the design of the inverter, which, to a moderate degree, can be tolerated because of the free-wheeling state or incorporated into the converter design. A parasitic increase of $C_{\mathrm{cpl}\Sigma}$ has no negative consequences. The components of C_{rec} are the parasitic secondary capacitance C_s of the coupling link and the rectifier and diode capacitance C_d.

C_{inv} and $C_{\mathrm{cpl}\Sigma}$ are integral parts of the operation of the converter and can be directly entered into the quantitative model from Section III-C. Lost power caused by C_{rec} can be

covered by a minor model extension. A part of the link current i_{cpl} charges and discharges C_{rec} to the amount of

$$q_{\mathrm{rec}} = 2U_{\mathrm{out}}C_{\mathrm{rec}} \tag{14}$$

during each switching period. It is, therefore, not available for the output current and reduces the effective output current at a given output voltage to

$$\bar{i}'_{\mathrm{out}} = |\bar{i_{\mathrm{cpl}}}| - q_{\mathrm{rec}} \cdot 2f_{\mathrm{sw}} \tag{15}$$

which can then be entered into (9).

Other parasitic effects with only a minor influence are the stray inductances in the coupling link, parameter variations in the inverter inductors, switches, and coupling capacitors, as well as operating point variations of the load and during transient processes. The stray inductances in the coupling link cause a high-frequency ripple on the coupling link current, but their influence on the power transfer is limited as long as their resonant frequency with $C_{\mathrm{cpl}\Sigma}$ is large compared to f_{sw}. The parameter variations are of no concern as they are adjusted for during the free-wheeling state. Especially variations in the coupling capacitor do not lead to a grave power loss, as the transmitted power is in good approximation proportional to the coupling capacitance and does not depend on the correct excitation of a resonance.

IV. Experimental Verification

The proposed topology is implemented as an SMPS using ceramic capacitors as the capacitive coupling interface and as a WPT system. The systems are based around the link capacitance values, which are chosen after (1) and (2) so that output power of more than 100 W can be reached at input voltages of up to 80 V. The effective total link capacitances $C_{\mathrm{cpl},\Sigma}$ are 265 pF (SMPS) and 110 pF (WPT). For the SMPS, a larger capacitance is chosen to investigate the influence of the C_{sw}-C_{cpl}-ratio. The WPT system uses a custom-designed capacitive coupler built from 10×10 cm^2 copper plates with about 1 mm of paper as an isolation barrier in between. The capacitance of the WPT coupler can be varied by adding or removing layers of paper. The inverter inductances are calculated following the presented models in [49] and verified through measurement. The SMPS converter board, as depicted in Fig. 13(a), is sized 10×8 cm^2, including the logic circuitry, TI's LM5114 drivers, the inverter, the link, and the rectifier with the power section occupying about half of the board. The inverter board of the WPT demonstrator, as shown in Fig. 13(c), is sized 11×9.5 cm^2 with all power components placed on a quarter of the board. The dimensions of the rectifier board are 5×2.5 cm^2 and include the footprint of a common mode choke. The driving signal is created externally. Table II gives an overview of the used power components, and Table III presents the design parameters.

Among the differences between the two demonstrators are the GaN HEMTs, the coupling interfaces, and the layout. Different switches were used to reduce their ON-resistance and with that permit higher inverter currents at the same amount of inverter losses. A WPT coupler connected by braided wires replaces the ceramic link capacitors and the inductance-optimized layout of the SMPS demonstrator. The coupling capacitance is reduced, as well as parasitic rectifier capacitances resulting from the layout, whereas the link inductances are increased because of the increased length of the connecting wires to the coupler.

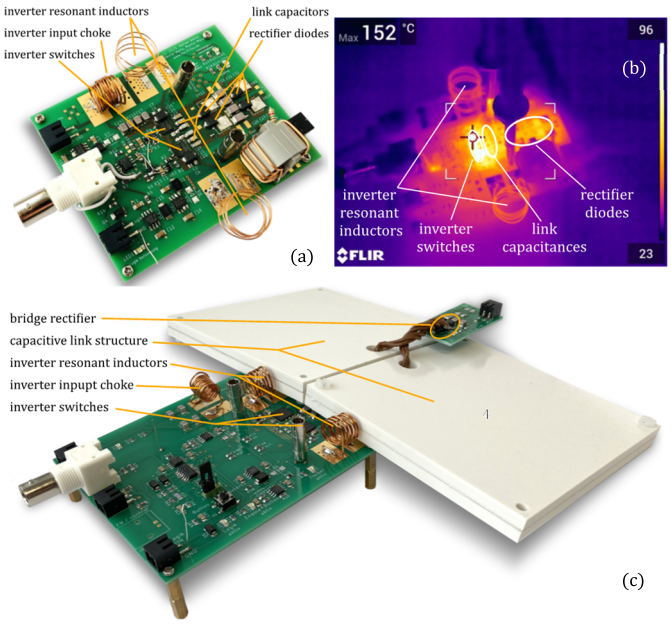

Fig. 13. (a) SMPS and (c) WPT demonstrators. (b) FLIR imaging for OP1.

A. Waveforms

Fig. 14 shows the characteristic waveforms of the SMPS demonstrator at operating point OP3. The rectifier input voltage is obtained by calculating the difference between the two rectifier inputs in reference to the primary side ground. The inverter and link currents are estimated by integrating the inductor voltage and differentiating the coupling capacitor voltage.

The measured switch voltages match the waveforms predicted by the theoretical analysis and obtained from the calculation model well, albeit with a minor ripple during the rising edge. Similar observations can be made for the rectifier input voltage and the link capacitor voltages. The inverter currents, which are calculated from the inductor voltages, are similar to the expected waveforms, and only a small deviation is visible in the inverter currents due to an oscillation between the input choke and the resonant inductors. The vertical current edge predicted for the coupling link is distorted and excites parasitic oscillations together with the parasitic link inductance. Although these are mainly visible in i_{cpl}, which is obtained by mathematically differentiating the capacitor voltages, thus possibly amplifying the current distortion, they also spread to the inverter and rectifier voltage waveforms, where a voltage ripple can be observed. The oscillations are of no harm to the power transfer ability of the system. The routing on the PCB of the SMPS demonstrator board is intended to achieve a lower parasitic link inductance compared to the WPT demonstrator. The resulting proximity of the conductors leads to an increased parasitic capacitance between them, which,

TABLE II
MAIN POWER COMPONENTS

Component	SMPS demonstrator	WPT demonstrator
Switch	GaN Systems GS-065-011-1-L 650 V GaN HEMT	Infineon IGLD60R190D1AUMA 650 V GaN HEMT
Coupling link	Yageo C0G multi-layer ceramic capacitors	Structure with copper plates (10 × 10 cm^2) and paper as spacer (1 mm)
Antiparallel diodes	GeneSiC GB01SLT06-214 650 V SiC Schottky Diode	GeneSiC GB01SLT06-214 650 V SiC Schottky Diode
Rectifier diodes	GeneSiC GB01SLT06-214 650 V SiC Schottky Diode	GeneSiC GB01SLT06-214 650 V SiC Schottky Diode

TABLE III
DEVICE VALUES

Component	SMSP demonstrator	WPT demonstrator
Total Switch Capacitance C_{sw1}, C_{sw2}	85 pF	70 pF
⌞ Switch effective output capacitance*	60 pF	50 pF
⌞ Antiparallel Diodes*	10 pF	10 pF
⌞ Parasitic capacitance°	15 pF	10 pF
Switch on-resistance $R_{ds(on),1}, R_{ds(on),2}$* (@25°C; 150°C)	150 mΩ / 380 mΩ	140 mΩ / 260 mΩ
Inverter input choke L_{DC}°	712 nH	602 nH
Inverter resonant inductors $L_{\sigma1}, L_{\sigma2}$°	326/309 nH	320/300 nH
Coupling capacitors $C_{cpl,\Sigma}$°	265 pF	110 pF
Parasitic link inductances* $L_{cpl,\Sigma}$	20 nH	180 nH
Total rectifier capacitance C_{rec}	160 pF	12 pF
⌞ Diode capacitance*	10 pF	10 pF
⌞ Parasitic capacitance°	150 pF	2 pF

* = estimated / from datasheet; ° = measured / modelled

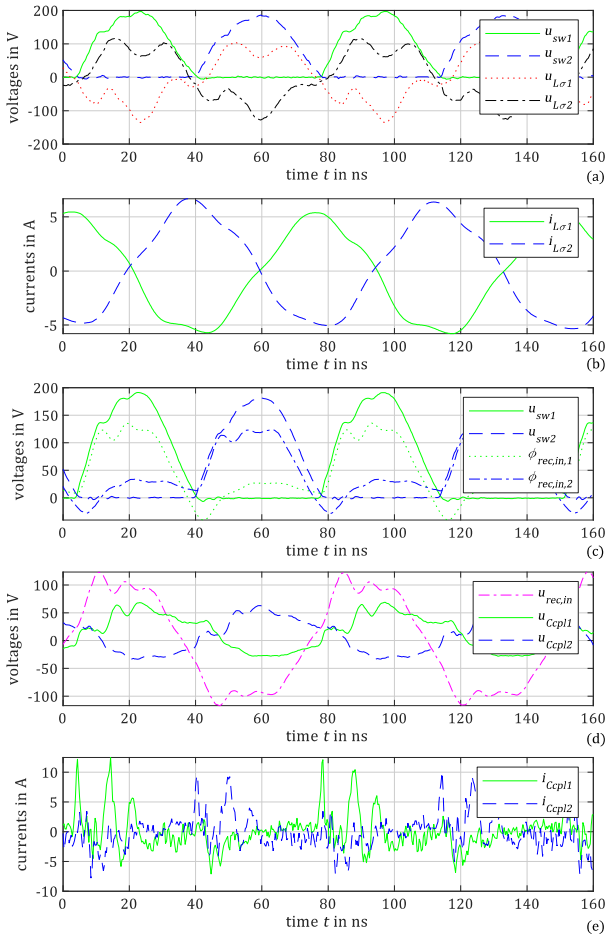

Fig. 14. Measured characteristic waveforms for the SMPS demonstrator at OP3: (a) inverter voltages, (b) resonant inductor currents, (c) rectifier input potentials, (d) link voltages, and (e) link currents.

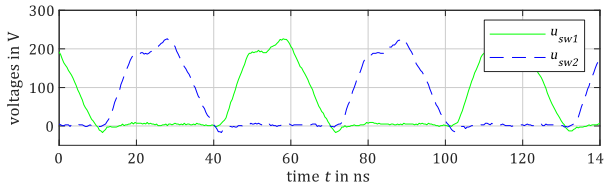

Fig. 15. Switch voltages for the WPT demonstrator at OP5.

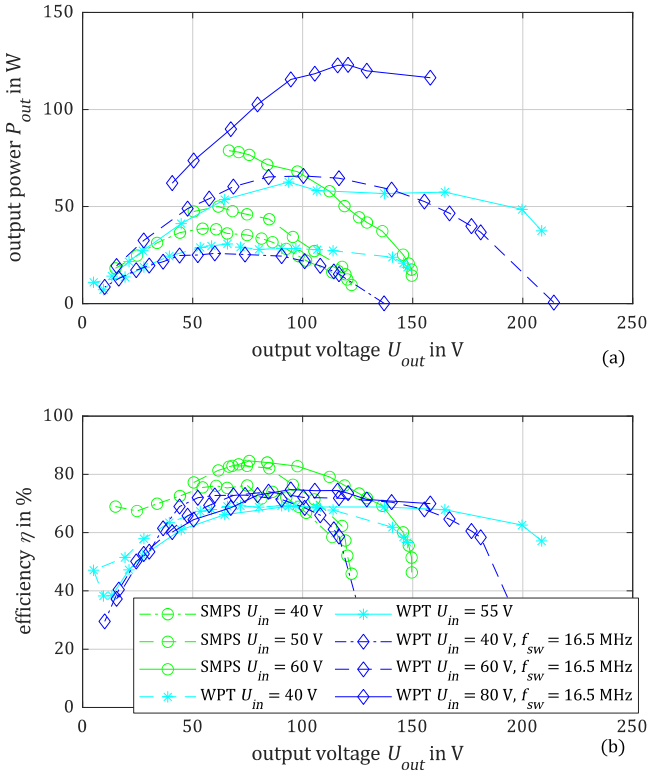

Fig. 16. Measured (a) output power and (b) efficiency across the load range for both demonstrators.

in its turn, enlarges the effective rectifier capacitance. The increase in the value of the rectifier capacitance is estimated to amount to 150 pF, thus reducing the maximum output power by as much as 49% at the given design parameters, according to the calculation model.

The inverter voltage waveforms of the WPT demonstrator can be seen in Fig. 15. The voltages at the inverter switches show a significant parasitic oscillation, which, indeed, is more severe than at the SMPS demonstrator but still does not negatively influence the power transfer. On the other hand, new positive development can be observed. The switch voltage waveforms are deformed in a manner similar to that known

TABLE IV
OPERATING POINTS

Operating points	f_{sw}	U_{in}	R_{out}	U_{out}	P_{out}	η
OP1 (SMPS)	13.56 MHz	75 V	139 Ω	127.1 V	115.9 W	82.1 %
OP2 (WPT)	16.5 MHz	80 V	118 Ω	120.6 V	122.9 W	73.6 %
OP3 (SMPS)	13.56 MHz	60 V	139 Ω	99.7 V	71.6 W	81.4 %
OP4 (SMPS)	13.56 MHz	60 V	139 Ω / 330 Ω	99.1 V / 129.5 V	70.7 W / 50.8 W	82.4 % / 74.8 %
OP5 (WPT)	16.5 MHz	65 V	139 Ω / 330 Ω	95.7 V / 142.2 V	65.87 W / 61.2 W	72.2 % / 69.7 %

from Class ϕ_2 inverters [34], thus reducing the peak inverter voltage. This property depends on the converter load and output voltage and is, therefore, specific to certain operating points. If operation in such points can be ensured, a reduced semiconductor voltage stress compared to other resonant inverters, e.g., Class E-inverters, can be realized.

B. Power, Voltage, and Load Characteristics and Losses

Fig. 16 shows the output power to voltage transfer curves of both demonstrators for the same designs from Table III but at different operating points. The curves match the expectations from the theoretical analysis well. The characteristic parabolic curve is visible. Maximum power is reached near the theoretical optimal load resistance calculated by (2) at $R_L = 44\ \Omega$ (SMPS) and $R_L = 106\ \Omega$ (WPT). Power only varies by 15% in the load ranges of $R_L \approx 40, \ldots, 150\ \Omega$ (SMPS) and $R_L \approx 70, \ldots, 400\ \Omega$ (WPT). The lost power is approximately constant across the complete load range, as losses are mainly caused by circulating currents in the inverter. Losses increase in operating points with a longer free-wheeling duration or, especially, when ZVS is lost. As the converters are designed to achieve a low free-wheeling duration while maintaining ZVS near the optimum load condition, the efficiency of the converters peaks at or near the maximum power point. The efficiency of the SMPS demonstrator is higher because of the more favorable C_{sw}-C_{cpl}-ratio. The maximum achieved powers for the SMPS and WPT demonstrators are displayed in OP1 and OP2 in Table IV.

The dependence of parameter variations, especially in the link capacitance, is examined by adding or removing layers of paper in the WPT coupler. A variation in $C_{\text{cpl},\Sigma}$ within the range of $67, \ldots, 188$ pF is investigated. Considering the results from Section II, it is expected that the output power varies linearly with the effective link capacitance. As previously discussed, the inverter losses stay approximately constant. The measurements in Fig. 17 validate the expected behavior.

The thermal imaging of the SMPS demonstrator, as presented in Fig. 13(b), identifies the inverter switches as hot spots. A rise in temperature is also observed for the inverter inductors and the rectifier diodes. The loss distribution is estimated by recreating the thermal footprints for central components in Fig. 13(b). The power, which is needed for the components to reach the respective temperatures observed at OP1, serves as an approximation for the losses during normal operation. The dc currents are induced into the switches, the

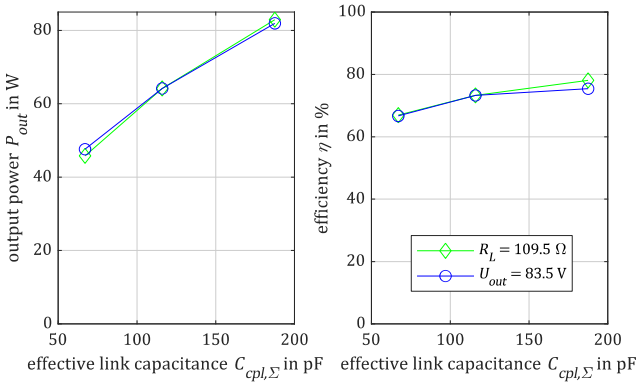

Fig. 17. (a) Power and (b) efficiency for a variation in the total link capacitance $C_{\text{cpl},\Sigma}$.

inductors, and the diodes. Due to the distance of the components and forced ventilation, the impact of heat spreading and, therefore, interdependence between the temperatures of the switches, the inductors, and the rectifier diodes can be neglected. The results, as shown in Table V, confirm the prediction that the inverter switches are a major source of losses. They are the consequence of the relatively high ON-state resistance $R_{\text{ds(ON)}}$ of the used switches. At 150 °C, the $R_{\text{ds(ON)}}$ value rises to more than twice the data sheet value at room temperature, further increasing the losses. The circulating currents, needed to achieve ZVS and reduce the link and load dependence of the inverter, cause significant parts of the conduction losses in the inverter. The resistance of the inverter inductors and the forward voltage of the rectifier diodes add additional losses. Together, they comprise the majority of the losses. The losses caused in connectors, power supply cables, capacitors, traces, and the input choke sum up to the losses unaccounted for in Table V. No significant lost power is expected and can be identified in the link capacitors.

C. Control

To reduce the dependence of U_{out} and P_{out}, in Section III-E, an OOC has been introduced. Fig. 18 presents the switch voltage waveforms and their transient variations, while the system is switched ON and OFF at $f_{\text{OOC}} = 500$ kHz. Fig. 18 includes the OOC input signal. When inactive, both switches are turned OFF. Otherwise, both alternate in the respective f_{sw} identical to the uncontrolled steady-state operation. Fig. 18(a) illustrates a more detailed view, whereas

TABLE V
LOSS DISTRIBUTION

	Absolute [W]	Percentage [%]
Both inverter switches	11.6	49%
Both inverter inductors	4.0	17%
All four rectifier diodes	5.5	23%
Unaccounted for	2.6	11%
Total losses	23.7	100%

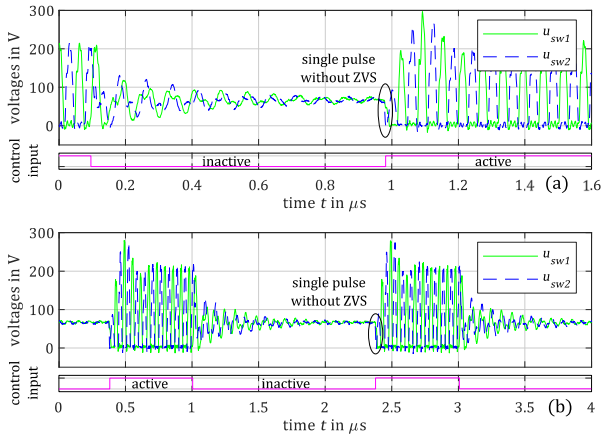

Fig. 18. Measured waveforms and control input for the WPT demonstrator during the OOC operation based on OP5: (a) $D = 55\%$ and (b) $D = 30\%$.

Fig. 18(b) shows a complete OOC cycle at a larger time base and for a different duty cycle. While turned ON, the system behaves similar to the continuous operation of the same system, and while turned OFF, no power is transmitted. The following observations are distinct for the OOC-operated system: The input choke causes minor transient oscillations directly after turning ON. Though the peak switch voltage may be higher directly after the switch-ON compared to the steady-state operation, only the first pulse misses the ZVS criterion. Oscillations between the switch capacitors and the inverter inductors after turn-OFF fade quickly. Compared to a continuous operation, no drop in efficiency can be observed, thus allowing an efficient controlled operation. The output voltage and efficiency in reference to the duty cycle of an OOC of both demonstrators during controlled operation are shown in Fig. 19. The parameters of the operating points OP4 and OP5 at $D = 100\%$ are listed in Table IV.

V. DISCUSSION

In CPT systems with non-resonant links, the transferrable power mainly depends on the absolute link capacitances, the input voltage, and the operating frequency. Therefore, to achieve high power, the system should be designed to operate at high link voltages and frequencies. Within the ISM bands, a base operating frequency of 13.56 MHz is chosen for the experiments performed within this article.

The power transfer and characteristic properties of the discussed topology depend on the switch capacitance and its relation to the link capacitance value. It is shown that

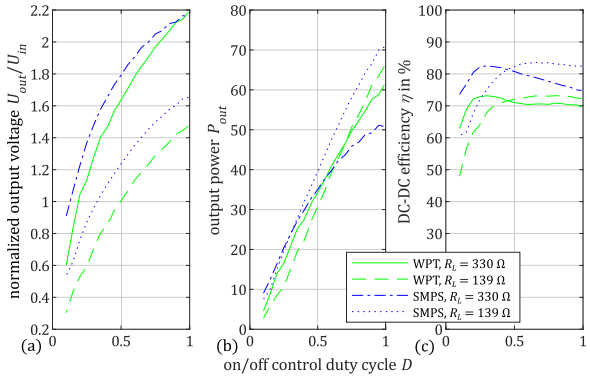

Fig. 19. Measured (a) output voltage, (b) power, and (c) efficiency under controlled operation for both demonstrators and different values for the load resistance R_L.

choosing C_{sw} smaller than C_{cpl} reduces the dependence of the inverter operation on the output voltage and link capacitance. The reduced load dependence comes at the cost of increased reactive power circulating in the inverter, which is a major contribution to the total losses of the system. As discussed in the theoretical analysis, if the output voltage range can be restricted, the inverter can be designed with C_{sw} greater than C_{cpl}, and $f_{\text{sw}} > f_{\text{inv,res,SS}}$, which improves efficiency. The same can be achieved by dynamically adjusting the operating frequency, if permissible. A main advantage of the system is that the same inductors of the inverter realize both the soft switching for the inverter switches and the current source behavior needed for directly driving the non-resonant CPT link. As a result, all inductive components in the coupling link and the rectifier are eliminated. Another consequence of the direct connection of the link capacitances to the semiconductor switches is that the operation of the converter cannot result in a link capacitor voltage greater than the switch breakdown voltage, thus defining a peak voltage stress of the link capacitors, which is practical for safety-critical applications. The free-wheeling state of the push-pull inverter makes the converter tolerant to parameter and output voltage variations though the voltage stress of the transistors rises for increasing free-wheeling durations.

The observed efficiency loss is mainly caused by the conduction losses of the inverter switches. For higher efficiency and reduced losses, semiconductor switches with low $R_{\text{ds(ON)}}$ are of great importance, but the parasitic switch capacitances increase with decreasing ON-resistance. An increase in the total switch capacitance solicits a redesign of the inverter inductors for the inverter to maintain $f_{\text{inv,res}}$. This yields a lower Z_0 and, therefore, increasing inverter currents. The same current increase can be observed when the system is designed for a higher operating frequency at a given switch capacitance. Therefore, the operating frequency is limited by the switch properties, namely, their capacitance and their current capability. The design in the experiments comes close to this limit. Significant losses arise during the free-wheeling state because of the poor reverse conduction characteristics of GaN HEMTs with a high forward voltage. For a better loss distribution, the presented demonstrators use antiparallel

TABLE VI
COMPARISON

Publication	Link Type	Inverter Type	U_{in} [V]	P_{out} [W]	η [%]	f_{sw} [MHz]	$C_{cpl,\Sigma}$ [pF]	Σ(L) [nH]	Component count	$\frac{P_{out}/U_{in}}{C_{cpl,\Sigma}}\left[\frac{W}{V\cdot nF}\right]$
[34]	Non-resonant*	HF-SEPIC	3.6	3	81	20	1270	63	8	0.656
[51]	Non-resonant*	HF-SEPIC	162.5	140	90	10	340	1160	7	2.54
[52]	DC block*	Class Φ_2	50	277	80	6.78	4620	2000	19	1.19
This work	Non-resonant*	Series-resonant push-pull	75	122.9	73.6	16.5	120	1200	11	13.7
[50]	Resonant (LC + LCL matching network)	Full bridge	100	774	81	13.56	1.35	11310	15	5733
[53]	Resonant (2x LC matching network)	Full bridge	60	150	66.7	1.5	2.8	173600	14	892

*non-resonant meaning the link does not obtain a distinct resonant network. The link capacitors may implement a DC decoupling or the realization of the power transfer may depend on the interaction between the non-resonant link and a resonant inverter topology.

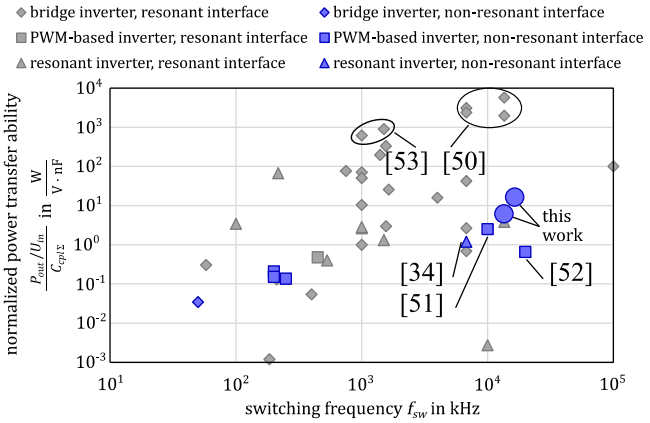

Fig. 20. This work and previously published converters compared for normalized power transfer ability.

Schottky diodes, which need to take over the current only for a few nanoseconds. As they are not connected sufficiently close to the switch, the very fast succession of commutations of the current from the switch capacitance to the diode and back to the switch channel is not handled as efficiently as possible. Better reverse conduction properties or an improved control, which activates the switches while reverse conducting, would be beneficial.

Further advantages of the proposed topology are the avoidance of high side switches, a fast transient response, and maintained ZVS under the OOC operation. Parasitic inductances in the coupling link have no significant influence on the power transfer if their resonant frequency with the link capacitors is sufficiently larger than the switching frequency.

Table VI and Fig. 20 are presented to compare the topology proposed in this article against previously published systems. CPT systems are usually compared for their ability to transfer power across a certain capacitance [34], [54]. To achieve comparability, we normalize the transferred output power not only to the link capacitance but also to the input voltage, as more power can be transferred at a higher input voltage. Fig. 20 arranges multiple previously published systems with a resonant and a non-resonant capacitive link for comparative purposes. Competitive systems with a non-resonant link are marked and entered in Table VI for a more detailed overview. The most advanced systems with a resonant link are also marked and included in Table VI for reference purposes. Though the normalized power transfer to link capacitance may be higher for topologies incorporating a resonant coupling link, most require an extensive amount of additional inductive components. Among CPT topologies with a non-resonant link, the work presented in this article reaches the highest input voltage-normalized power transfer to link capacitance value of 13.7 W/(nF·V).

VI. CONCLUSION

In this article, we deployed a push-pull resonant inverter to directly drive a non-resonant CPT interface. By driving such a capacitive link directly from an HF inverter and by integrating the capacitors into the core operation of the converter, the issue of only a low power transfer ability of a non-resonant CPT system as a result of either a low operating frequency ability or unnecessarily large coupling capacitor values is mitigated. The inverter is easy to design and tolerant of parameter and operating point variations. A further benefit comes from the total elimination of all inductive components in the coupling link and the rectifier, especially in comparison with resonant CPT links. We achieve the highest normalized power transfer ability compared to previously published circuits with a non-resonant CPT link. In this article, the behavior of the proposed system is described, mathematically modeled, evaluated, and experimentally verified. Using the presented converters, the transfer of 122.9 W across an effective link capacitance of 120 pF can be achieved. With the proposed topology, we enhance the applicability of non-resonant CPT.

Future work may include the characterization of a modified topology with, e.g., an eliminated input choke or the integration of the inverter inductors into a transformer. Another interesting prospect is the optimization of the link inductance to reduce the switch voltage stress based on the observed effects in this article. We will also gain insights into applications, e.g., the charging of UAVs.

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Adrian Amler received the B.Sc. and M.Sc. degrees in electrical and electronics engineering and information technology from the Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany, in 2019 and 2021, respectively, where he is currently pursuing the Ph.D. degree with the Institute of Power Electronics.

Since 2021, he has been with the Institute of Power Electronics, FAU. His research interests include capacitive coupling, wireless power transfer, wide bandgap devices, and converter and drive technologies.

Nikolai Weitz received the B.Sc. and M.Sc. degrees in electrical engineering from the Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany, in 2017 and 2019, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering with the Institute of Power Electronics.

Since 2019, he has been with the Institute of Power Electronics, FAU. His research interests include the design, magnetic integration, and control of radio frequency power converters.

Martin März received the Diploma and Ph.D. degrees in electrical engineering from the Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany, in 1988 and 1995, respectively.

During his Ph.D. degree at the Institute of Microwaves and Photonics, FAU, his research focus was on microwave excitation of CO_2 lasers. Beginning in 1995, he was with the Semiconductor Division, Siemens (later Infineon), Munich, Germany. Since 2000, he has been the Head of the Power Electronics System Department and the Deputy Director of the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany. Since 2016, he has been the Head of the Institute of Power Electronics, FAU. His research interests include innovative technologies for power electronics with a focus on very high power density and efficiency, thermal management, system integration, and cognitive power electronics.