TCAD Investigation of Differently Doped DLC Passivation for Large-Area High-Power Diodes

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***Abstract*— An electroactive passivation for high-voltage diodes with bevel termination has been investigated based on diamond-like carbon (DLC) films. Variations of the DLC properties, i.e., conductivity and geometry, have been investigated by experiments and numerical simulations to the purpose of gaining an insight on their influence on the diode leakage current and breakdown voltage. The role played by the DLC/Si interface has been investigated by characterizing metal–DLC–Si devices. Both boron and nitrogen doping have been investigated, and a TCAD setup has been provided accounting for the main transport features of the DLC material with different doping configurations. A significant polarization effect has been observed in the DLC material, which improves the DLC performance as a passivation material. High-voltage diodes have been characterized and simulated with different DLC layers on top of the bevel termination in order to identify the role played by conductivity and polarization on the blocking state. The correlation of leakage current and voltage breakdown with the DLC doping and thickness is provided and explained by the TCAD simulation results.**

***Index Terms*— Bevel termination, diamond-like carbon (DLC) simulation, large-area diode, TCAD modeling.**

I. Introduction

In THE field of power devices with the highest current handling capability, large-area silicon diodes and thyristors with very low leakage current and high blocking voltage have been recently proposed as key elements for the ultrahigh-power applications [1], [2]. The required breakdown voltage is typically between 3 and 10 kV. The maximal rating currents range from 0.5 to 6.25 kA, and surge currents as high as 100 kA are reached depending on the pulse length. In order to reach such current levels, diodes use a full wafer with a diameter ranging from 40 to 150 mm. The wafers are treated to reduce defects while well-optimized junction-termination techniques are used to reach a stable blocking with minimal consumption of wafer periphery area at the same time. Usually, the state-of-the-art beveling of the wafer periphery is applied to control the curvature of the junction at the surface and consequently reduce the local electric field [3], [4].

In order to preserve the ideal termination effect and provide a stable breakdown capability, high-quality surface passivation is needed to control or compensate the charging effects at the silicon interface. Both insulating and semi-insulating materials have been used in the past as passivation layers, e.g., polyimide and polycrystalline silicon [5], [6]. More recently, amorphous carbon (a-C:H), also called diamond-like carbon (DLC), has been used as a robust surface passivation material [7], [8], [22]. This material is very attractive as it shows outstanding mechanical, chemical, thermal, and optical properties [9]. From an electric point of view, it comes out from the mixture of diamond and graphite bonds, leading to very interesting features as, e.g., a significant polarization effect which was recently characterized and simulated in a commercial TCAD framework as a corresponding dielectric loss via the Debye equation [10].

The attractiveness of the DLC compared to other known passivation processes is given by the fact that the whole passivation layer can be processed by the plasma-enhanced chemical vapor deposition (PECVD) sequence under the same vacuum including the doping and masking. Moreover, the process allows one to adjust the composition of the DLC layer in a sufficiently wide processing window giving the breakdown voltage close to the theoretical limit with a high reproducibility. Also, the mechanical strength and a good adhesion of the diamond-based layer are important for a high production yield of the discrete devices with diameters up to 150 mm. Last but not least, in the long-term electrical stability, the DLC layer easily outperforms the other available passivation concepts. All these benefits can be achieved provided that the doping profiles, bevel geometry, as well as the whole process of mechanical grinding and subsequent surface treatment are optimized. In this article, the best design to the knowledge of authors has been used for experimental demonstration.

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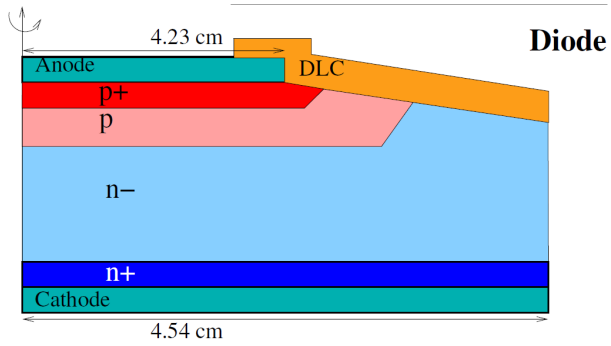

Fig. 1. Schematic of the cross section of the investigated large-area diode with cylindrical symmetry. Top and bottom radii are reported. The termination region is realized with a bevel passivated by a DLC layer. An additional encapsulation is assumed on the diode periphery to set required creepage distance between anode and cathode (not drawn). The structure is not in scale.

The conductivity of the DLC layer can be efficiently controlled using boron or nitrogen doping. Experimental results clearly showed that doping is substitutional but strongly compensated and accompanied by an increased defect density in the bandgap [11]–[13]. Recently, the TCAD modeling of the charge transport in doped DLC materials was addressed to investigate their application as an electroactive passivation for bevel terminations [14]. Charge transport in nitrogen-doped DLC layers was simulated by assuming the presence of doping shallow states as well as bandgap traps, polarization effects were fit against C–V curves, and TCAD predictions of the breakdown voltage were compared with experiments for diodes with differently N-doped DLC passivation in order to validate the simulation approach. As the TCAD setup accounts for the 3-D structure of the diodes along with the correct model of the Si/DLC heterostructure, it can be used to further study and compare the effects of the DLC conductivity on the diode leakage current as well.

Starting from [14], the modeling approach has been extended to boron-doped DLC layers in this article and the important issue of correlating the leakage current and blocking voltage of the diode with the doping and thickness of the DLC passivation layers is addressed for the first time. Both experiments and numerical simulations have been carried out allowing a detailed understanding of the device operation including charge transport through the passivation layer up to avalanche conditions. This knowledge is important for further reduction of silicon area consumed by the junction termination in future devices.

II. Test Structures and Characterization

Our reference device is a circular diode as schematically represented in Fig. 1. The diode is processed using classical implantation and drive-in techniques at a silicon wafer. Afterward, it is cut-out to the final diameter and the negative bevel is mechanically grinded to provide the required blocking voltage. The bevel is then chemically treated to minimize the surface roughness and provide a clean surface for the subsequent passivation process. The DLC is used as passivation layer directly in contact with the silicon bevel edge. The same device geometry was used with different DLC depositions

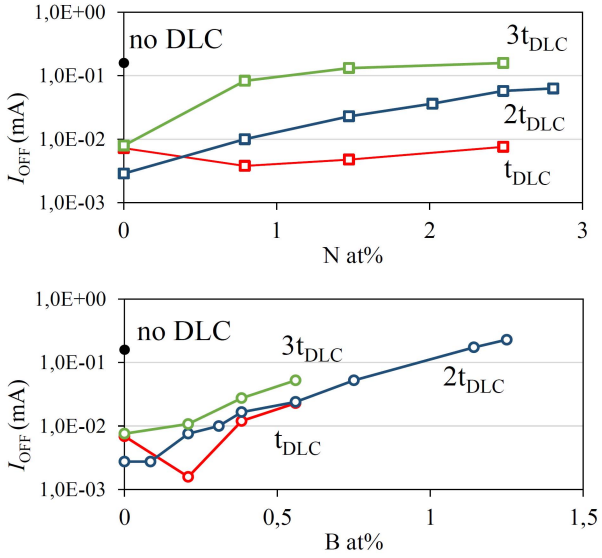

Fig. 2. Leakage current of the diodes versus doping atomic percentage of the DLC passivation for three different DLC thicknesses. Nitrogen doping (top). Boron doping (bottom). Black dot: diodes without DLC passivation.

for investigating the performance of the DLC materials under real application conditions. Both undoped and doped DLC films were grown with the same process steps apart from adding the doping species, and n-type and p-type doped DLCs were prepared by introducing nitrogen and boron, respectively. Different atomic concentrations have been used to study the role of doping on the DLC conductivity. As the DLC thickness is a key design parameter along with the doping for a resistive termination, three different deposition times have been used to grow thicknesses equal to t_{DLC}, $2t_{DLC}$, $3t_{DLC}$, with t_{DLC} the reference thickness of the layer, ranging from about 190 to 300 nm. The latter values depend on the doping concentration as different chemical reactions are activated by the flow of dopants during the deposition leading to a lower growth rate for doped DLCs.

The performance of the diodes with different passivation layers has been measured by collecting the leakage current (I_{OFF}) at a reverse bias of 4000 V and the breakdown voltage (V_{BD}) at a fixed current of 15 mA. The measurements were carried out at room temperature in order to limit the current flowing in the bulk silicon to its minimum, leading to a leakage current mostly flowing at the surface along the termination region. Experiments carried out on diodes without the DLC passivation are reported for comparison, showing significantly high leakage current and the lowest breakdown voltage: the presence of mobile charges close to the semiconductor surface can be the main cause for such a compromised performance.

The measured I_{OFF} is reported in Fig. 2 as a function of different atomic concentrations of nitrogen and boron for the three different DLC thicknesses. In the case of nitrogen doping, the increase of I_{OFF} with increasing passivation conductivity is observed only for the thicker layers. Differently, the increase of I_{OFF} in the case of boron doping is observed also for the thinner layer. A possible explanation of the latter feature could be the presence of an interface layer close to silicon with transport properties different from the

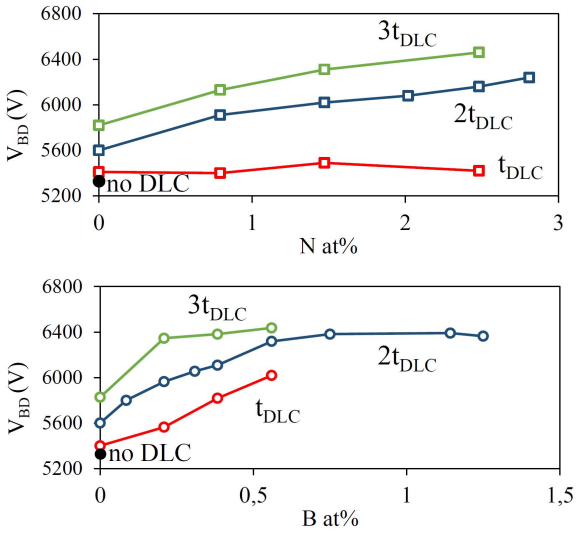

Fig. 3. Breakdown voltage of the diodes versus doping atomic percentage of the DLC passivation for three different DLC thicknesses. Nitrogen doping (top). Boron doping (bottom). Diode nominal rating is 4.5 kV. Black dot: diodes without DLC passivation.

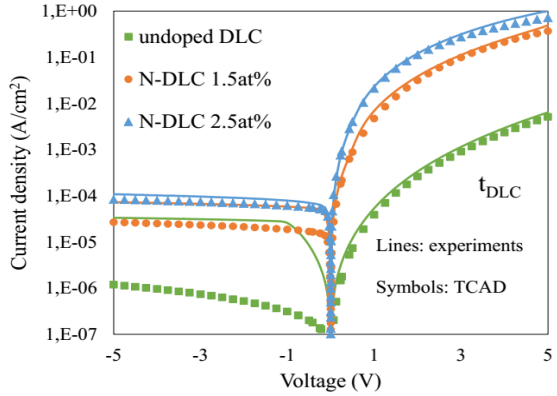

Fig. 4. Current density characteristics of the metal–DLC–Si test structures with an n-type silicon substrate and N-DLC with different doping concentrations. Symbols: TCAD results. Lines: experiments.

DLC film on top. This was experimentally confirmed by the conductivity measurements carried out on lateral and vertical metal–DLC–Si test structures: a difference of about a factor 100 was found between the conductivity extracted from J–V measurements on the vertical stack and on a lateral structure with both contacts on top of the grown DLC. In addition to this, variations of the DLC properties of the interface layer are expected on the bevel structure due to the surface roughness [15] and to the effect of the angle in the reaction chamber [16].

Thus, in order to consistently model it, an interface film of DLC has been realized in the TCAD structure assuming a limited conductivity independent of the doping [14]. A similar model was proposed in [17] for the interpretation of the optical properties of boron-doped DLCs, which led to the extraction of different interlayer and doped DLC thicknesses. The interface layer thickness should thus be assumed depend on different doping types and concentrations due to the effect of the chemical reactions taking place in the deposition process. To this purpose, the interlayer thickness in the TCAD setup was fixed by directly comparing the simulation results with experiments on the diode: a thickness of about 130 nm was used for the undoped interlayer in the nitrogen case compared to about 70 nm for the boron one, which nicely explain why a limited doping dependence is observed in the N-DLC with respect to the B-DLC.

The measured V_{BD} is reported in Fig. 3 as a function of different atomic concentrations of nitrogen and boron for the three different DLC thicknesses. A significant increase of the blocking voltage is found for both doping types when thicker layers and larger doping doses are used. It confirms the expected role played by the conductivity of the passivation layer in releasing the surface electric field: as in this kind of diodes the onset of avalanche in silicon takes place below the surface along the bevel, the DLC provides an effect similar to the SIPOS field-plate structures [5], [18], [19]. A saturation effect in the V_{BD} is found for layer conductivities larger than those which give the optimum surface-field release. Differences between nitrogen and boron cases also arise from the role of different types of free charges moving in the passivation layer, as explained with TCAD results in Sections III and IV.

III. TCAD Modeling of DLC Passivation Layers

Following [10] and [14], a simulation setup for the reference diode has been prepared in the framework of the commercial TCAD tool by Synopsys [20]. As shown in Fig. 1, the structure of the reference diode is cylindrical; thus, a 2-D radial description of the device has been used and transport equations are solved under cylindrical coordinates to obtain full 3-D results. Special care has been devoted to the definition of the doping profiles received from the spreading resistance profiling. The Shockley–Read–Hall model for the thermal generation–recombination has been used with a high carrier lifetime fit against the reverse leakage current curves at different temperatures. The fabricated diodes did not experience the usual shaping of the lifetime through irradiation, which would require electrothermal simulations to calibrate the deep defect levels introduced by this process [21]. The Van Overstraeten model for the impact-ionization generation has been used with default parameters.

The DLC layer is simulated as a two-layer system. A first interface layer of DLC close to the silicon substrate has been realized in the TCAD structure assuming conductivity and distribution of midgap traps different with respect to the second layer on top [22]. The first film has been modeled with a thickness of about 130 nm for N-DLC and 70 nm for B-DLC as explained in Section II. The DLC layer has been modeled using the TCAD setup adopted for the MIS structures in [14] for the undoped and N-doped DLC. More specifically, the drift-diffusion (DD) transport model has been used with suitable physical parameters [23]. A hopping mobility has been used as J–V measurements on the vertical metal–DLC–Si devices clearly show a Poole–Frenkel-like behavior independently of the adopted doping type and concentrations [12], [24], [25] (Figs. 4 and 5).

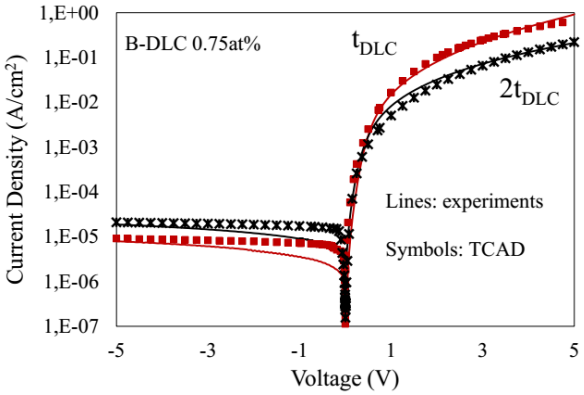

Fig. 5. Current density characteristics of the metal–DLC–Si test structures with an n-type silicon substrate and B-DLC with different DLC thicknesses. Symbols: TCAD results. Lines: experiments.

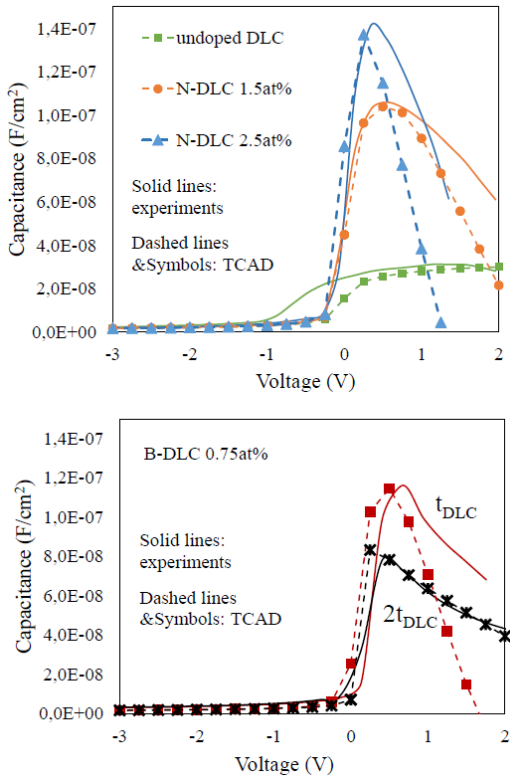

Fig. 6. Simulated *C–V* curves of the metal–DLC–Si test structures compared with experiments at 10 kHz. The TCAD data well reproduce the experimental data by introducing the polarization effect through the Debye model. N-DLC (top). B-DLC (bottom).

By studying the current–voltage characteristics with N and B-DLC, an n-type behavior was observed for the N-DLC case while no clear evidence of a p-type behavior is observed in the B-DLC curves. In agreement with [12], no threshold-voltage shift is experimentally observed in the current characteristics (Figs. 4 and 5), even if a significant increase of conductivity is found. As far as the doping concentration is concerned, the boron doping is more active than the nitrogen one, as a very large conductivity is obtained with lower at%.

In order to correctly model the doping effects, a first set of characterizations were carried out. All DLC layers showed a

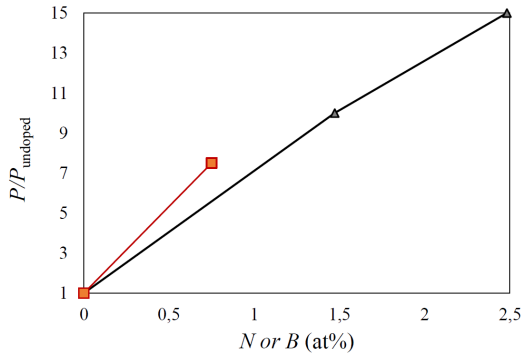

Fig. 7. Normalized polarization values used in the TCAD simulations of the metal–DLC–Si devices reported in Figs. 4 and 5. Triangles: N-DLC. Squares: B-DLC.

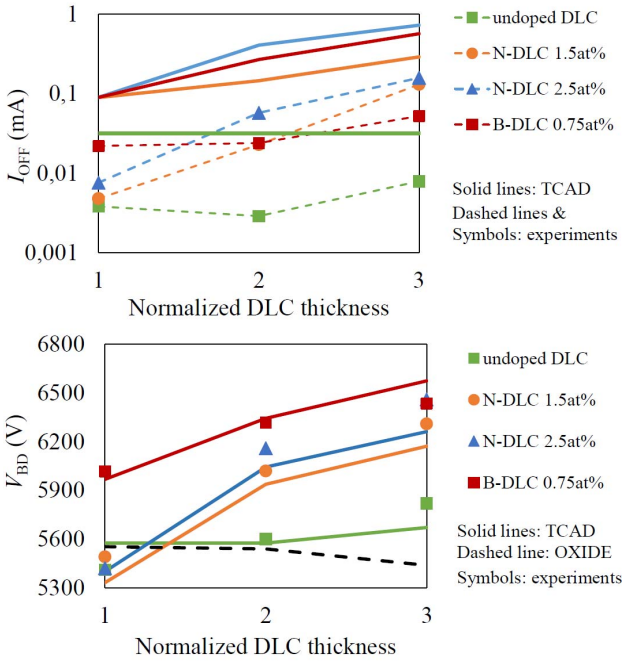

Fig. 8. Simulated leakage currents (top) and breakdown voltages (bottom) compared with experiments for different DLC passivation thicknesses and doping configurations.

quite constant optical bandgap of about 1 eV, independent of the doping. The optical answer in DLC is dependent on the presence of sp^2 bonds (graphite-like carbon) with π orbitals in the bandgap of the diamond-like structure given by sp^3 molecules with σ orbitals [26]. The constant optical bandgap indicates that the sp^2 bands are formed with similar features in all the DLC layers.

The effect of nitrogen doping is modeled in the TCAD by assuming a donor doping concentration, which corresponds to the usual effect of shallow traps close to the conduction band, and an additional Gaussian distribution of partially occupied deep level defects in the midgap as explained by theoretical studies [6], [27]. The detailed description of the adopted parameters is reported in [14], where TCAD data are validated against *J–V* experiments of MIS devices for different *N* concentrations. Here, the current density characteristics are reported for completeness showing also the reverse bias regime

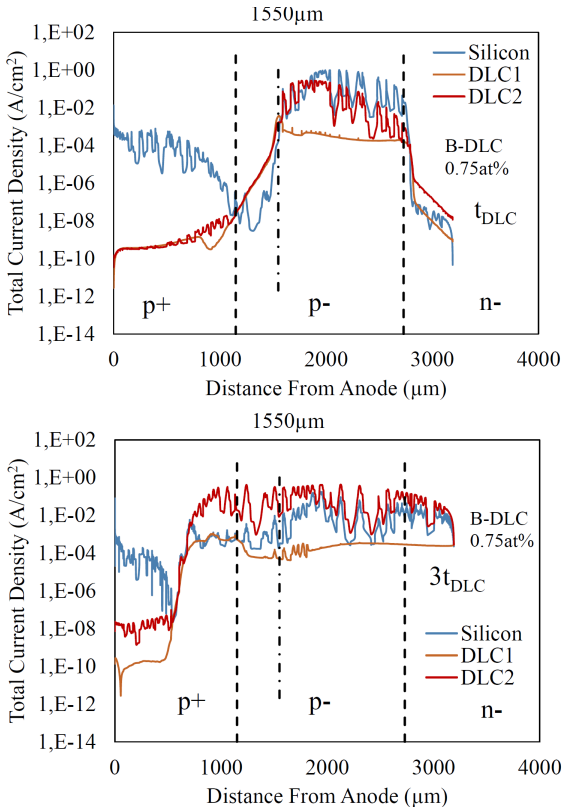

Fig. 9. Simulated current densities along the bevel in silicon, DLC1, and DLC2. The DLC is B-doped with a thickness of t_{DLC} (top) and $3t_{DLC}$ (bottom). Dashed lines: positions of the p+/p− and p−/n− junctions along the bevel. Central dot-dashed line: position where the silicon surface current density significantly changes at the anode region.

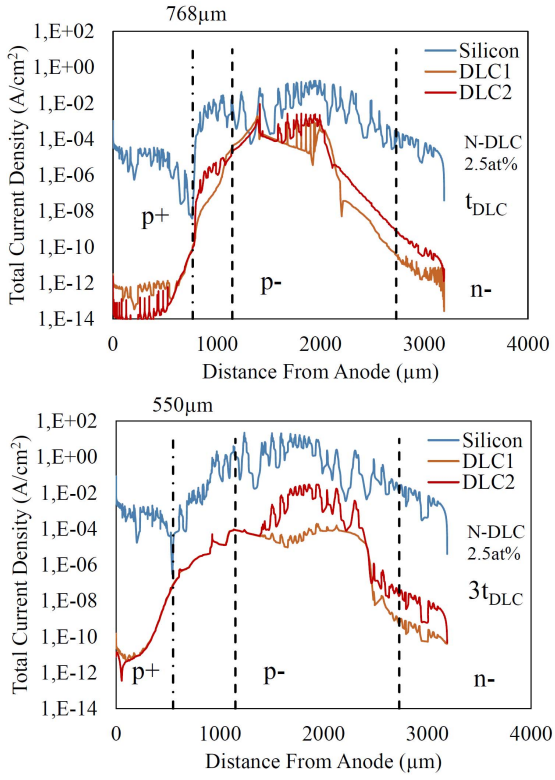

Fig. 10. Simulated current densities along the bevel in silicon, DLC1, and DLC2. The DLC is N-doped with a thickness of t_{DLC} (top) and $3t_{DLC}$ (bottom). Dashed lines: positions of the p+/p− and p−/n− junctions along the bevel. Left-side dot-dashed line: position where the silicon surface current density significantly changes at the anode region.

(Fig. 4). The main role played by the bandgap traps is that of introducing trapped charges at the Si/DLC interface along the diode termination, which eventually improves the breakdown voltage as shown in Section IV.

For the boron-doped case, the same bandgap of about 1 eV has been adopted, but no shallow or Gaussian traps should be included in the material setup as no evidence of their electrostatic effect is visible in the *J*–*V* curves, i.e., no threshold-voltage shift is observed in Fig. 5 with respect to Fig. 4. In agreement with the theoretical explanations in [6], [12], and [27], the acceptor level lies within the occupied π shoulder forming the valence band edge and gives rise to defects at the conduction band edge, increasing dramatically the density of states (DOS) leading to a modification of the band itself. Differently from the electrostatic effect of localized defects, the increased DOS leads to an increase of free charges without pinning the Fermi level. In order to correctly model boron doping, the Gaussian DOS (G-DOS) model for disordered organic semiconductors available in the TCAD tool has been adopted [20]. The DOS peaks have been calibrated by fitting the *J*–*V* curves reported in Fig. 5. As with nitrogen, the high increase of current in forward regime is ascribed to the Poole–Frenkel-like hopping model which has been tuned as discussed in [10]. The standard deviation of the G-DOS has been kept at the default value as no correlated effect is observed in the reference experiments.

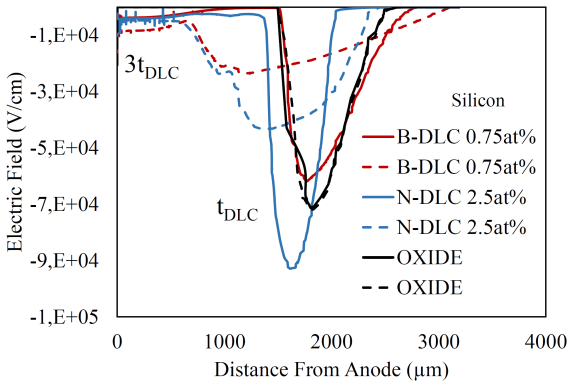

Fig. 11. Simulated electric field along the bevel versus distance from anode edge. TCAD cutlines within silicon on diodes with ideal SiO_2 oxide, N-DLC, and B-DLC. Two different thicknesses are reported. Solid lines: t_{DLC}. Dashed lines: $3t_{DLC}$.

The dielectric polarization P induced by the DLC disorder has been accounted for in the TCAD setup by the solution of the first-order Debye equation in the ferroelectric model [20]. A similar disorder has been measured in DLC layers with different doping types from the visible Raman spectra. Thus, a congruent increase of P is expected for B and N. The polarization vector has been calibrated against *C*–*V* experiments following the approach reported in [10]. To this purpose, data at relatively low frequency (10 kHz) have been used to determine P, which gives the capacitance peak at the threshold

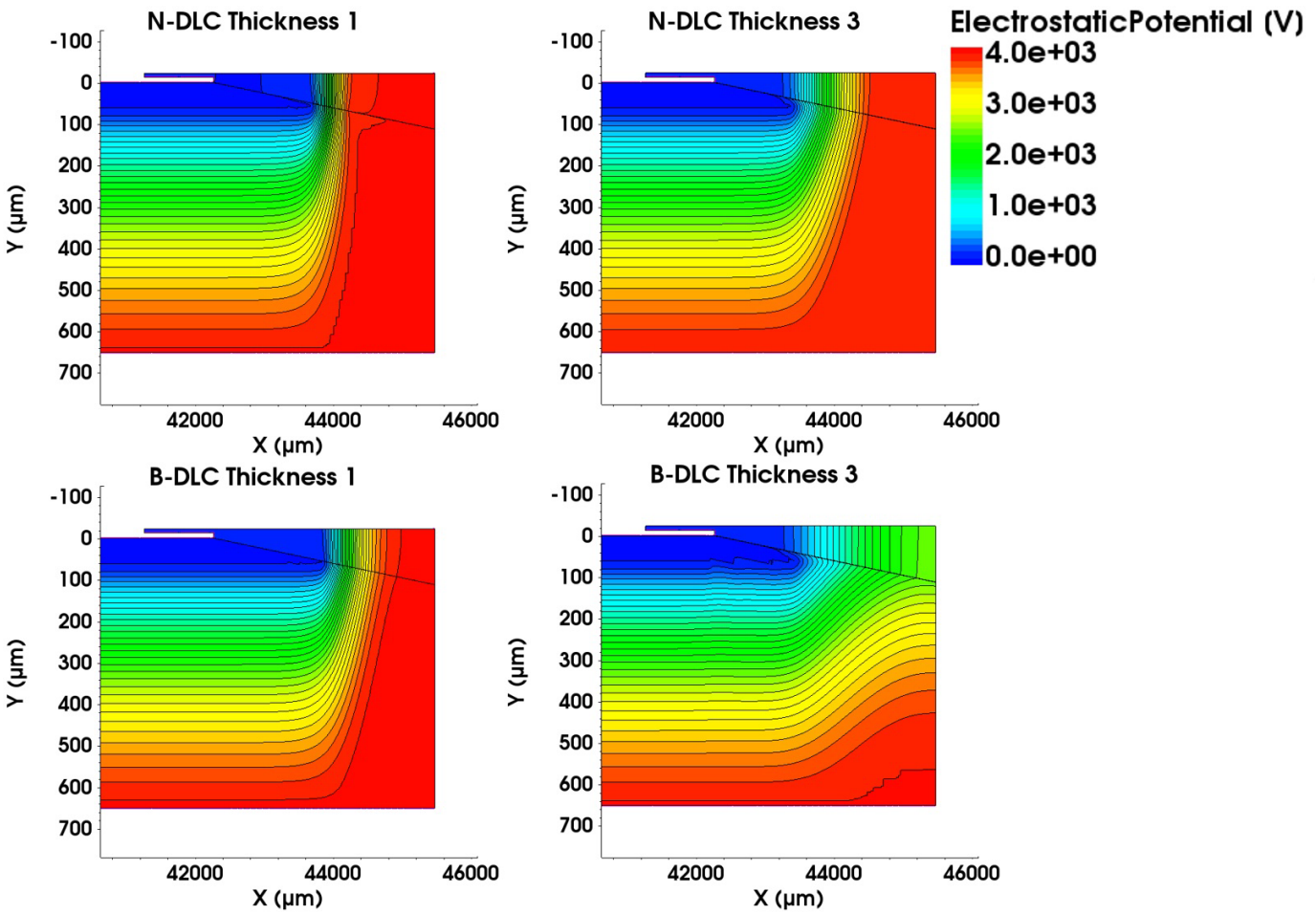

Fig. 12. 2-D potential contour plots of the diode termination region for different cases reported in Fig. 11.

voltage. In Fig. 6, the model previously calibrated on N-DLC devices in [14] is compared with new data on B-DLC for two different DLC thicknesses. The increase in the fit P is reported as a function of doping in Fig. 7 for both B and N cases: the curves show similar increasing rate in agreement with the expected similar DLC disorder.

IV. Simulation Results of I_{OFF} and V_{BD}

TCAD simulations of the diode structure have been carried out by using the simulation setup reported in Section III. The DLC interlayer (DLC1) and the top side passivation (DLC2) have been realized along the bevel region. The DLC1 thickness is fixed to 130 nm for N-DLC and 70 nm for B-DLC, while the DLC2 thickness is changed in order to emulate different deposition times. The transport and polarization models for the nitrogen and boron cases calibrated for the vertical metal–DLC–Si devices are applied to the DLC on the diode in order to emulate different doping configurations by keeping the same parameters values. In this way, the effect of the DLC/silicon heterostructure is correctly accounted for.

Fig. 8 shows the simulation results, showing I_{OFF} at 4 kV and V_{BD} at 15 mA as functions of the DLC thickness for different doping configurations. The predicted I_{OFF} overestimates the measured current with almost the same factor for any configuration. This might be ascribed to a lack in the modeling of the silicon interface related to the bevel structure, such as mobility degradation due to nonuniformities (surface roughness). The V_{BD} results are in good quantitative agreement with experiments. The main difference has been observed for the undoped case. In this specific case, we compared the DLC results with numerical simulations using an ideal insulator (OXIDE): in both cases, no significant increase of V_{BD} with t_{DLC} was found, leading to the conclusion that an increase of conductivity is experienced by the DLC material when longer deposition times are used, maybe due to some kind of annealing effect.

The trends ascribed to the transport effects of the DLCs are nicely reproduced by the TCAD results, allowing for a detailed understanding of the charge transport through the passivation layer up to avalanche conditions. The main conclusions reached by this analysis are that, at high voltage, the reverse current flowing into the passivation layer increases with increasing conductivity of the DLC2 region. The N-DLC results are more effectively influenced by the thickness of the passivation in accordance with the thicker interlayer region with limited conductivity. At larger thicknesses, the B-DLC case shows a lower I_{OFF} and a larger V_{BD} compared to the N-DLC ones. In order to gain an insight on the latter feature, the current densities and electric fields at the diode surface

have been analyzed. In Figs. 9 and 10, the total current densities along the bevel are reported at three cutlines in silicon, DLC1 and DLC2, respectively. Both boron and nitrogen cases are reported for the thicknesses t_{DLC} and $3t_{DLC}$, respectively. A limited current density is experienced in the silicon at the quasi-neutral region on the anode side, which corresponds to a significant current drop in the DLC1 and DLC2 regions, while large current densities are shown along the depleted region by all layers. Due to the effect of the positive charge in the B-doped DLC, a smaller extension of the depleted region is experienced at the anode side, leading to a lower leakage flux in the inner area of the diode [Fig. 9 (top)]. At larger thicknesses, the current density in the B-DLC is larger than at the surface silicon and spread on an extended region of the bevel [Fig. 9 (bottom)]: in this case, a linearization of the potential is expected, due to the large conductivity of the passivation, while a relatively limited I_{OFF} is spread on the periphery of the diode.

Vice versa, an opposite effect is shown by the N-DLC case, where the depleted region is shifted toward the center of the diode [Fig. 10 (top)]. When a thicker layer is used, a further shift of the depleted region is observed, and an increase of the I_{OFF} is experienced, mostly given by a vertical current path localized in the central part of the bevel [Fig. 10 (bottom)]. As the current density in the doped DLC2 is high and spread on the bevel, a reduction of the peak electric field is anyway expected.

As far as the V_{BD} is concerned, the larger V_{BD} of the B-DLC cases can be again ascribed to the role of the positive free charge in the DLC2 and to the consequent shift of the depletion region toward the periphery of the diode. In Fig. 11, the electric field profile within silicon along the bevel is reported at the fixed bias of 4000 V, showing the role of the DLC transport properties on the critical surface electric field. The effect of the free charges flowing on top of the depleted region is significant in changing the shape and peak of the electric field: similar surface electric field distributions are observed for the thinner DLC layers with respect to the case with an insulator (OXIDE), while quite spread fields are visible when thick DLC layers are adopted. The potential contours in the device radial cross section of the bevel region are reported in Fig. 12, showing the significantly reduced surface field experienced by the thicker DLC layers.

Finally, the effect of polarization on the electrostatics of the diode was checked by simulations: the presence of P in the DLC layers induces an increase of the breakdown voltage ranging from 180 to 250 V in the analyzed cases (not shown), which is in agreement with the significant reduction of the peak electric field shown in [14].

V. Conclusion

To our knowledge, this is the first model implemented in commercial semiconductor simulators for the DLC material, calibrated and verified against a wide set of experiments. To understand the electrical behavior of DLC layers, the microscopic nature of this material has been accounted for, by defining the bandgap, the DOS, traps, and defects consistently with theoretical studies. As the DLC is a disordered material, the capacitance curves have been used to model the polarization effects, and the dependence on doping configuration was extracted for the experimental results. The model was finally demonstrated to nicely reproduce the performance of large-area diodes including the passivation layer. An increase of breakdown voltage and leakage current with increasing doping and thickness of the DLC layer observed experimentally hereby received a theoretical support. Our implementation can be a useful starting point for designing high-voltage devices with terminations in which DLC can play even more relevant role in the improvement of ratings than up to this time.

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