Predictive Current Controller for Single-Phase Grid-Connected VSIs With Compensation for Time-Delay Effect and System Uncertainty

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***Abstract*— In the last decade, predictive current control (PCC) has been widely implemented for grid-connected voltage source inverters (VSIs) due to the advantages of low-current harmonic injection, fast dynamic response, and easy implementation for digital control systems. However, with the increasing switching frequency of VSIs applied to pursue a better output quality, inevitable time delays and uncertain system disturbances are aggravating system performance and stability, which presents a serious challenge for the PCC design. Thus, a new PCC algorithm has been proposed in this paper for a single-phase VSI to improve the quality of the current fed to the grid, as well as enhance the system stability and robustness. The proposed control scheme is developed from the traditional predictive current controller along with a simple weighted filter predictor and a robust adaptive voltage compensator. The results of simulation and experiment investigation have demonstrated the improvements of the proposed control scheme in inverter output quality and robustness to parameter variations.**

***Index Terms*— Inverters, predictive control, total harmonic distortion (THD).**

I. Introduction

DRIVEN by government incentives as well as environmental requirements, grid-connected voltage source inverters (VSIs) for wind and photovoltaic (PV) generation systems have been significantly developed in recent years [1], [2]. To meet the requirement of grid interconnection standards, current control pulsewidth modulation (PWM) techniques are usually employed to produce the high quality output with fast and accurate current response. And thus, predictive current control (PCC) as one of the most effective current control algorithms attracts the support from both academic research and industrial applications taking advantages of a fast transient response, zero steady-state errors, robust time-delay compensation, and full compatibility with the digital signal processor (DSP)-based digital system implementation.

There are several current control techniques presented under the name of "predictive control" in grid-connected VSI applications, such as the well-known deadbeat controller [3], [4] with advantages of fast dynamic response and simple implementation, the Smith predictor [5], [6] featured in deadtime compensation, the model predictive control (MPC) methods [7], [8] which can benefit control robustness by giving system uncertainty consideration in the design stage, and the algorithms of finite control set model predictive control [9], [10] which can further reduce the system computation loss by removing the modulator. However, when the inverter operates at a higher switching frequency, the amplified time-delay effect caused by sampling distribution, computation in DSP, and inherent PWM generator update is inevitable which severely degrades the performance and stability of PCC. The model PCC stated in [11] and [12] improved time-delay compensation and reference tracking by selecting the switch state to minimize the cost function; however, it asked for a high-level requirement for load current prediction as well as strict guidelines for parameter tuning. Some attempts can be found in the recent literature: modified Smith predictors [13], [14] and MPCs [15] offer the potential of a complete time-delay compensation for PCC, but a precise system model is indispensable; a linear extrapolation method is widely used for PCC [16]–[19] without system information required; however, the accuracy of the current approximation is highly dependent on distributions of actual measurements as well as the effective duty cycle for each switching period; an approach presented in [20] is used to improve the performance of PCC with a dual-timer sampling strategy, but it is only valid when the sampling frequency is an integer multiple of the switching frequency of the PWM control. In addition, the poor stability margin for parameter variations of the system model such as the practical filter inductance will also have a large influence on the performance of PCC.

In order to alleviate the aforementioned limitations, a robust current control scheme featuring high adaptability to time delays and system uncertainties and high robustness to parameter mismatch has been designed in this paper. The proposed scheme is built on a structure of PCC and developed with an improved time-delay compensation technique, which greatly reduces the current tracking errors through a simple weighted filter predictor (WFP) and completely eliminates static voltage errors introduced by system disturbances and uncertainties through a robust adaptive voltage compensator (AVC).

The remainder of this paper is organized as follows. A description of the PCC system of VSIs is introduced

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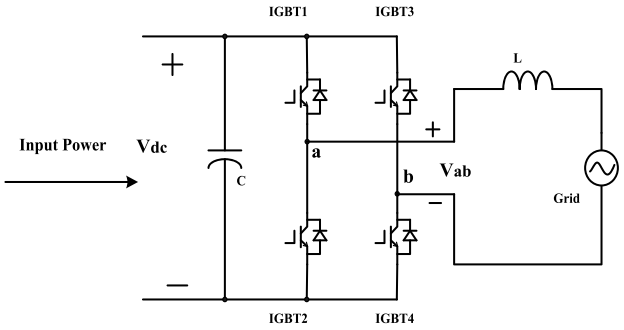

Fig. 1. Typical topology of single-phase grid-connected VSIs.

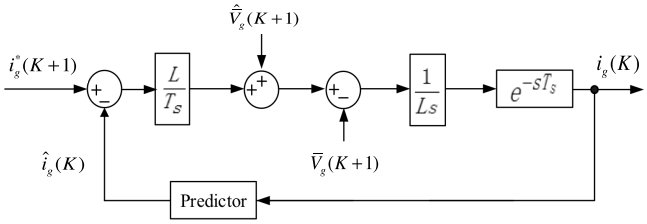

Fig. 2. PCC scheme of grid-connected VSIs.

in Section II. Modeling of VSI digital current control is detailed in Section III. A novel robust PCC scheme for single-phase grid-connected VSIs is proposed in Section IV. Stability analysis is presented in Section V. Experimental results are discussed in Section VI, and the conclusion is provided in Section VII.

II. PCC System of VSIs

Fig. 1 shows a typical topology of single-phase VSIs used for grid-connected wind and PV generation systems, which is composed of a dc-link capacitor bank used as an energy buffer and a single-phase full-bridge insulated gate bipolar transistor inverter with L-type filter. The VSI investigated in this paper is developed on a TMS320LF2407A DSP platform.

A. Control System Configuration

When the switching frequency of VSIs is much higher than the grid frequency, the averaged output voltage of the inverter (v_{ab}) can be written in discrete form based on the averaged switch model of VSIs as

$$v_{ab}(K+1) = L\frac{i_g(K+1) - i_g(K)}{T_s} + \overline{v_g}(K+1) \qquad (1)$$

where T_s is the switching period, $i_g(K)$ and $i_g(K+1)$ are the grid currents measured at the end points of Kth and $(K+1)$th switching periods, and $\overline{v_g}(K+1)$ is the averaged value of the grid voltage during the $(K+1)$th switching period.

As the VSI is connected to the grid, the quality of current output becomes the main concern for grid interconnection standards. Thus, a basic PCC scheme can be developed from a typical deadbeat controller to achieve a lower current total harmonic distortion (THD), which is shown in Fig. 2. When a precise model of the system is given and no extra delay time is introduced, the PCC scheme is an ideal deadbeat

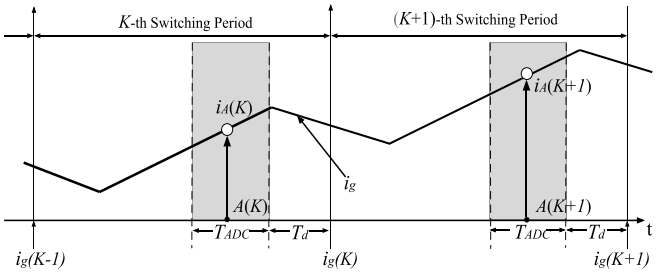

Fig. 3. Sampling strategy for robust current controller.

current controller which has fast response and good tracking performance by enforcing the grid current $i_g(K+1)$ to the value of the reference current $i_g^*(K+1)$. However, in practical implementation, the delay due to sampling and calculation time is inevitable, which makes it impossible to acquire the instantaneous value of the grid current at the endpoint of the Kth switching period, $i_g(K)$. Thus, a predictor is necessary to compensate the delay time by forecasting the forthcoming values of system variables. In Fig. 2, the actual values of the grid current $i_g(K)$ and the averaged grid voltage $\overline{v_g}(K+1)$ are estimated by predictions of the past measurements with a real-time sampling strategy, which are denoted by $\hat{i}_g(K)$ and $\hat{\overline{v}}_g(K+1)$, respectively. And thus, the acquired (reference) output voltage of the inverter can be described by

$$v_0^*(K+1) = L\frac{i_g^*(K+1) - \hat{i}_g(K)}{T_s} + \hat{\overline{v}}_g(K+1). \qquad (2)$$

It is clear that the performance of this presented PCC system is depended heavily on the prediction methods and corresponding sampling schemes applied to the estimation of forthcoming values of the grid current and voltage.

B. Sampling Strategy for PCC

Several sampling strategies in [17]–[19] can be employed for the PCC based on linear prediction technique. However, time-delay compensation by a linear predictor is only valid when the system dynamic characteristic is significantly slower than the delay time [23]. When the switching frequency is comparable to the sampling frequency ($T_s/T_{\mathrm{ADC}} \leq 5$, where T_{ADC} represents the sampling period), a glaring error in current estimation will be realized. In addition, when a variable switching frequency is applied to the system [24] or the sampling frequency cannot be a multiple of the switching frequency, the distribution of sampling points varies in different switching periods which severely reduces the accuracy of the predictive grid current and thus leads to undesirable and uncontrollable fluctuation in the output performance of current harmonic distortion.

To overcome these limitations of the linear prediction method, a new sampling strategy is designed in this section which will work together with the proposed robust PCC scheme to attenuate the time-delay effect. Fig. 3 shows the new sampling scheme, where T_d denotes the inevitable part of time delays including the program calculation and the PWM update. In this paper, $T_d = 20\mu$s which is limited for the

DSP TMS320LF2407A. Consequently, the measurement of the actual current $i'_g(K)$ is selected at the sampling point $A(K)$ which is located in the period $[KT_s - T_d - T_{\rm ADC}, KT_s - T_d]$ in order to minimize the delay time as well as to keep the enough margins for operation, which is expressed by

$$i'_g(K) = i_A(K) \tag{3}$$

where $i_A(K)$ is the measured value of the actual current at the sampling point $A(K)$.

In addition, when the switching frequency of VSIs is much higher than the grid frequency, the average grid voltage $\overline{v_g}(K)$ can also be estimated by the measurement at sampling point A. Meanwhile, working on an assumption of a linear change of the grid voltage in two consecutive switching periods, the average grid voltage in the $(K+1)$th switching period can be predicted by

$$\hat{\overline{v}}_g(K+1) = 2\overline{v_g}(K) - \overline{v_g}(K-1). \tag{4}$$

According to the forgoing analysis, the new sampling scheme is effective to limit the sampling delay T_m in a small range of T_d to $(T_d + T_{\rm ADC})$, where $T_{\rm ADC}$ is set to 25μs in this paper. Moreover, the impact of time delays can be directly reflected in the control system diagram to evaluate the performance and stability of the current controller.

III. Modeling of Digital Control System of VSIs

For a DSP-based VSI control system, modeling in z-plane is an easy and effective method to describe the system characteristics and analyze the system stability. Thus, a discrete model of VSIs needs to be built first for the PCC design accounting for the nature of the inverter and sampling approximation. According to the averaged switch model of VSIs described by (1), the output voltage of the inverter is assumed to remain constant during each switching cycle; thus, the inverter can be modeled as a sample-and-hold element, which can be represented by a zero-order hold circuit with a transfer function $G_0(s)$

$$G_0(s) = \frac{1 - e^{-sT_s}}{s}. \tag{5}$$

And thus, the discrete model of the VSI can be obtained as

$$G_{\rm inv}(z) = Z\left\{G_0(s)\cdot\frac{1}{Ls}\right\} = \frac{T_s}{L}\frac{1}{z-1}. \tag{6}$$

In addition, as the delay influence lasts until the next switching cycle, the time delays introduced by the proposed sampling strategy can be regarded as a sample and linearly varying element, which can be represented by a first-order hold circuit with a transfer function $G_1(s)$

$$G_1(s) = \frac{1}{1+sT_s}. \tag{7}$$

Then, the z transform of the transfer function of the sampling delay e^{-sT_m} can be given by

$$G_d(z) = Z\{G_1(s)\cdot e^{-sT_m}\} = \frac{(1-K_d)z + K_d}{z} \tag{8}$$

where $K_d = (T_m/T_s)$.

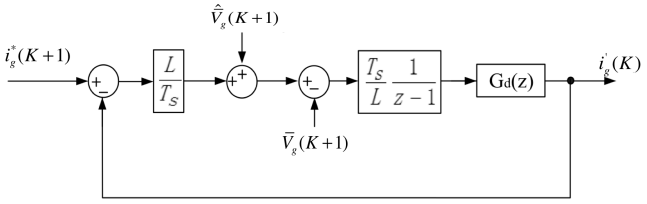

Fig. 4. Discrete model of ideal predictive current controller.

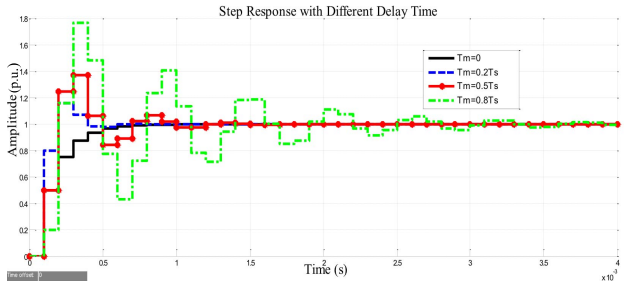

Fig. 5. Step responses of predictive current controller with different time delays.

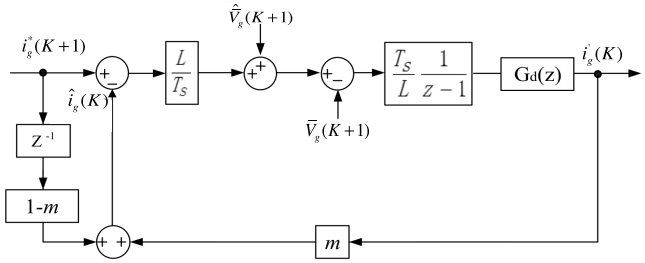

Fig. 6. PCC scheme with WFP.

Therefore, the proposed PCC scheme of VSIs with time-delay consideration in z-domain is presented in Fig. 4, and its closed-loop unit step response is illustrated in Fig. 5 when a 10-kHz switching frequency is applied. It can be observed that the system dynamic performance is rapidly deteriorated in terms of both the percent overshoot and the settling time, as the delay time increases.

IV. Robust PCC Scheme

A. Weighted Filter Predictor

In order to compensate the effect of time delays generated from the new sampling strategy, the current control system with a simple WFP is proposed in Fig. 6. Compared with the predictive current controller shown in Fig. 4, a weight factor m has been introduced to the current feedback loop to mitigate the tracking errors due to the sampling delay. The predictive current at the endpoint of the Kth switching period can be obtained by a weighted filter prediction method which is given as

$$\hat{i}_g(K) = mi_A(K) + (1-m)i_g^*(K-1) \tag{9}$$

where $i_g^*(K-1)$ is reference current value for the $(K-1)$th switching cycle and the weight factor $m \in (0, 1]$.

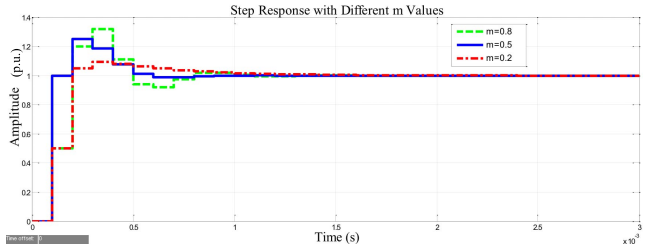

Fig. 7. Step response of predictive current controller with WFP when m varies.

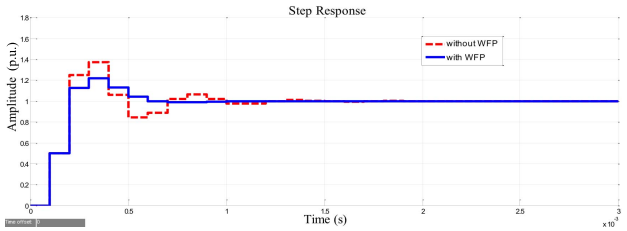

Fig. 8. Step responses of predictive current controller with and without WFPs.

The factor m is used to determine the extent of robust error cancelation as well as the dynamic performance of current control scheme. A larger m renders a faster transient response, but a higher amplitude of the overshoot, and vice versa, as shown in Fig. 7. When a proper value of m is selected, the proposed WFP can reduce the current tracking error to approximate m times smaller as the original, while providing the enough information about transient characteristic of the feedback current. The selection of m is highly dependent on the sampling strategy and the load requirement. In this paper, m is set to 0.5 for a grid-connected application, taking into account both compensation performance and system dynamics. Fig. 8 shows performance comparison of step responses of the predictive current controller with and without the time-delay compensation by the WFP, when $m = 0.5$ and $T_m = 0.5T_s$. The simulation result illustrates that the proposed WFP can provide a good compensation for time-delay effect featured in shorter settling time and lower overshoot amplitude.

B. Adaptive Voltage Compensator

Although the PCC with WFP exhibits robust control performance for the time-delay effect, the error of the grid-voltage estimation and the mismatch of system parameter modeling can also result in uncertain disturbances in a practical grid-connected VSI system and aggravate the system performance and stability, such as the filter inductance. Thus, to relax the assumption of no disturbance existence, an AVC is designed in this section to eliminate the steady-state errors caused by the system disturbances as well as enhance robustness of the system to parameter variations. As shown in Fig. 9, a voltage $\hat{\Delta}(K+1)$ has been added to the current control scheme as disturbance compensation by the proposed AVC. As a result, the reference value of the output voltage of the inverter in the $(K+1)$th switching period can be given by

$$v_{ab}^*(K+1) = \frac{L_m}{T_s}\left[i_g^*(K+1) - \hat{i}_g(K)\right] + \hat{\overline{v}}_g(K+1) + \hat{\Delta}(K+1) \quad (10)$$

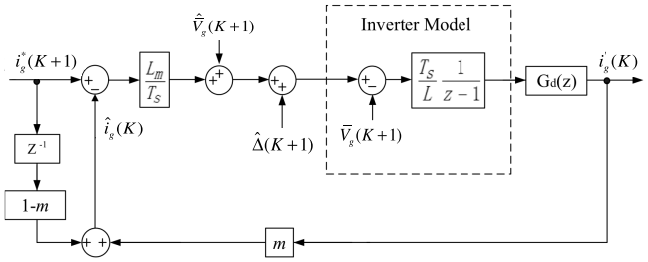

Fig. 9. WFP-based PCC scheme with disturbance compensation.

where L_m is the modeling (or nominal) value of the filter inductance.

Assuming that the actual inverter output current is consistent with the reference value by a proper PWM technique, the operation of the grid-connected VSI can be expressed as

$$v_{ab}^*(K+1) = \frac{L}{T_s}[i_g(K+1) - \hat{i}_g(K)] + \overline{v}_g(K+1). \quad (11)$$

When L_m is denoted by $K_L L$, where K_L is the mismatch coefficient, (11) can be rewritten as

$$\begin{aligned} v_{ab}^*(K+1) &= \frac{K_L L}{T_s}[i_g(K+1) - \hat{i}_g(K)] \\ &\quad + \frac{(1-K_L)L}{T_s}[i_g(K+1) - \hat{i}_g(K)] + \overline{v}_g(K+1). \end{aligned} \quad (12)$$

Solving (10) and (12) to obtain

$$\begin{aligned} \hat{\Delta}(K+1) &- \{[\overline{v}_g(K+1) - \hat{\overline{v}}_g(K+1)] \\ &+ \frac{(1-K_L)L}{T_s}[i_g(K+1) - \hat{i}_g(K)]\} \\ &= \frac{K_L L}{T_s}[i_g(K+1) - i_g^*(K+1)]. \end{aligned} \quad (13)$$

It is clear that the term of $\{[\overline{v}_g(K+1) - \hat{\overline{v}}_g(K+1)] + ((1-K_L)L/T_s)[i_g(K+1) - \hat{i}_g(K)]\}$ of (13) denotes the uncertain system disturbances due to the grid-voltage estimation error and the filter inductance mismatch during the $(K+1)$th switching cycle, which can be denoted by $\Delta(K+1)$ in this paper. Hence, the difference between the estimated voltage compensation and actual system disturbances can be formulated as

$$\hat{\Delta}(K+1) - \Delta(K+1) = \frac{K_L L}{T_s}\left[i_g(K+1) - i_g^*(K+1)\right]. \quad (14)$$

The error between the reference value and actual current at the end of each switching period indicates the gap in the compensation for the system disturbances. Thus, a complete compensation for system disturbances can be achieved by an appropriate disturbance voltage adaptation algorithm with this current error.

Considering that the variation of the system disturbances in adjacent switching periods is tiny due to the high switching frequency applied, the uncertain system disturbances in the $(K+1)$th switching period can be estimated by

$$\Delta(K+1) \approx \Delta(K). \quad (15)$$

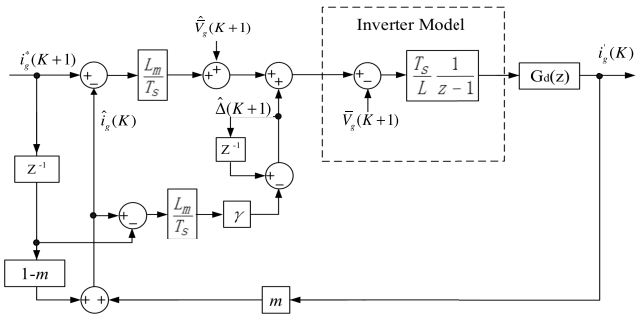

Fig. 10. Proposed robust PCC scheme.

Substituting (15) into (14) to yield

$$\begin{aligned}\hat{\Delta}(K+1) &\approx \frac{K_L L}{T_s}\left[i_g(K+1)-i_g^*(K+1)\right]+\Delta(K)\\ &= \frac{K_L L}{T_s}\left[i_g(K+1)-i_g^*(K+1)\right]+\hat{\Delta}(K)\\ &\quad -\frac{K_L L}{T_s}\left[i_g(K)-i_g^*(K)\right]. \end{aligned} \tag{16}$$

As current error between the actual measurement and reference value should be reduced progressively until rejected by the proposed iterating voltage compensation, $[i_g(K+1)-i_g^*(K+1)]$ can be defined as

$$\begin{aligned} i_g(K+1)-i_g^*(K+1) &= \left[i_g(K)-i_g^*(K)\right]\\ &\quad -\gamma\left[i_g(K)-i_g^*(K)\right] \end{aligned} \tag{17}$$

where $\gamma \in (0,1)$. A larger value of γ can accelerate the convergence of the control system, but may result in system instability. In practice, γ is chosen as 0.1 in this paper.

Then, the disturbance compensation during the $(K+1)$th switching period can be estimated by substituting (17) into (16) as

$$\hat{\Delta}(K+1) \approx \hat{\Delta}(K) - \frac{K_L L}{T_s}\gamma\left[\hat{i}_g(K)-i_g^*(K)\right] \tag{18}$$

where $i_g(K)$ is replaced by $\hat{i}_g(K)$ with WFP implementation.

Fig. 10 shows the proposed robust current control scheme with WFP and AVC. The AVC is developed based on the algorithm described in (18) which can be adopted to offer a complete voltage compensation for uncertain system disturbances. And Fig. 11 shows step responses of the proposed robust current controller with filter inductance mismatch. Compared with the traditional predictive controller without WFP and AVC, the simulation results illustrate that the proposed robust current control scheme is effective to reject the uncertain system disturbances and enhance the system robustness to parameter variations.

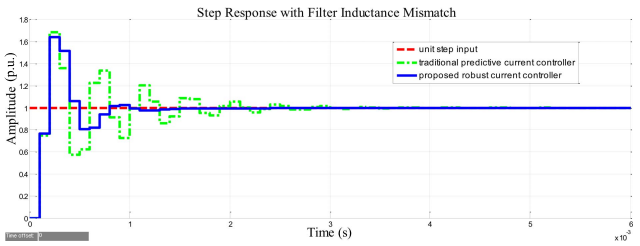

Fig. 11. Step response of the proposed PCC scheme with filter inductance mismatch ($K_L = 1.5$).

V. Stability Analysis

From the proposed PCC scheme shown in Fig. 10, the grid voltage acting as system disturbance is assumed to be completely compensated by the proposed AVC; hence, the analysis in this section is to concentrate on the system stability and robustness for the current loop within a filter inductance mismatch.

The closed-loop transfer functions of the proposed PCC scheme is given as (19).

The Jury stability criterion [25] has been adopted in this section to determinate the stability of the proposed control system by evaluating the coefficients of the system characteristic equation which is given by

$$\begin{aligned} F(z) &= z^3+(K_L m+K_L m\gamma-K_L K_d m-K_L K_d m\gamma-2)z^2\\ &\quad +(1+2K_L K_d m+K_L K_d m\gamma-K_L m)z-K_L K_d m. \end{aligned} \tag{20}$$

As a result, the system will be stable if all conditions shown in the following are satisfied:

$$\begin{cases} F(1)>0\\ F(-1)<0\\ |-K_L K_d m|<1\\ |(1+\gamma)[(K_L K_d m)^2-K_d(K_L m)^2]\\ \quad +K_L m-K_L K_d m\gamma-1|\\ <|(K_L K_d m)^2-1|. \end{cases} \tag{21}$$

As satisfied K_L for a stable system indicates a consecutive range of filter inductance variations, when $m, \gamma \in (0,1)$ and $K_d \in (0, 0.5)$ limited by a maximum switching frequency of 10 kHz, solve (21) to obtain

$$K_L < \min\left\{\frac{4}{(2m+m\gamma)(1-2K_d)}, \frac{2}{m}, \frac{1-K_d\gamma}{K_d m(1+\gamma-K_d\gamma)}\right\}. \tag{22}$$

It can be found that $(4/(2m+m\gamma)(1-2K_d))$ yields the minimum value when $K_d = 0$, while $(1-K_d\gamma/K_d m(1+\gamma-K_d\gamma))$ gets its minimum when $K_d = 0.5$. Thus,

$$G_c(z) = \frac{(K_L-K_L K_d)z^3+(K_L m-2K_L+K_L m\gamma-K_L K_d m+3K_L K_d-K_L K_d m\gamma)z^2+(K_L-K_L m-3K_L K_d+2K_L K_d m+K_L K_d m\gamma)z+K_L K_d-K_L K_d m}{z^4+(K_L m+K_L m\gamma-K_L K_d m-K_L K_d m\gamma-2)z^3+(1+2K_L K_d m+K_L K_d m\gamma-K_L m)z^2-K_L K_d m z} \tag{19}$$

TABLE I
ELECTRICAL PARAMETERS OF THE PROPOSED VSI

PARAMETER	Value
Rated power of the VSI	10 kW
Reference dc-link voltage (V_{dc}^*)	390 V
DC-link capacitors (C_{dc})	2050 μF
Output inductor (L)	1.6 mH
Grid voltage (V_g)	240 V
Grid frequency (f_0)	60 Hz

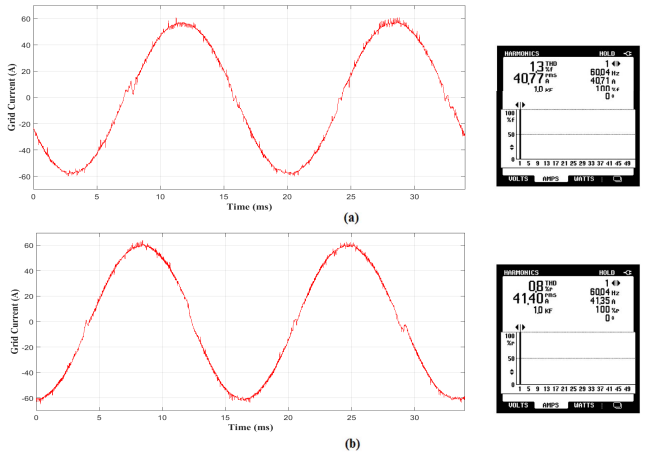

Fig. 12. Grid current waveform and THD performance at 10 kW with a switching frequency of 10 kHz. (a) With the linear PCC. (b) With the proposed PCC.

to stabilize the system with any time delay which is less than $0.5T_s$, the allowed K_L can be derived from (22) by evaluating the possible minimum value. As $\min\{(1-K_d\gamma\,/K_d m(1+\gamma-K_d\gamma)) < \min\{(4/(2m+m\gamma)(1-2K_d)) < (2/m)$, K_L is chosen for the stable control system as

$$K_L < \frac{1-0.5\gamma}{0.5m(1+0.5\gamma)}. \tag{23}$$

It is clear that lower values of m and γ can enhance the system robustness, however, hurt the system dynamic response. To achieve good quality in both robustness and fast response, values of m and γ are evaluated by practical experiments. In this paper, $m = 0.5$ and $\gamma = 0.1$. Thus, the system with the proposed current controller is stable for $0 < K_L \leq 3.6$. Compared with the traditional PCC with a stable range of $0 < K_L < 2$, the proposed control scheme significantly improves the system stability and robustness.

VI. EVALUATION RESULTS

To verify the performance of the proposed control scheme, experiments have been carried out on a laboratory platform of a 10-kW single-phase grid-connected inverter, whose electrical parameters are listed in Table I. Fig. 12 shows the quality of the grid current when the inverter works at 10 kW with a switching frequency of 10 kHz which has a fixed

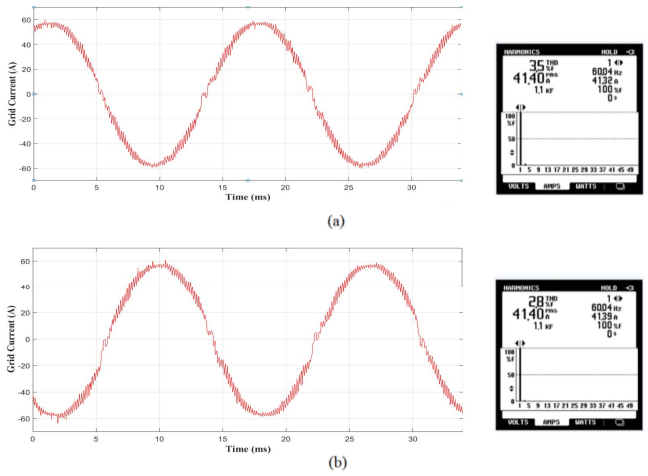

Fig. 13. Grid current waveform and THD performance at 10 kW with a switching frequency of 3 kHz. (a) With the linear PCC. (b) With the proposed PCC.

TABLE II
GRID CURRENT THDS WITH FILTER INDUCTANCE MISMATCH

K_L	Current THD (%) with linear PCC	Current THD (%) with proposed robust PCC
0.5	3.4	2.5
0.8	1.9	1.3
1	1.5	1.0
1.2	3.8	1.3
1.5	8.7	1.7
0.5	3.4	2.5

distribution of current measurements during each switching period. It can be seen that the current THD under the linear prediction was 1.3%, and improved by the proposed robust current controller which had a better THD of 0.8% shown in Fig. 12(b). Fig. 13 shows the performance of the VSI output current when the applied switching frequency is 3 kHz, which indicates that even though the sampling points are randomly distributed in every PWM period, the proposed PCC can also provide high quality output overcoming the limitations of linear extrapolation methods.

In addition, Figs. 14 and 15 illustrate the experimental comparison of the two current control schemes under the filter inductance mismatch conditions. When the inverter operated at 7 kW with a 10-kHz switching frequency, the modeling inductance of the filter L_m was set at five different values, which included the correct filter inductance L, $(1 \pm 20\%)L$ and $(1 \pm 50\%)L$. In Figs. 14 and 15, the scope measurements of grid current (i_g) were processed by a low-pass filter with a cutoff frequency of 5 kHz for observation. The THDs of output grid current are summarized in Table II, which indicate when $K_L < 1$, which means that the modeling inductance is smaller than the actual one; two current control algorithms show comparable results, while when $K_L > 1$, the proposed current control scheme exhibits a much better robustness characteristic for the filter inductance mismatch.

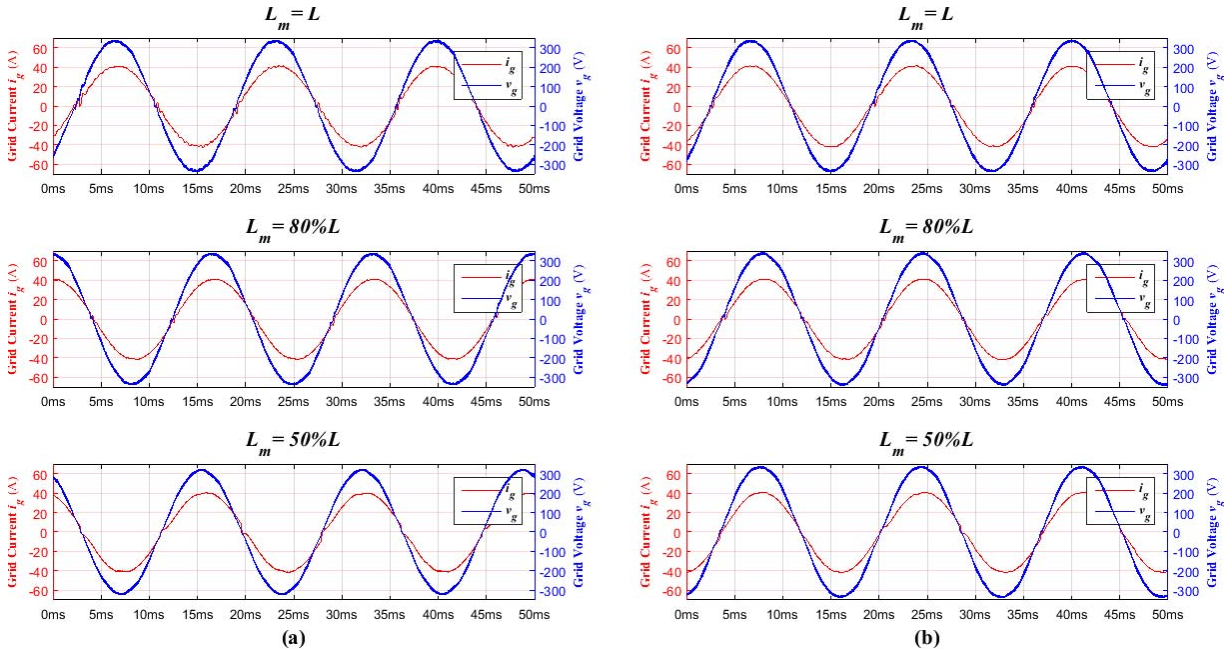

Fig. 14. Waveforms of grid current and voltage when $K_L \leq 1$. (a) With the linear PCC. (b) With the proposed PCC.

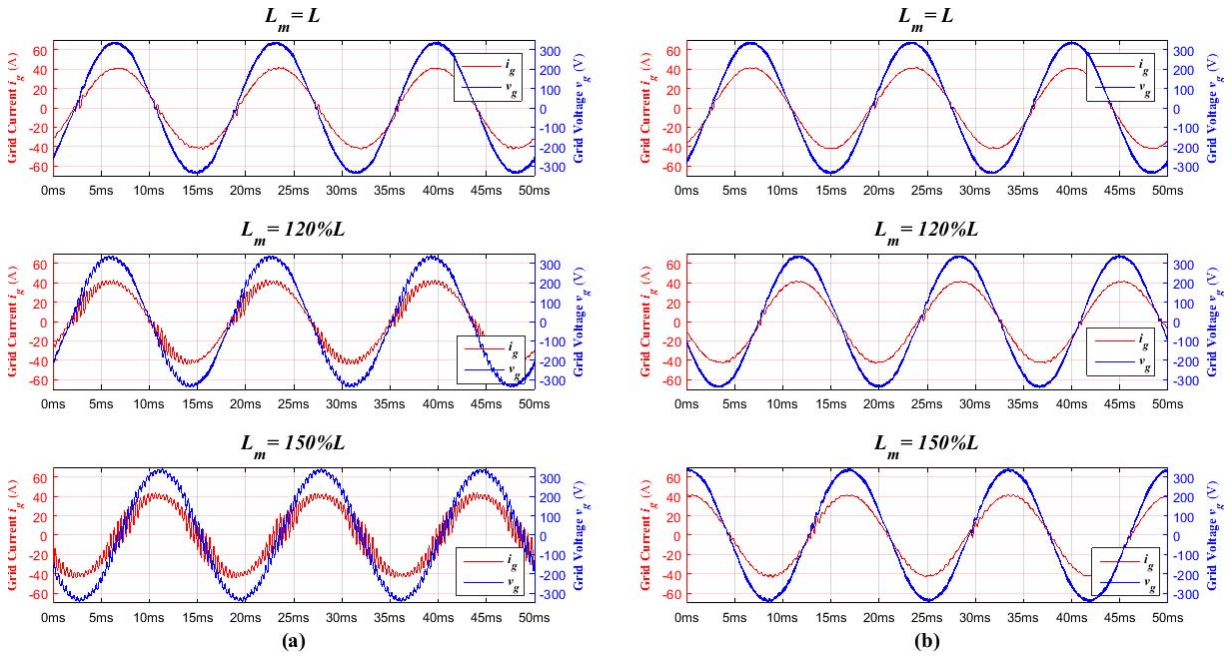

Fig. 15. Waveforms of grid current and voltage when $K_L \geq 1$. (a) With the linear PCC. (b) With the proposed PCC.

VII. Conclusion

In this paper, a robust current control scheme is designed for grid-connected VSIs to improve the quality of the current fed to the grid as well as enhance the system stability and robustness. The proposed control scheme is developed from the traditional predictive current controller along with a WFP and an AVC. The WFP instead of the linear prediction method is primarily used to attenuate the amplified effect of time delays when the switching period is short or not a multiple of the sampling cycle. And the AVC is implemented to provide a complete compensation for system disturbances which include estimation errors for the grid voltage and variations of system parameters through an adaptive voltage control. The performance of the proposed control scheme is verified by the experimental results of a 10-kW single-phase grid-connected inverter prototype.

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