Improved Reliability of Planar Power Interconnect With Ceramic-Based Structure

Hui Zhang, Jianfeng Li, Jingru Dai, Martin Corfield, Xuejian Liu, Yan Liu, Zhengren Huang, and Christopher Mark Johnson, *Member, IEEE*

***Abstract*— This paper proposes an advanced Si_3N_4 ceramic-based structure with through vias designed and filled with brazing alloy as a reliable interconnect solution in planar power modules. Finite-element (FE) modeling and simulation were first used to predict the potential of using the proposed Si_3N_4 ceramic-based structure to improve the heat dissipation and reliability of planar interconnects. Power cycling tests and nondestructive microstructural characterization were then performed on Si_3N_4 ceramic-based structures, flexible printed circuit boards (PCBs), and conventional Al wire interconnect samples to evaluate the FE predictions. Both the FE simulations and experimental tests were carried out on single Si diode samples where both the ceramic-based structures and flexible PCBs were bonded on the top sides of Si diodes with eutectic Sn-3.5Ag solder joints. The results obtained demonstrate that Si_3N_4 ceramic-based structures can significantly improve the reliability of planar interconnects. The experimental average lifetimes and FE simulated maximum creep strain accumulations for the ceramic-based structure and flexible PCB interconnect samples can reasonably be fitted to existing lifetime models for Sn-3.5Ag solder joints. Discrepancies between the models and experimental results can be attributed to defects and poor filling of the brazing alloy in the vias through the Si_3N_4 ceramic.**

***Index Terms*— Electronic packaging, finite-element (FE) method, material reliability, planar power module, power cycling, X-ray computation tomography.**

I. Introduction

In A typical conventional power module, Si or SiC power devices are attached on a ceramic-based substrate with solder joints for achieving sufficient mechanical support and electrical insulation between the electrical circuit tracks and the cooling unit, commonly including a base plate and heat sink [1]. Ultrasonically bonded Al wires in combination with soldered bus bars are generally used to achieve the interconnections. However, wire bonds and bus bars have limited ability to dissipate heat and have relatively high parasitic inductance, which often restricts the thermal and electrical performance of the power module [2], [3]. Furthermore, from the viewpoint of manufacturing, multiple soldering and wire bonding steps are not efficient and cost effective for assembling power modules which often have hundreds of wire bonds. To overcome these problems for the development of high power density and high reliability power modules, several alternative packaging structures based on different interconnect technologies have been proposed and investigated. These interconnect technologies include ribbon bond [2], embedded chip technology [4], [5], metal postinterconnect parallel-plate structure [1], [6], [7], dimple array interconnect [3], planar interconnect technology [8]–[10], pressure contact technology [11], flexible printed circuit board (PCB)-based packaging technology [12]–[14], and press pack technology [15]–[17].

The planar interconnect power modules have been demonstrated not only to obtain dramatic improvement in the thermal and electromagnetic performance, but also allow for efficient and low-cost manufacturing processes [8]–[10]. However, despite promising work in the selection of materials, manufacturability and reliability for the implementation of this interconnect technology is still needed for wider acceptance and commercialization. For example, metals, alloys, or flexible PCBs (metal/polymer laminates) have been used as interconnect materials, and joined on the top sides of Si or SiC devices and/or ceramic-based substrates. These joints may be formed using conventional Sn-based solder alloys, i.e., eutectic or near eutectic Sn–Ag or Sn–Ag–Cu alloys, or the emerging Ag sintering technology. Because of the mismatch in coefficients of thermal expansion (CTEs) between the interconnect materials with higher CTEs and the power devices and the substrates with lower CTEs, thermal stress and inelastic strain develop in the solder joints and the sintered Ag joints during the assembly process and in subsequent service environments. In such a case, the solder joints or the sintered Ag joints (whichever is used to join the interconnect structure) will be potential thermomechanical weak points in the assembled planar interconnect power modules.

In this paper, advanced Si_3N_4 ceramic with designed through vias has been proposed to provide the necessary insulation and to control the CTE of conductive Cu tracks for achieving reliable planar interconnects. The through vias

Manuscript received December 23, 2016; revised June 16, 2017; accepted September 24, 2017. Date of publication November 13, 2017; date of current version January 31, 2018. This work was supported by the Engineering and Physical Sciences Research Council, U.K., through the Centre for Power Electronics (grants for the hub and components theme), under Grant EP/K035304/1 and Grant EP/K034804/1. Recommended for publication by Associate Editor Ron Hui. *(Corresponding author: Jianfeng Li.)*

H. Zhang, X. Liu, Y. Liu, and Z. Huang are with the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai 201899, China (e-mail: zhanghui@mail.sic.ac.cn; xjliu@mail.sic.ac.cn; stony2000@mail.sic.ac.cn; zhrhuang@mail.sic.ac.cn).

J. Li, J. Dai, M. Corfield, and C. M. Johnson are with the Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham NG7 2RD, U.K. (e-mail: Jianfeng.Li@nottingham.ac.uk; eexjd11@exmail.nottingham.ac.uk; Martin.Corfield@nottingham.ac.uk; Mark.Johnson@nottingham.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JESTPE.2017.2758901

are filled with a conductive brazing alloy with subsequent conductive Cu tracks bonded on the ceramic using active brazing technology. The main objective of this paper is to demonstrate the reliability of such an innovative ceramic-based interconnect technology through comparison with conventional Al wire-bond technology and flexible PCB interconnect technology under similar power cycling conditions. A comparison has been carried out using both finite-element (FE) simulations and experimental tests on single Si diode samples where both the ceramic-based and flexible PCB interconnects were bonded on the top sides of Si diodes with eutectic Sn-3.5Ag solder joints. However, the results obtained can readily be applied to power modules which contain multiple power devices constructed with these interconnect technologies.

II. Finite-Element Modeling and Simulation

Before preparation of any samples, FE thermal and thermomechanical modeling and simulation have been used to predict the potential of the proposed Si_3N_4 ceramic-based structure to improve the heat dissipation and reliability of planar interconnects using commercial available FE analysis software Abaqus 6.14-1 and its graphic user interface CAE.

A. Description of Samples for Power Cycling Tests

This paper is mainly concerned with ceramic-based interconnect technology, where conventional Al wire bonding and emerging flexible PCB interconnect technologies are employed as benchmarks. Fig. 1 shows computer-aided design images of single Si diode samples, which are constructed with the three interconnect technologies for both the FE simulation and the power cycling tests. For all samples, the Si diode is attached on an AlN-based substrate with 100-μm-thick Sn-3.5Ag solder joint. The Si diode is 13.5 mm $\times$ 13.5 mm $\times$ 0.5 mm in size, and the AlN-based substrate is 58.2 mm $\times$ 49.5 mm $\times$ 1 mm thick AlN ceramic tile with 0.3-mm-thick Cu tracks actively brazed on both sides.

For each of the Al wire bond interconnect samples, 10 Al wires (375 μm in diameter) are bonded on the top anode of the diode at one end, and on the substrate at the other end. In each of the flexible PCB interconnect samples, a 13.5 mm $\times$ 13.5 mm $\times$ 0.5 mm Cu post is attached with a 100-μm-thick Sn-3.5Ag solder joint on a Cu island of the substrate. A 30 mm $\times$ 13.5 mm flexible PCB is soldered on the top sides of both the Si diode and the Cu post with Sn-3.5Ag solder joints for achieving the interconnect, where the thickness of the solder joints is also 100 μm. The flexible PCB consists of 100-μm-thick polyimide laminated with 50-μm-thick Cu tracks on both sides. As shown in Fig. 2(a), the vias (0.5 mm in diameter) in the flexible PCB are through the bottom Cu tracks and the polyimide layer, and are filled with Sn-3.5Ag solder alloy.

As shown in Fig. 2(b), in each of the ceramic-based interconnect samples, a Si_3N_4 ceramic-based structure is soldered on the top sides of both the Si diode and a Cu post with 100-μm-thick Sn-3.5Ag solder joints. The Si_3N_4 ceramic tile is selected due to its high strength and thermomechanical reliability. It is 0.3 mm in thickness, and the through vias (0.5 mm in diameter) are filled with a conductive brazing alloy with subsequent conductive Cu tracks bonded on it using active brazing technology. The brazing alloy is Ag-35.25Cu-1.75Ti, and 0.05-, 0.1-, and 0.2-mm-thick Cu tracks are considered. Different combinations of Cu tracks and insulation/support

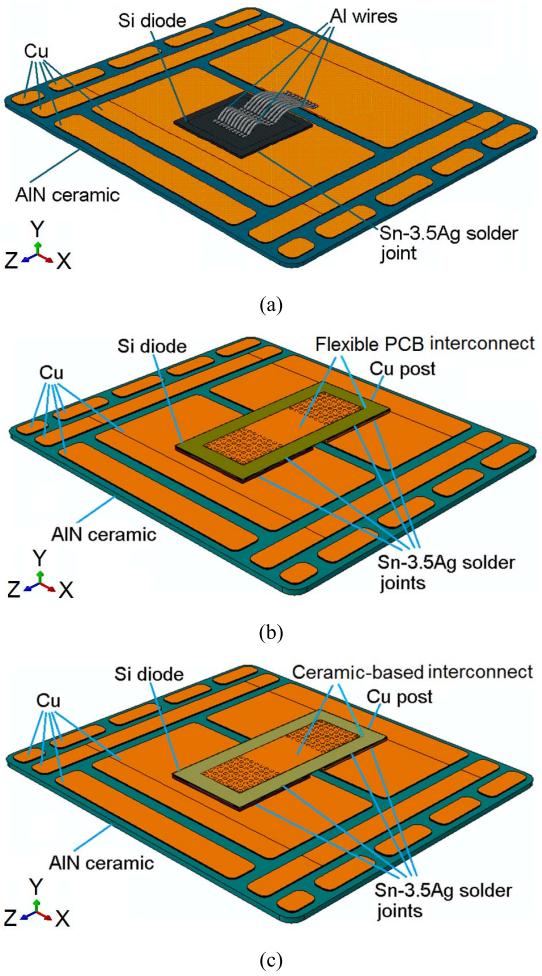


Fig. 1. Computer-aided design graphs of the single Si diode samples with the three types of interconnect technologies. (a) Al wire. (b) Flexible PCB. (c) Si_3N_4 ceramic-based structure.

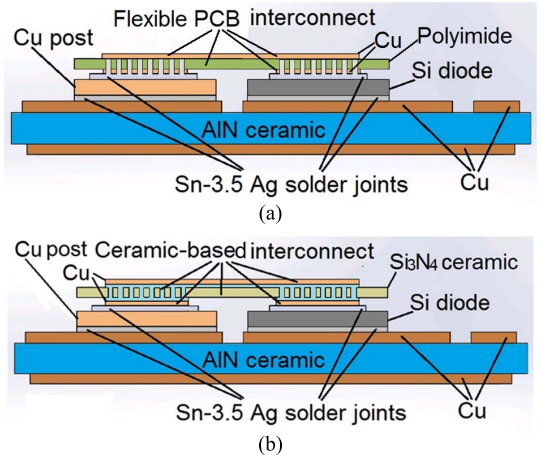


Fig. 2. Cross-sectional schematics of the single Si diode samples with planar interconnects. (a) Flexible PCB. (b) Ceramic-based structure.

TABLE I
CODES AND THE CORRESPONDING COMBINATIONS OF Cu TRACKS AND INSULATION/SUPPORT LAYERS IN THE FLEXIBLE PCB AND CERAMIC-BASED STRUCTURE

Code	Bottom Cu tracks	Insulation/support	Top Cu tracks	Via filling
Flex PCB	0.05 mm thick Cu	0.1 mm thick polyimide	0.05 mm thick Cu	
ACT1	0.1 mm thick Cu	0.3 mm thick Si_3N_4 with true CTE of 3 ppm/°C	0.1 mm thick Cu	Perfect
ACT2	0.2 mm thick Cu	0.3 mm thick Si_3N_4 with true CTE of 3 ppm/°C	0.2 mm thick Cu	Perfect
ACT3	0.1 mm thick Cu	0.3 mm thick Si_3N_4 with true CTE of 3 ppm/°C	0.1 mm thick Cu	Imperfect
ACT4	0.05 mm thick Cu	0.3 mm thick Si_3N_4 with true CTE of 3 ppm/°C	0.2 mm thick Cu	Perfect
ACT5	0.1 mm thick Cu	0.3 mm thick Si_3N_4 with assumed CTE of 6 ppm/°C	0.1 mm thick Cu	Perfect
ACT6	0.1 mm thick Cu	0.3 mm thick Si_3N_4 with assumed CTE of 9 ppm/°C	0.1 mm thick Cu	perfect

layers considered for the flexible PCB and the Si_3N_4 ceramic-based structures are listed in Table I.

It should be noted that AlN ceramic which has a higher thermal conductivity and is more commonly used as a support substrate in power electronic packaging is not suitable for forming through vias designed and filled with brazing alloy. This is because it has a relatively weak mechanical strength, and is easily broken during laser drilling/cutting to produce the through vias. In [18], Si_3N_4-based substrates with four through vias mechanically filled with Cu cylinders were used to construct planar half bridge modules. However, the vias were not directly on the top sides of the power devices, and the reliability of the constructed modules was not tested.

On the other hand, it is well known that Si_3N_4 ceramic has better reliability, but poorer thermal performance than AlN ceramic under similar thermomechanical loads. This paper is concerned with the reliability of top side interconnects of 0.5-mm-thick Si diodes which have been attached on AlN-based substrates. In the case of conventional Al wire bonds as top side interconnects, failure is dominated by the inelastic strain development in the Al wire bond due to mismatch of CTEs between Al and Si. If the substrate is changed to thinner Si_3N_4 ceramic (i.e., 0.32-mm or 0.64-mm thick) from thicker AlN ceramic (i.e., 1-mm thick), heating current pulses with lower amplitude have to be used for achieving similar temperature profiles during the power cycling tests, while the inelastic strain development, and hence the reliability of the Al wire bonds would remain similar.

B. FE Models

For all the single Si diode samples described above, FE thermal models have been developed to simulate the temperature fields during 50 power cycles. In each sample, the top one third thickness of the Si diode was considered as the active region generating electrical heat, and two different volumetric heating sources were considered. The latter being the product of 50 current pulses with an amplitude of 90 A multiplied by the voltage drop across either a 2.5-kV Si diode (referred to as lower power diode because of lower forward voltage drop and power dissipation) or a 4.5-kV Si diode (referred to as higher power diode because of higher forward voltage drop and power dissipation) during the power cycling test. For each of the two heating sources, the ON time and OFF time during every current pulse was determined by achieving 40 °C and 120 °C as the low and high limits of the average temperatures on the hottest 5 mm × 5 mm top surface area on the sample. A convection heat exchange condition with a heat exchange coefficient of 575 $W \cdot m^{-2} \cdot k^{-1}$ was applied on the bottom surface of the AlN-based substrate.

The thermomechanical model is mainly concerned with the stress/strain developments within the solder joints in the flexible PCB and ceramic-based interconnect samples. During the simulation, each of the samples was first subjected to a predefined temperature profile of 192 °C down to 25 °C within 3 min to simulate the reflow process. The initial heating up stage of the reflow process was found to have negligible effects on the simulated stress/strain development in solder joints [19] and was, therefore, not considered. The eutectic Sn-3.5Ag solder alloy has a melting point of 221 °C, and the solidification of the molten solder generally occurs at a supercooling temperature of 192 °C [20]. The temperature field simulated with the aforementioned thermal model was then used as inputs to simulate the further stress/strain developments in the sample during the 50 current pulses.

Similar meshing systems were employed to discretize all the samples, and the same meshing system was used for the thermal model and the thermomechanical models where applicable. Fig. 3 presents a representative meshing system consisting of 481820 DC3D6E linear triangular prism elements and C3D4 linear tetrahedron elements to discretize one ceramic-based interconnect sample. The smallest and the largest element sizes in the plane directions of the substrate are, respectively, 0.25 and 1 mm, and the smallest and the largest element sizes in the through-thickness direction are, respectively, 0.025 and 0.428 mm. In all the simulation cases, the elements used in the critical domains all have the same dimensions. For example, the sizes of the triangular prism elements used to discretize the critical solder joints whose maximum von Mises stress and creep strain accumulation will be used to assess the thermomechanical reliability are all 0.25 mm in the plane directions, and 0.025 m in the through-thickness direction. This is necessary because longer computing times would be required if meshing size-independent solutions were implemented for the present 3-D model with a much finer meshing system. Therefore, relatively coarse meshing systems with the same size of elements (in the critical domains for all the simulation cases) have been employed to achieve acceptable computing times.

The thermal and thermomechanical properties of the polyimide in the flexible PCB and the Si_3N_4 ceramic and brazing alloys in the ceramic–based structures are given in Table II. The brazing alloy between the Cu and AlN ceramic tile

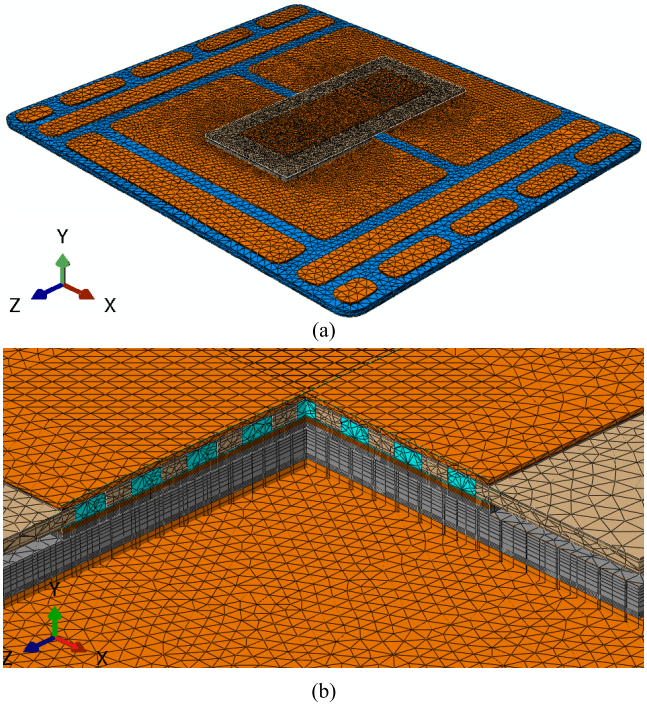


Fig. 3. Representative meshing system to discretize a ceramic-based interconnect sample. (a) Overview. (b) Locally enlarged view.

TABLE II
THERMAL AND THERMOPHYSICAL PROPERTIES OF PART MATERIALS IN THE SINGLE Si DIODE SAMPLES

	Polyimide	Si_3N_4	Ag35.25Cu1.75Ti
Thermal conductivity ($W \cdot K^{-1} \cdot m^{-1}$)	0.12	90	180
Specific heat ($J \cdot kg^{-1} \cdot °C^{-1}$)	1150	691	292
Density ($kg \cdot cm^{-3}$)	1.43	3.20	9.80
Young's modulus (GPa)	3.2	312	83
Poisson ratio	0.34	0.27	0.30
Yield strength (MPa)			271
Tensile/flexual strength (MPa)		700	346
Elongation (%)			20
CTE ($ppm \cdot °C^{-1}$)	11.6+0.12T	3.0	18.5

T is temperature in °C.

is ignored. The properties of the other materials used for the simulations were taken from [21]–[23], and are not repeated here. Of them, Chaboche's plastic model was used to describe the mechanical properties of both Al and Cu, and Anand's creep model was used to describe the mechanical properties of the Sn-3.5Ag solder joints. Only elastic deformation was considered for Si and AlN in all the samples.

For the Al wire bonds, flexible PCB and ceramic-based structures ACT1 and ACT2 interconnect samples, both lower and higher power Si diodes were considered, and the simulations are referred to as main simulations. For the ceramic-based structures ACT3, ACT4, ACT5, and ACT6, only higher power Si diode were taken, and the simulations are referred to as additional simulations. All the thermal and thermomechanical simulations have been executed on a PC computer with Intel[R] Core[TM] i7-3820 CPU at 3.60-GHz processor

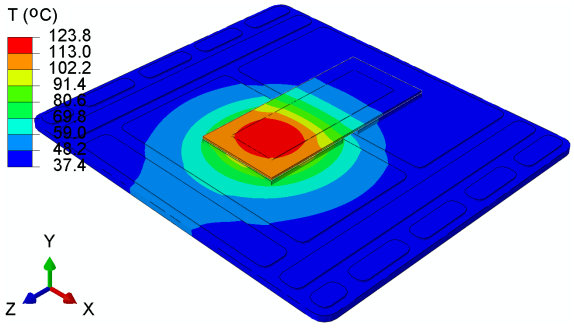


Fig. 4. Simulated distribution of temperature in the hottest ACT1 interconnected sample during one power cycle, where the Si diode is a lower power diode.

and 64-GB RAM. The running times for the thermal simulations were approximately 2 h and for the thermomechanical simulations 33 to 48 h for all cases.

C. FE Simulation Results

During the thermal simulation, the heat is generated within the active region of the Si diode, and hence this region is at a higher temperature than the rest of the regions in the sample. During the early stage of the transient simulation, the low and high limits of the average temperatures on the hottest 5 mm × 5 mm top surface area of all the samples were somewhat lower and gradually increased with increasing number of power cycles (current pulse with an amplitude of 90 A). After about 60 s of the transient simulation, they all reached the specified 40 °C and 120 °C during every power cycle. Fig. 4 shows an example of the simulated distribution of the temperatures in a sample during one such power cycle. Fig. 5 presents the heating power (heating source during the simulation) and the simulated evolution of the cyclic average temperatures on the hottest 5 mm × 5 mm top surface area of the flexible PCB interconnect sample for both lower power Si diode and higher power Si diode.

Fig. 6 compares the ON time and OFF time of the pulse current during every power cycle for the samples with both lower power diode and higher power diode to achieve the specified 40 °C and 120 °C as the low and high limits of the average temperatures on the hottest 5 mm × 5 mm top surface area of the assembled samples. It can be seen that with lower power Si diode, the flexible PCB interconnect sample has an ON time and OFF time similar to those of an Al wire interconnect sample. By contrast, the ceramic-based interconnect samples can increase the ON time by 28% to 38%, and increase the OFF time by 28% to 30%. With higher power Si diode, the flexible PCB interconnect sample can slightly increase both the ON time and OFF time by 8% compared to the Al wire interconnect sample. In comparison, the ceramic-based interconnect samples can increase the ON time by 34% to 52%, and the OFF time by 22% to 28% to an Al wire interconnect sample. The present thermal simulation has fixed the low and high limits of the temperatures. Therefore, if all the samples are subjected to the same current pulses, i.e., the same heating power, the ceramic-based interconnect samples would reduce the chip temperatures when

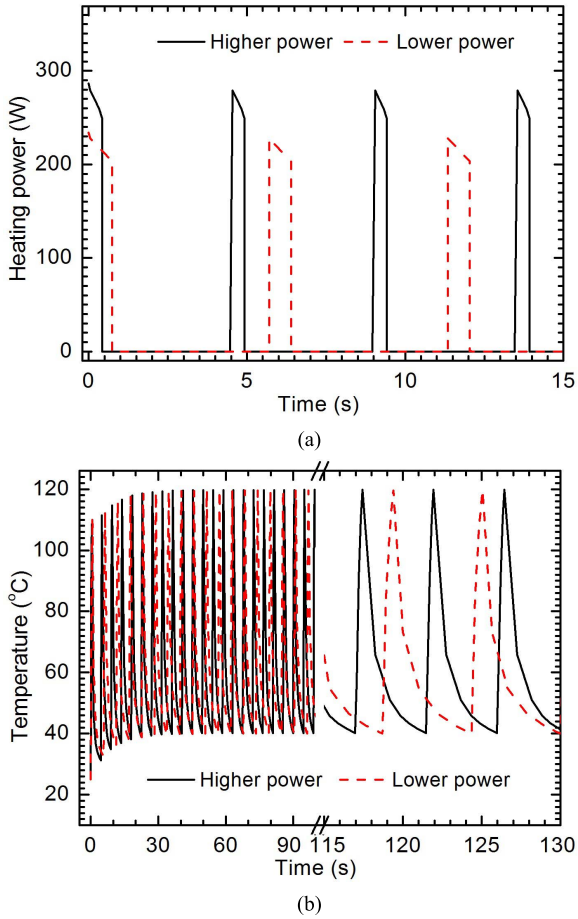


Fig. 5. Thermal simulation results of the flexible PCB interconnect sample with both lower power and high power Si diodes (a) heating power and (b) evolution of the cyclic average temperatures on the hottest 5 mm × 5 mm top surface area.

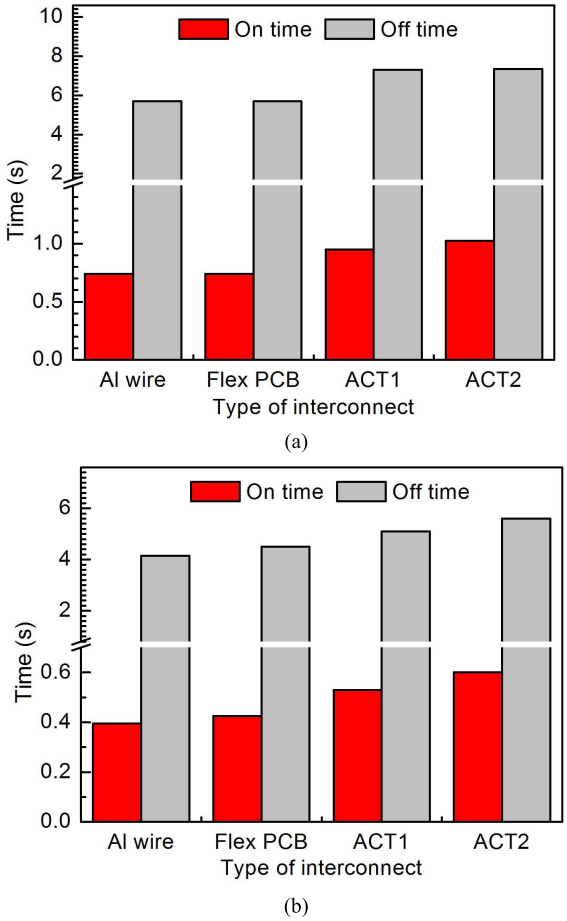


Fig. 6. Comparison of ON time and OFF time of pulse current during every power cycle for different samples with (a) lower power Si diode and (b) higher power Si diode to achieve the specified temperature profile.

compared with Al wire and flexible PCB interconnect samples. It should be iterated that in the thermal simulation the heat is assumed to be removed from the bottom side of the AlN-based substrate for all the samples. Therefore, it can be concluded that the ceramic-based interconnects indeed improve the ability of the samples to dissipate heat.

The thermomechanical simulation results indicate that in all the as-reflowed samples, the maximum Mises stress and maximum creep strain accumulation occur in the solder joints used to attach the Cu posts on the AlN-based direct bonded copper (DBC) substrates. This can be ascribed to the mismatch of CTEs between the Cu post and DBC substrate. During the power cycling, the maximum stress and creep strain accumulation have been moved to the solder joint used to bond the flexible PCB or the Si_3N_4 ceramic-based structures on the top sides of the diodes in all the simulation cases, especially near the interface between the solder and the Si diode. This can be explained by the higher cyclic temperatures encountered by this solder joint, as shown in Fig. 4, while both the flexible PCB and the Si_3N_4 ceramic-based structures still have higher CTEs than the Si diodes. Fig. 7 presents the simulated distributions of Mises stress and creep strain accumulation in all the solder joints in the ACT1 ceramic-based interconnect sample after 50 power cycles. The solder joint with the maximum Mises stress and the maximum creep strain accumulation is hence identified as the weakest solder joint.

Figs. 8 and 9 further compare the evolutions of the maximum Mises stress and the maximum creep strain accumulation in the weakest Sn-3.5Ag solder joint in all main simulations, where $\Delta\varepsilon_{ca}$ stands for the stable creep strain accumulation per power cycle. It can be seen that the cyclic range of the maximum Mises stress in the solder joint is remarkably affected by the cycle time. The sample with higher power Si diode and shorter cycle period has larger cyclic range of the maximum Mises stress than the corresponding sample with lower power Si diode and longer cycle period. This can readily be understood because the solder joints experience relatively low time-dependant creep deformation and relatively high elastic recovery with shorter cycle time than with longer cycle time.

By contrast, the maximum creep strain accumulation is more remarkably affected by the interconnect material and structure. The maximum creep strain accumulation per power cycle in the weakest solder joint in the sample with ACT1 ceramic-based structure is almost 50% lower than that in the

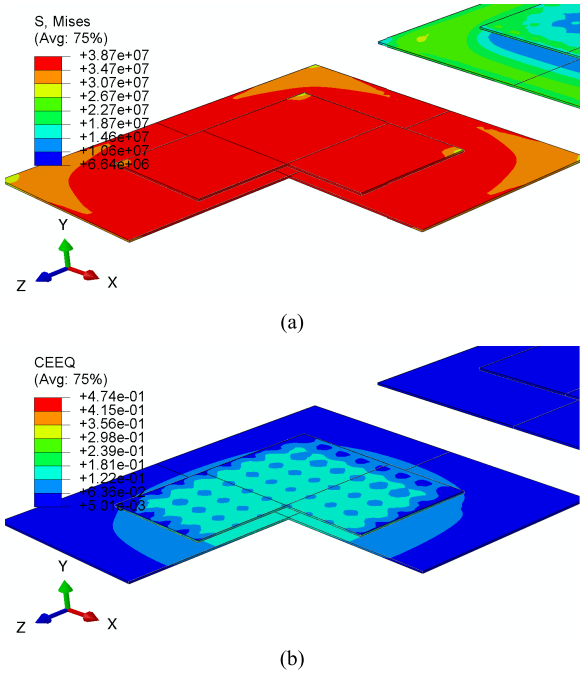


Fig. 7. Thermomechanical simulation results in all the solder joints in the ACT1 ceramic-based interconnect sample with higher power Si diode after 50 power cycles. (a) Distribution of Mises stress. (b) Distribution of creep strain accumulation.

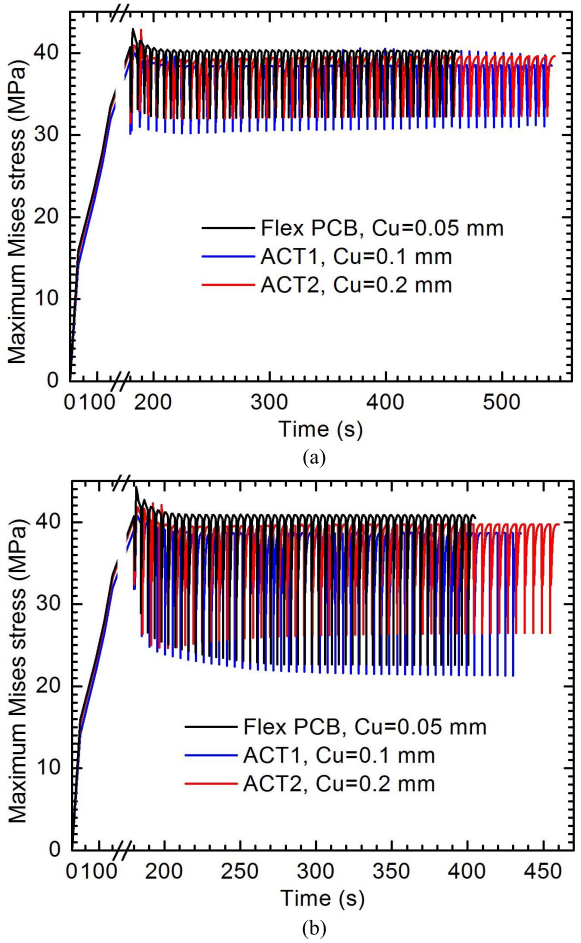


Fig. 8. Simulated maximum Mises stress in the weakest Sn-3.5Ag solder joint during the reflow process and 50 power cycles in the flexible PCB and ACT1 and ACT2 ceramic-based interconnect samples with (a) lower power Si diode and (b) higher power Si diode.

samples with flexible PCB and ACT2 ceramic-based structure. This result can be attributed to the fact that the creep strain development within the solder joint is closely associated with the CTE mismatch between the interconnect structure and the Si diode. The flexible PCB has higher CTE mismatch with the Si diode as expected, while the ACT2 ceramic-based structure also has higher CTE mismatch with the Si diode. The Si_3N_4 ceramic tile with the designed vias is less effective to control the CTE of 0.2-mm-thick Cu tracks than 0.1-mm-thick Cu tracks. In addition, it should be iterated that the thickness of the Cu tracks on the flexible PCB is 0.05 mm. If thicker, e.g., 0.1-mm-thick Cu tracks are applied, the creep strain accumulation in the solder joint will be significantly higher than the values presented in Fig. 9 for the flexible PCB.

In the thermomechanical simulation, the mechanical property of the solder joints have been described by the Anand viscoplastic model, and the simulated creep strains include both the creep and plastic deformation developments in the solder joints subjected to the power cycling. The lifetimes of the solder joints may hence be predicted with the following Engelmaier model [24]:

$$N_f = \frac{1}{2}\left(\frac{\Delta\varepsilon_{cr}}{2C_1}\right)^{1/C_2} \quad (1)$$

where N_f is number of cycle to failure, $\Delta\varepsilon_{ca}$ is the maximum creep strain accumulation per power cycle, C_1 is fatigue ductility coefficient, and C_2 is fatigue ductility exponent. As reported in [24]–[28], the fatigue ductility exponents for the eutectic or near eutectic Sn–Ag and Sn–Ag–Cu solder alloys are generally negative constants with absolute values less than one. Therefore, the present thermomechanical simulation results predict that the proposed Si_3N_4 ceramic-based structure with 0.1-mm-thick Cu tracks can significantly improve the reliability of the planar interconnect.

III. Experimental Evaluation

A. Sample Preparation and Power Cycling Tests

As shown in Fig. 6, the Al wire and flexible PCB interconnect samples with lower power Si diode and the ACT1 and ACT2 Si_3N_4 ceramic-based structure interconnect samples with higher power Si diode have similar cycle times when subjected to the simulated power cycling conditions and, thus, they were constructed and experimentally tested. The Al wire interconnect samples and both the lower power and higher power Si diodes were obtained from Dynex Semiconductor Ltd (Lincoln, U.K.). The as-received Si diodes have ~0.1/1/1-μm-thick Ti/Ni/Ag metallization on the cathode (back side) and ~5-μm-thick Al metallization on the anode (top side). They were processed to add ~0.1-/1-/1-μm-thick Ti/Ni/Ag trimetal on the existing ~5-μm-thick metallization on the top sides for making the flexible PCB and ceramic-based interconnect samples.

The flexible PCBs and AlN-based substrates were custom manufactured from Stevenage Circuits Ltd (Stevenage, U.K.)

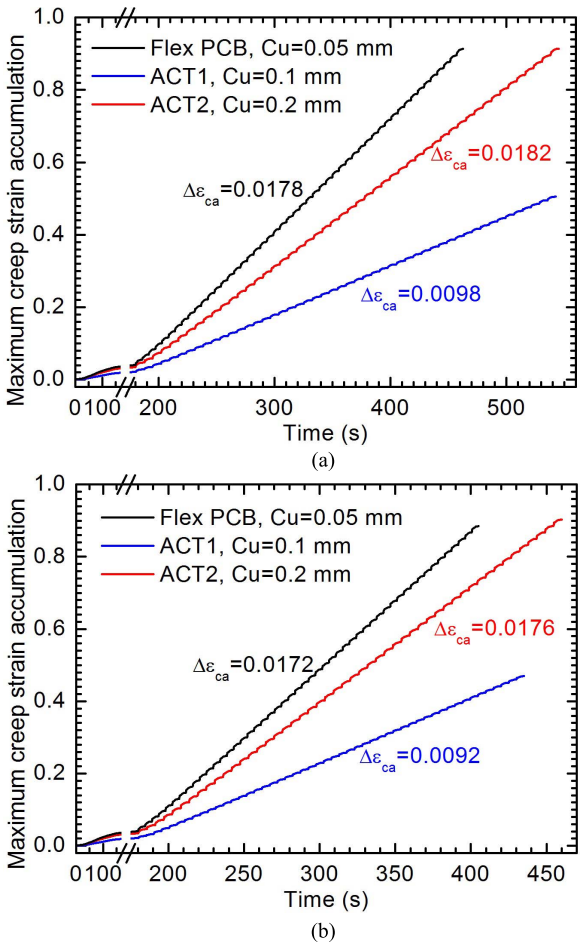


Fig. 9. Simulated maximum creep strain accumulation in the weakest Sn-3.5Ag solder joint during the reflow process and 50 power cycles in the flexible PCB and ACT1 and ACT2 ceramic-based interconnect samples with (a) lower power Si diode and (b) higher power Si diode.

and DOWA Metaltech Co., Ltd (Tokyo, Japan), respectively. For making the ceramic-based structure, 0.3-mm-thick Si_3N_4 ceramic tiles were prepared using the sintering process which is well established in Shanghai Institute of Ceramics. They were machined into the specified size of 30 mm × 13.5 mm and the designed vias were drilled with laser cutting. The ACT1 and ACT2 Si_3N_4 ceramic-based structures were formed by bonding 0.1- and 0.2-mm-thick Cu tracks on both sides of the machined Si_3N_4 ceramic tiles with Ag-25.25Cu-1.75Ti brazing alloy. The amount of the brazing alloy used on each structure was determined based on the total volume of the designed vias and 25-μm-thick brazing alloy between the ceramic tile and the Cu tracks. The brazing process was carried out in vacuum of 10^{-3} Pa and at 880 °C for 10 min.

The flexible PCB and ceramic-based interconnect samples were assembled using the same solder reflow process. 100-μm-thick Sn-3.5Ag solder performs were placed between the surfaces to be bonded together, as shown in Fig. 2. The Sn-3.5Ag solder joints were formed by reflowing in vacuum of 500 Pa and at a peak temperature of 260 °C for 5 min.

Power cycling tests were carried out on prepared single Si diode samples using a bespoke power cycling rig, where

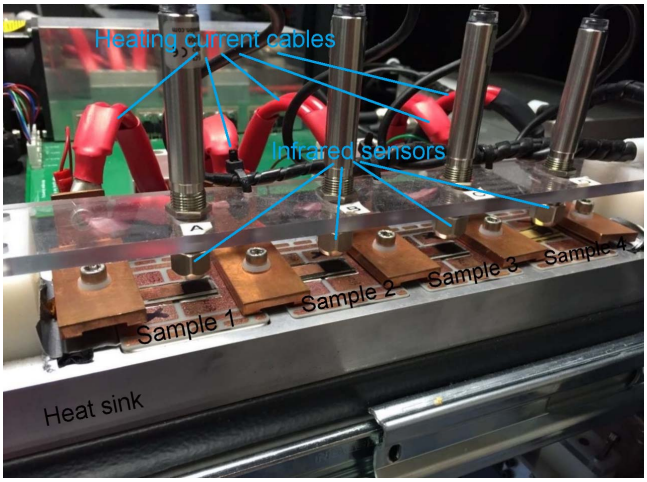


Fig. 10. Photograph of four samples installed on the power cycling test rig.

10 to 12 samples for each of the four types of samples were tested. Fig. 10 shows an example image of four samples installed on the testing rig; heated by passing current pulses with a ampitude of 90 A through the diodes and cooled by mecahnically mounting on a cold plate of a water-based heat sink. The temperatures on the top sides of the samples were monitored with infrared sensors. The cyclic temperatures were set between 40 °C and 120 °C for all the samples, while the switching of the current pulses through each of the sanples were controlled independently. During the test, the cycle number, cycle time, duty cycle (ratio of heating time to cycle time) and forward voltage drop across the diode at 120 °C were collected. The failure of the samples was considered by a 20% increase in the forward voltage.

After the power cycling test, both visual observation and nondestructive structural characterization were used to check the location and mechanism of any failures. The lattter was carried out using 3-D X-ray computed tomography (CT) imaging on an Xradia Versa XRM-500 CT system.

B. Experimental Results

During the power cycling tests, typical average cycle times for all the samples were in the range of 5 to 6 s, and duty cycles of between 9% and 12%. These were in reasonable agreement with the thermal simualtion results, as shown in Figs. 5 and 6. Fig. 11 presents representative cycle times and forward voltage measurements collected during the power cycling tests. The flutuations (or noise) on the curves of cycle time versus number of power cycles were mainly associated with the thermal interface between the samples and cold plate of the water-based heat sink. This is becasue the samples were only mechanically mounted on the cold plate to achieve sufficient thermal resistance, and hence short cycle times. The criterion of power cycling to failure was set as 20% increase in the forward voltage drop across the Si diode. Once the forward voltage drop of a sample increased to 20%, it further increased rapidly and significantly until the sample failed to open circuit, as can be seen from Fig. 11(b).

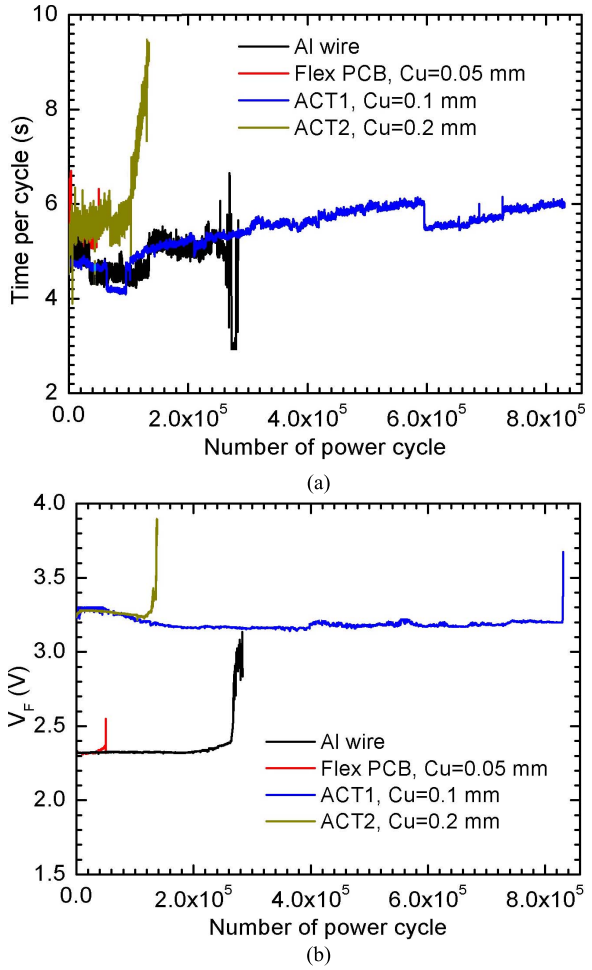


Fig. 11. Representative curves of the collected parameters versus number of power cycle during the power cycling tests. (a) Cycle time. (b) Forward voltage drop across the Si diode.

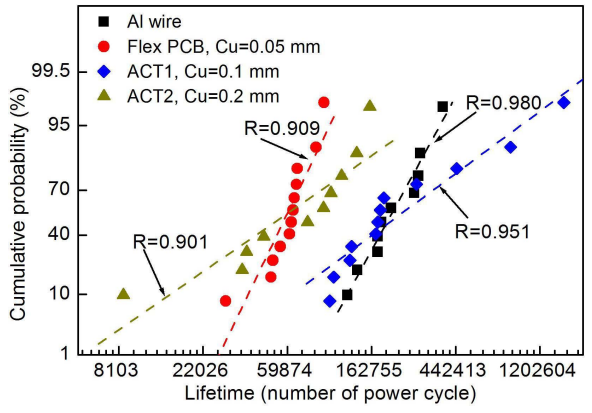


Fig. 12. Comparison of the lifetimes of all the samples obtained during the power cycling tests.

Fig. 12 presents the curves of cumulative probability on the logarithm-normal probability coordinates for the lifetimes obtained from the four types of samples during the power cycling test. Here, the R values stand for the coefficients of correlation for the linear data fittings. The cumulative probability for each measured data set $f(i)$ was calculated

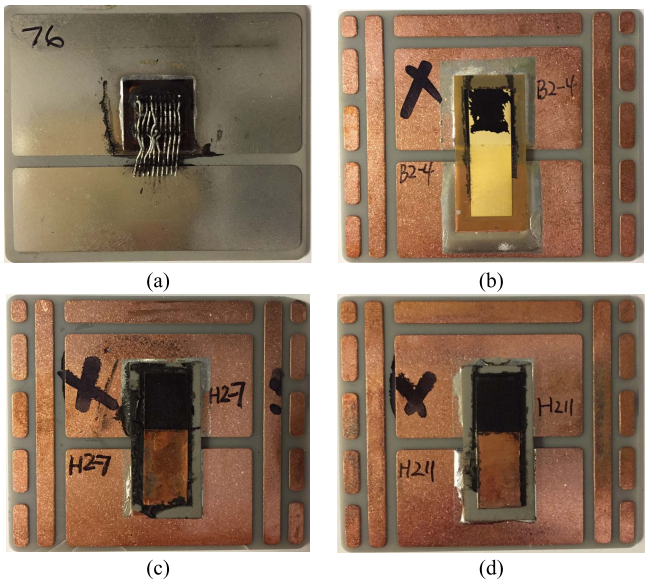


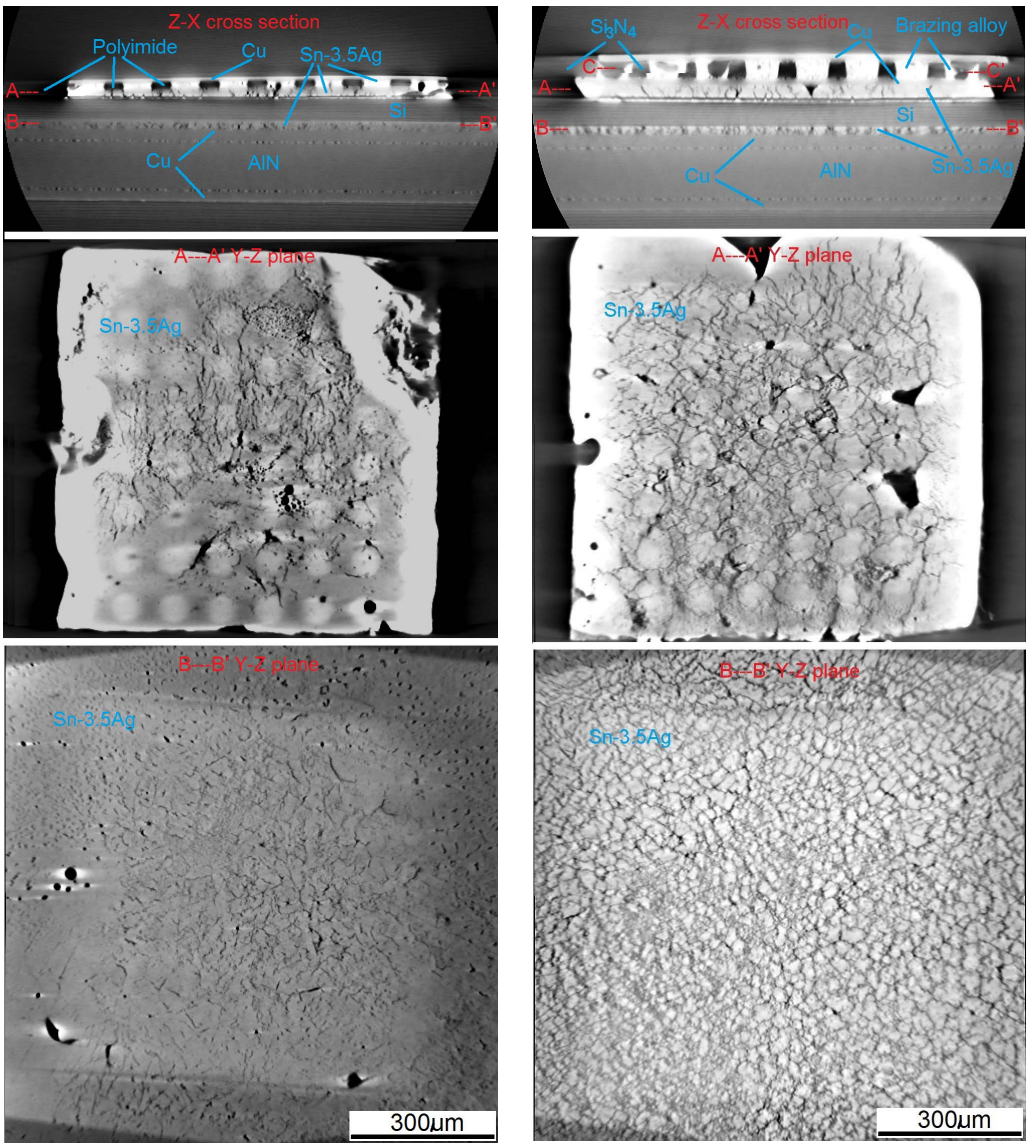
Fig. 13. Photographs taken from the failed samples interconnected with (a) Al wire, (b) flexible PCB, (c) ceramic-based ACT1, and (d) ceramic-based ACT2.

from placing the data of the lifetimes in ascending order and letting

$$f(i) = \frac{i - 0.5}{n} \times 100\% \tag{2}$$

where n is the total number of data points for each type, and i is the ith order in ascending data set [10]. The lifetimes of the four types of samples statistically follow the Logarithm-Normal distribution quite well. In particular, the planar flexible PCB and ACT2 ceramic-based interconnect samples have lifetimes shorter and, thus, less reliable than conventional Al wire interconnect samples. By contrast, the ACT1 ceramic-based samples have lifetimes comparable with and significantly longer than the conventional Al wire interconnect samples.

Both visual observation and microstructure characterization reveal that all the samples failed within the interconnects during the power cycling test. Fig. 13 shows photographs taken from four failed samples. The Al wire interconnect samples failed due to wire-bond lift off from the top sides of the Si diodes. The relevant mechanisms are well investigated in [29] and [30] and are, therefore, not repeated here. All the flexible PCB and ceramic-based interconnect samples failed within the solder joints used to bond the interconnect structures on the top sides of the Si diodes (near the solder/Si interfaces). Such a result is in excellent agreement with the weakest point identified by the simulated maximum creep strain accumulation, as shown in Fig. 7. Fig. 14 presents reconstructed X-ray CT images obtained from two representative samples after power cycling tests. The cracks leading to debonding of the flexible PCB and the ACT1 ceramic-based structure from the Si diodes can clearly be observed within the weakest solder joints (top interconnects A-A) near the solder/Si interfaces in both samples. Networked cracks separating the solder layers into a distinctive network of particles can also be seen in the weakest solder joints and also in the solder joints



(a) (b)

Fig. 14. Reconstructed X-ray CT images obtained from (a) flexible PCB interconnect sample with lifetime of 49 347 power cycles, and (b) ACT1 ceramic-based interconnect sample with lifetime of 850 062 power cycles.

that attach the Si diodes to the AlN-based substrate (lower interconnects B-B). These are typical of creep-induced fatigue cracks due to grain boundary sliding. These cracks are more developed in the weakest solder joints in the central areas where there should be relatively higher temperatures during the power cycling test, as shown in Fig. 4. This can easily be explained because the solder alloy at higher temperatures has lower resistance to grain boundary sliding than at lower temperatures.

Further structural characterization reveals that the filling of the brazing alloy in the vias through the Si_3N_4 ceramic tile in the samples with shorter lifetimes was relatively poor and less uniform than that in the samples with longer lifetimes. Fig. 15 shows reconstructed X-ray CT images obtained from 2 ACT1 ceramic-based interconnect samples with significantly different lifetimes. Here, the white phase around the vias indicates good filling of the brazing alloy, while dark phases indicate poor or lack of filling of the brazing alloy in the vias. Poor or lack of filling of the brazing alloy in the vias made the Si_3N_4 ceramic tile less effective to control the CTE of the Cu tracks. This is probably the reason why filling of the brazing alloy in the vias appears to correlate with the lifetimes and reliability of the ceramic-based interconnect samples. This can further be supported by additional FE simulation results as presented in Fig. 16, where the filling of the brazing alloy in the vias in an ACT3 ceramic-based structure was similar to the imperfect via filling, as shown in Fig. 15(a). The imperfect via filling increases around 10% of the simulated maximum creep strain accumulation in the weakest solder joint. During the simulation, both the bottom and top Cu tracks were assumed to be bonded on the Si_3N_4 ceramic tile perfectly, and hence the actual increase in the maximum creep strain accumulation

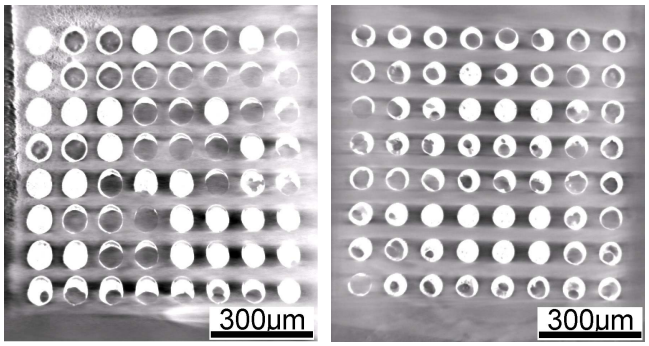


Fig. 15. Reconstructed C–C' *yz* plane [labeled in Fig. 14(b)] X-ray CT images obtained from the ACT1 ceramic-based interconnect samples with lifetimes of (a) 125 890 power cycles and (b) 447 971 power cycles.

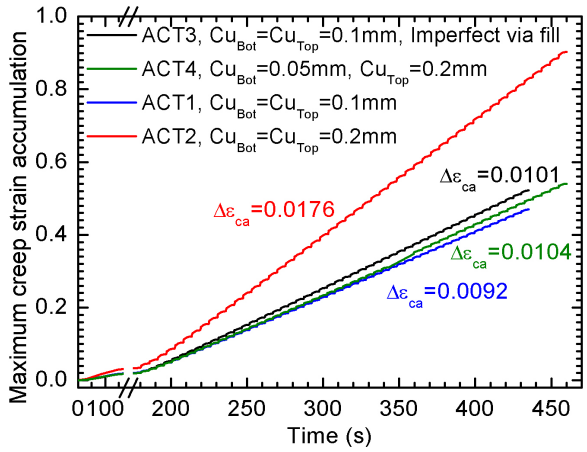


Fig. 16. Additional FE simulation results comparing the maximum creep strain accumulation in the weakest solder joint with the different ceramic-based interconnect structures during the reflow process and 50 power cycles.

might be higher if local imperfect bonding between the Cu tracks and the Si_3N_4 ceramic tile also exists. Practically, work is still ongoing to improve the filling of the brazing alloy in the through vias by considering different supplies of the brazing alloy and better process control. Another possibility may be the predeposition of thin metallic film, e.g., Ti/Ni/Ag or Ti/Ni/Au, to improve the wettability of the brazing alloy on the side walls of the through vias.

C. Discussion

As all the flexible PCB, and ceramic-based interconnect samples failed at the weakest solder joints through creep-induced fatigue cracks due to grain boundary sliding; the lifetimes of these samples can be described and predicted with an established lifetime model, e.g., (1) or other similar equations for Sn-3.5Ag solder joints. Combining the experimental average lifetimes with the simulated creep strain accumulations presented in Fig. 9, the fatigue ductility coefficient C_1 and fatigue ductility exponent C_2 in (1) can be extracted through data fitting, as shown in Fig. 17. The present $C_1 = 1.02$ and $C_2 = [-0.516$ to $-0.327]$ (90% confidence interval of C_2) are obtained.

In [24]–[28], the values of $C_1 = 0.045$ to 0.205 and $C_2 = -0.697$ to -0.323 for eutectic or near eutectic Sn–Ag

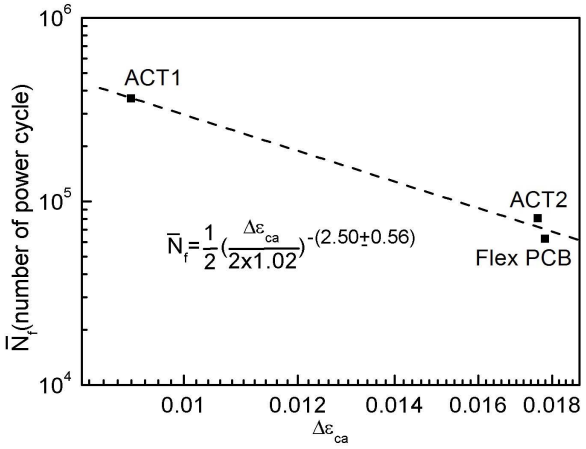


Fig. 17. Data fitting of the experimental average lifetimes and the FE simulated maximum creep strain accumulations to the lifetime model of the Sn-3.5Ag solder joint.

and Sn–Ag–Cu solder alloys were reported or can be calculated from the relevant data reported. The present fatigue ductility exponent is comparable with, but the present fatigue ductility coefficient is somewhat higher than those values. This may be related to the fact that the present power cycling tests with cycle times of 5 to 6 s and cyclic temperatures between 40 °C and 120 °C were quite different from reported previous tests. They reported passive thermal cycling tests with cycle times of 30 min to 1 h between −40 °C and 125 °C, −55 °C and 125 °C, and 0 °C and 100 °C [25], or isothermal tensile tests from 11 °C to 90 °C and strain rate range from 5×10^{-5} to 2×10^{-2} s^{-1} [28], or low-cycle fatigue tests at room temperature and strain ranges of 1.4%, 3%, 4%, and 7.5% [26].

As is well known, the fatigue ductility exponent and fatigue ductility coefficient of a solder alloy may be dependent on strain rate, temperature, as well as other secondary factors such as material structure and aging history [24]. The present data fitting, as shown in Fig. 17, was based on the simulated creep strain accumulation in the ceramic-based interconnect samples with perfect filling of the brazing alloy in the through vias, but the experimental average lifetimes are obtained from ceramic-based interconnect samples with defects and poor filling of the brazing alloy in the through vias. If experimental lifetimes are obtained from samples with perfect filling of the brazing alloy in the through vias the fatigue ductility exponent and fatigue ductility coefficient with values lower than the present absolute values are expected. These would then more approximately describe and predict the lifetimes of the weakest solder joints subjected to the power cycling conditions with short cycle times. Nevertheless, the present experimental results from samples with defects and poor filling of the brazing alloy in the through vias still have lifetimes similar to and even significantly better than conventional Al wire interconnect samples. Further additional FE simulation results indicate that the maximum creep strain accumulation in the weakest solder joints clearly increase with increasing CTE of the ceramic tile in the ceramic-based structure, see Fig. 18. Therefore, both the FE simulation results and the experimental tests demonstrate that the proposed Si_3N_4 ceramic-based structure is valid to

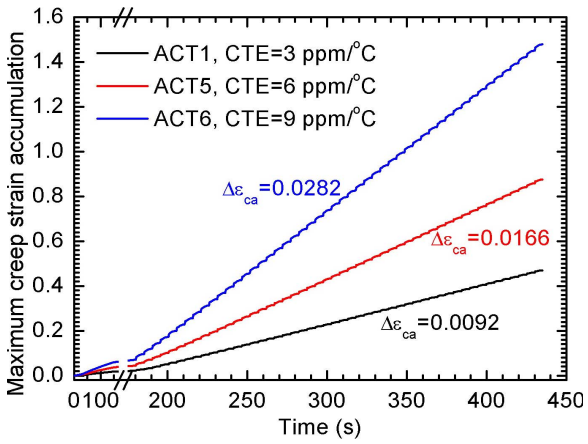


Fig. 18. Additional FE simulation results considering the effect of assumed CTE of the ceramic tile in the ceramic-based structure on the maximum creep strain accumulation in the weakest solder joint during the reflow process and 50 power cycles.

control the CTE, and hence improve the reliability of planar power interconnects.

Increasing the thickness of either the polyimide or the Cu tracks in the flexible PCB would result in lifetimes and reliability worse than those presented in Fig. 12 for the flexible PCB. Conversely decreasing the thickness of the polyimide and/or the Cu tracks in the flexible PCB may improve lifetime and reliability. However, this would also reduce the insulation or current carrying capability of the interconnect. In [3], dimple array interconnect based on dimples preformed on flexible PCB and solder bump as electrical connection was employed to eliminate the structural singularity at the solder/silicon interface and, thus, improve the reliability of the interconnect. However, the reported lifetime of 12 700 power cycles from 10 °C to 100 °C for this interconnect technology was still quite low. This can probably be attributed to the fact that the dimple array did not eliminate the mismatch of CTEs between the flexible PCB and the Si device, and the creep or inelastic strain development in the solder joint could still be quite high if the flexible PCB was above a certain thickness.

The Ag–Cu–Ti brazing alloy has a thermal conductivity and electrical conductivity much higher than the eutectic or near eutectic Sn–Ag and Sn–Ag–Cu solders alloys. With improved filling of the brazing alloy in the vias through the Si_3N_4 ceramic tile, the ceramic-based structure is expected to further improve the heat dissipation and thermomechanical reliability of planar power interconnects over conventional Al wire interconnects. For carrying higher currents, the ceramic-based structure can be designed with thinner Cu tracks on the side which will be bonded on to the power device and thicker Cu tracks on the other side, so as to still achieve high thermomechanical reliability. This assumption can be supported by the FE simulated maximum creep strain accumulation in the weakest solder joint for a ACT4 ceramic-based structure which is much lower than that for a ACT2 ceramic-based structure, as shown in Fig. 16. In addition, the ceramic-based structure also facilitates efficient and cost-effective manufacturing process to assemble planar power modules. The power die attachment and interconnect can be formed with a single soldering reflow step, rather than multiple soldering and wire bonding steps as used in assembling conventional power modules. Therefore, the presently proposed ceramic-based structure is promising as an alternative interconnect for the development of high performance, high reliability and cost-effective planar power modules.

In addition, it should also be pointed out that the current carrying capability of the flexible PCB and ceramic structure mainly depends on the cross-sectional area of their top side Cu tracks. In the present single Si diode samples, 0.05-mm-thick Cu track on the flexible PCB has current carrying capability worse than the Al wire bond consisting of 10 Al wires (375 μm in diameter). 0.1-mm-thick Cu track on the ceramic structure has current carrying capability similar to, and 0.2-mm-thick Cu track on the ceramic structure has current carrying capability better than the Al wire bond.

IV. Conclusion

Using conventional Al wire bonding technology and the flexible PCB technology as benchmarks, the proposed Si_3N_4 ceramic-based structure as a reliable interconnect solution in planar power modules has been investigated with both FE simulation and experimental tests. They have been carried out on single Si power diode samples, where both the ceramic-based structure and flexible PCB were bonded on the top sides of Si diodes with eutectic Sn-3.5Ag solder joints.

FE thermal simulation results predict that the Si_3N_4 ceramic-based structures with 0.1- and 0.2-mm-thick Cu tracks can both improve the heat dissipation during power cycling tests when compared with 0.375-mm diameter Al wires and flexible PCB with 0.050-mm-thick Cu track as the interconnect. This can be ascribed to the fact that the ceramic-based structures have higher thermal mass and thermal conductivity.

FE thermomechanical simulation results also predict that Si_3N_4 ceramic-based structures with 0.1-mm-thick Cu tracks can significantly reduce the creep strain accumulation and, thus, improve the thermomechanical reliability of the Sn-3.5Ag solder joint on the top side of the Si diode when compared with the flexible PCB with 0.05-mm-thick Cu tracks as the interconnect. This can simply be attributed to the effective constraint of CTE of the Cu tracks by the Si_3N_4 ceramic.

Power cycling tests verify that even with defects and poor filling of brazing alloy in the through vias, the prepared Si_3N_4 ceramic-based structure with 0.1-mm-thick Cu tracks can significantly improve the thermomechanical reliability of the Sn-3.5Ag solder joint on the top side of the Si diode when compared with the flexible PCB with 0.05-mm-thick Cu tracks as the interconnect. Single Si diode samples with ceramic-based interconnects have lifetimes which are comparable to and significantly longer than conventional Al wire interconnect samples.

The experimental average lifetimes and FE simulated maximum creep strain accumulations for the ceramic-based structure and flexible PCB interconnect samples can reasonably be fitted to existing lifetime models of Sn-3.5Ag solder

joints, Discrepancies between the model and experimental can be attributed to defects and poor filling of the brazing alloy in the vias through the Si_3N_4 ceramic.

Further discussion also suggests future design of the ceramic-based structure interconnect with thicker Cu tracks for carrying higher currents, and highlights that the ceramic-based structure facilitates an efficient and cost-effective manufacturing process to assemble planar power modules.

REFERENCES

[1] C. M. Johnson *et al.*, "Compact double-side liquid-impingement-cooled integrated power electronic module," in *Proc. 19th Int. Symp. Power Semiconductor Devices ICs*, Jeju, South Korea, May 2007, pp. 53–56.

[2] C. Luechinger, "Ribbon bonding—A scalable interconnect for power QFN packages," in *Proc. 9th Electron. Packag. Technol. Conf.*, Singapore, Dec. 2007, pp. 47–54.

[3] G.-Q. Lu, X. Liu, S. Wen, J. N. Calata, and J. G. Bai, "Strategies for improving the reliability of solder joints on power semiconductor devices," *Soldering Surf. Mount Technol.*, vol. 16, no. 2, pp. 27–40, 2004.

[4] J. Yin, Z. Liang, and J. D. van Wyk, "High temperature embedded SiC chip module (ECM) for power electronics applications," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 392–398, Mar. 2007.

[5] Z. Liang, B. Lu, J. D. V. Wyk, and F. C. Lee, "Integrated CoolMOS FET/SiC-diode module for high performance power switching," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 679–686, May 2005.

[6] L. Ménager, M. Soueidan, B. Allard, V. Bley, and B. Schlegel, "A lab-scale alternative interconnection solution of semiconductor dice compatible with power modules 3-D integration," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1667–1670, Jul. 2010.

[7] J. Lee, D. M. Fernandez, M. Paing, Y. C. Yeo, and S. Gao, "Electroless Ni plating to compensate for bump height variation in Cu–Cu 3-D packaging," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 6, pp. 964–970, Jun. 2012.

[8] R. Fisher, R. Fillion, J. Burgess, and W. Hennessy, "High frequency, low cost, power packaging using thin film power overlay technology," in *Proc. 10th Annu. Appl. Power Electron. Conf. Expo. Conf. (APEC)*, vol. 1. May 1995, pp. 12–17.

[9] B. Ozmat, C. S. Korman, P. McConnelee, M. Kheraluwala, E. Delgado, and R. Fillion, "A new power module packaging technology for enhanced thermal performance," in *Proc. 7th Intersoc. Conf. Thermal Thermomech. Phenomena Electron. Syst. (ITHERM)*, vol. 2. May 2000, pp. 287–296.

[10] K. Weidner, M. Kaspar, and N. Seliger, "Planar interconnect technology for power module system integration," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Mar. 2012, pp. 459–463.

[11] C. Göbl and J. Faltenbacher, "Low temperature sinter technology die attachment for power electronic applications," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, vol. 1. Mar. 2010, pp. 1–5, paper 10.

[12] N. Pluschke and P. Beckedahl, "Novel packaging technology for power modules," in *Proc. IEEE Int. Symp. Ind. Electron. (ISIE)*, May 2012, pp. 420–424.

[13] U. Scheuermann, "Reliability of planar SKiN interconnect technology," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Mar. 2012, pp. 1–8.

[14] T. Stockmeier, P. Beckedahl, C. Göbl, and T. Malzer, "SKiN: Double side sintering technology for new packages," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, May 2011, pp. 324–327.

[15] F. J. Wakeman and G. W. Lockwood, "Electromechanical evaluation of a bondless pressure contact IGBT," *IEE Proc.–Circuits, Devices Syst.*, vol. 148, no. 2, pp. 89–93, Apr. 2001.

[16] F. Wakeman, W. Findlay, and G. Li, "Press-pack IGBTs, semiconductor switches for pulse power," in *Pulsed Power Plasma Sci. (PPPS) Dig. Tech. Papers*, vol. 2. Jun. 2001, pp. 1051–1054.

[17] S. Eicher *et al.*, "4.5 kV press pack IGBT designed for ruggedness and reliability," in *Proc. 39th IAS Annu. Meeting. Conf. Rec. IEEE Ind. Appl. Conf.*, vol. 3. Oct. 2004, pp. 1534–1539.

[18] A. K. Solomon, A. Castellazzi, N. Delmonte, and P. Cova, "Highly integrated low-inductive power switches using double-etched substrates with through-hole viases," in *Proc. 27th Int. Symp. Power Semiconductor Devices IC's*, Hong Kong, May 2015, pp. 329–332.

[19] J. F. Li, A. Castellazzi, T. Dai, M. Corfield, A. K. Solomon, and C. M. Johnson, "Built-in reliability design of highly integrated solid-state power switches with metal bump interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2587–2600, May 2015.

[20] Z. Mei, "Microstructual evolution and interfacial interaction in lead-free solder interconnects," in *Lead-Free Solder Interconnect Rel*, D. Shangguan, Ed. Materials Park, OH, USA: ASM, 2005, pp. 29–66.

[21] A. Zéanh *et al.*, "Thermomechanical modelling and reliability study of an IGBT module for an aeronautical application," in *Proc. 9th Int. Conf. Thermal, Mech. Multiphys. Simulation Experim. Micro-Electron. Micro-Syst. (EuroSimE)*, Freiburg im Breisgau, Germany, Apr. 2008, pp. 1–7.

[22] A. Zéanh, O. Dalverny, M. Karama, and A. Bouzourene, "Lifetime and reliability assessment of AlN substrates used in harsh aeronautic environments power switch modules," *Adv. Mater. Res.*, vol. 112, pp. 113–127, May 2010.

[23] W. W. Sheng and R. P. Colino, *Power Electronic Modules: Design and Manufacture*. Boca Raton, FL, USA: CRC Press, 2005.

[24] Q. Zhang and A. Dasgupta, "Constitutive properties and durability of selected lead-free solders," in *Lead-Free Electronics*, S. Ganesan and M. Pecht, Eds. New York, NY, USA: Wiley, 2006, pp. 237–382.

[25] A. Syed, "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints," in *Proc. ECTC Conf.*, Las Vegas, NV, USA, Jun. 2004, pp. 737–746.

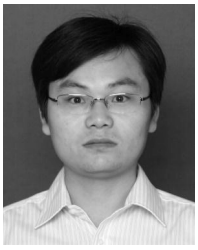
[26] C. Andersson, Z. Lai, J. Liu, H. Jiang, and Y. Yu, "Comparison of isothermal mechanical fatigue properties of lead-free solder joints and bulk solders," *Mater. Sci. Eng. A*, vol. 394, nos. 1–2, pp. 20–27, Mar. 2005.

[27] C. Xiangyang and Z. Dejian, "Modeling and reliability analysis of lead-free solder joints of bottom leaded plastic (BLP) package," in *Proc. Conf. High Density Microsyst. Design Packag. Compon. Failure Anal. (HDP)*, Shanghai, China, Jun. 2006, pp. 247–253.

[28] P. Zhou, B.-T. Hu, J.-M. Zhou, and Y. Yang, "Parameter fitting of constitutive model and FEM analysis of solder joint thermal cycle reliability for lead-free solder Sn-3.5Ag," *J. Central South Univ.*, vol. 16, no. 3, pp. 339–343, Jun. 2009.

[29] S. Kraft, A. Schletz, and M. Maerz, "Reliability of silver sintering on DBC and DBA substrates for power electronic applications," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, Mar. 2012, pp. 439–444.

[30] E. Arjmand, P. A. Agyakwa, M. R. Corfield, J. Li, and C. Johnson, "Predicting lifetime of thick Al wire bonds using signals obtained from ultrasonic generator," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 5, pp. 814–821, May 2016.



Hui Zhang received the B.E. degree from the Taiyuan University of Technology, Taiyuan, China, in 2004, and the Ph.D. degree in materials science from the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China, in 2010.

He has been with the Advanced Carbide Ceramics Group, Shanghai Institute of Ceramics, since 2010. His current research interests include ceramic substrate, ceramic cooler, ceramic/copper brazing, reliability of ceramic-based power electronic interconnects, and the fabrication and joining technologies of advanced ceramics including carbides, borides, and nitrides.

Jianfeng Li received the B.S. degree in mineralogy from Nanjing University, Nanjing, China, in 1991, and the M.S. and Ph.D. degrees in materials science from the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China, in 1996 and 1999, respectively.

He was with the University of Technology of Belfort, Monbeliard, France, and the University of Manchester, and King's College, London, U.K., until 2007, where he was involved in thermal spray, laser material processing, and high-temperature electronic packaging. He joined the Power Electronics, Machines, and Control Group, University of Nottingham, Nottingham, U.K., in 2008, where he is currently a Senior Research Fellow, and focusing on integration, packaging, thermal, electro-thermal and thermomechanical simulation, new packaging structure, manufacturing technologies, and reliability of high performance and low-cost power electronic modules.

Jingru Dai received the B.S. degree in material science and engineering from Shandong University, Jinan, China, and the M.S. degree in material science and engineering from the Beijing University of Aeronautics and Astronautics, Beijing, China. She is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, U.K.

Her current research interests include silver sintering technology for die attachments, reliability tests, and failure analysis.

Martin Corfield received the B.Sc. degree in engineering science from the University of Hull, Kingston upon Hull, U.K. in 1996, and the M.phil. and Ph.D. degrees in metallurgy and materials from the University of Birmingham, Birmingham, U.K., in 1998 and 2003, respectively.

He held research fellowship posts with the University of Birmingham and the University of Sheffield, Sheffield, U.K. He is currently a Research Fellow with the Department of Electrical and Electronic Engineering, the University of Nottingham, Nottingham, U.K.

Xuejian Liu received the B.S. degree from Henan University, Kaifeng, China, in 1993, and the M.S. degree in physical chemistry in Zhejiang University, Hangzhou, China, in 1996, and the Ph.D. degree in materials science from the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China, in 1999.

His current recent research interests include the nitride-based phosphor powder and fluorescent ceramics, and the fabrication and applications of nonoxide ceramics including SiC and Si_3N_4.

Yan Liu received the B.S. degree from the Harbin University of Science and Technology, Harbin, China, in 1996, and the M.S. degree from the Harbin Institute of Technology, Harbin, in 2001, and the Ph.D. degree in materials science from the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China, in 2009.

He has been with the Shanghai Institute of Ceramics, where he is involved in the advanced integration technology of SiC ceramics and ceramic matrix composites and the nickel-based connector of solid oxide fuel cell. He has authored or co-authored over 20 papers in peer reviewed specialist journals and conferences.

Zhengren Huang received the B.S. degree from Jilin University, Changchun, China, in 1987, and the M.S. and Ph.D. degrees in materials science from the Shanghai Institute of Ceramics, Chinese Academy of Sciences, Shanghai, China, in 1990 and 1999, respectively.

His current research interests include SiC carbide ceramics, 3-D printing of ceramics, ceramic matrix composites, surface modification of advanced ceramics, the low-stress integration of ceramics, and the nondestructive testing technology of ceramics, porous SiC ceramic membrane, and ultra-high temperature ceramics.

Christopher Mark Johnson (M'90) received the B.A. degree in engineering and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 1986 and 1991, respectively.

From 1990 to 1992, he was a Research Associate with the University of Cambridge. He was a Lecturer with the University of Newcastle, Newcastle upon Tyne, U.K. in 1992, where he was involved in the design, analysis, and characterization of power semiconductor devices, resonant power conversion, and instrumentation. From 1998 to 2001, he managed the U.K. national programme on Silicon Carbide Electronics and in 2000 he became Reader of Power Electronics with the University of Newcastle. In 2003, was a Rolls-Royce/RAEng Research Professor of power electronic systems with the University of Sheffield, University of Sheffield, U.K. In 2006, he was a Personal Chair with the University of Nottingham, Nottingham, U.K. where he leads research into power semiconductor devices, power device packaging, reliability, thermal management, power module technologies and power electronic applications.

Dr. Johnson is the Director of the U.K. Engineering and Physical Sciences Research Council Centre for Power Electronics, which combines the U.K.'s best academic talent to address the key research challenges underpinning power electronics.