JESTPE-2022-12-1352

Medium-Voltage Megawatt Power-Electronic-Based Grid Emulators: Testing Capability Requirements and Dynamics Challenges – A Review

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***Abstract*- Power-electronic-based grid emulators are emerging as a promising way to test the grid-code compliance of renewable energy resources. Yet, the ever-increasing power and voltage levels of device under test pose new requirements and challenges to power-electronic-based grid emulators. This paper first gives an overview of testing capability requirements based on the recent grid codes and standards, then discusses the resulted dynamic interactions and solutions for power-electronic-based grid emulators. Perspectives on the open issues and emerging trends of grid emulators are finally shared.**

***Index Terms*—Grid emulator, grid-code requirements, testing, dynamic interactions.**

I. Introduction

POWER-electronic-based grid emulators are increasingly used to test the grid-code compliance of renewable energy resources, energy storage systems, and power-to-x systems, etc. Over the past years, the power and voltage levels of these devices under test (DUTs) have been continuously increasing. For instance, beginning in 1980s with tens of kilowatts (kW) wind turbines (WTs), 16 megawatt (MW) WTs are deployed today in offshore wind power plants [1], [2], where the voltage level of collector systems increases up to 66 kV [3]. The rapid growth of renewable energy resources has driven the evolution of grid codes with more stringent requirements, e.g., DUTs may need to ride through the overvoltage up to 160% of the nominal grid voltage and 15 consecutive grid faults [4], [5]. These trends demand a scalable and versatile grid emulator, which not only can accommodate the increasing voltage and power levels of DUTs but is also able to test compliances of DUTs with the evolving grid-code requirements.

Fig. 1 shows a general diagram of power-electronic-based grid emulators, which is commonly built on a back-to-back power conversion system with an active-front end (AFE) and a controlled voltage generator (CVG) [3]. For scalability, AFE and CVG are generally composed by series/ parallel connected modular power converters, such as the cascaded or interleaved neutral point clamped (NPC) converter [6]-[10], the cascaded H-bridge (CHB) converter [11]-[13], and the modular multilevel converter (MMC) [14]-[17]. Those topologies typically employ several neutral-point (NP), cell or submodule (SM) capacitors as the energy buffer of the power conversion, where low-frequency fluctuations of capacitor voltages are actively regulated, introducing internal dynamics into grid emulators [13], [14], [18]. The internal dynamics can interact with the external dynamics of CVG when emulating transient events, causing voltage imbalance or even over-/under-voltage of the internal capacitors, which may, in turn, adversely affect the testing capabilities of CVG, such as the synthesis of harmonic voltages and the emulation of varying grid impedance during a fault ride-through (FRT) test [16].

Besides the dynamic interactions within CVG, the external control of CVG may also interact with the AFE through the dc link of grid emulators, and with the control dynamics of DUT, posing multifold challenges to the dynamics of grid emulators. In [12], [19], [20], it has been reported that an FRT test by CVG may result in the over-/ under-voltage at the common dc link, which can cause the overmodulation or even instability of CVG. In addition, the time delay involved in the digital control system can introduce a negative resistance into the output impedance of CVG and DUT, which may destabilize their interactions [3], [21].

This paper thus provides a review of testing capability requirements and dynamics challenges for power-electronic-based grid emulators. First, the testing capability requirements for a versatile grid emulator are formulated based on the latest updates of grid codes and standards. Following the testing capability requirements, a systematic discussion is then presented on dynamic interactions that may occur within the grid emulator, as well as between the grid emulator and DUT.

This work was supported by the Energy Technology Development and Demonstration Program (EUDP) for the project MERGE - Megawatt Scalable Versatile Grid Emulation System. (*Corresponding author: Xiongfei Wang*)

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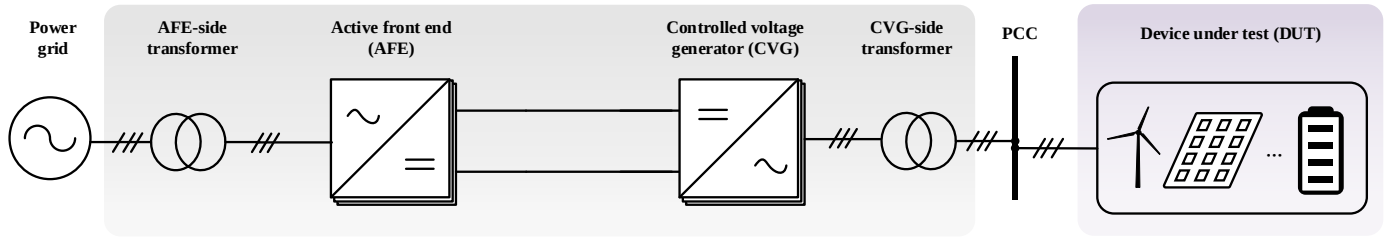

Fig. 1. General system diagram of power-electronic-based grid emulators.

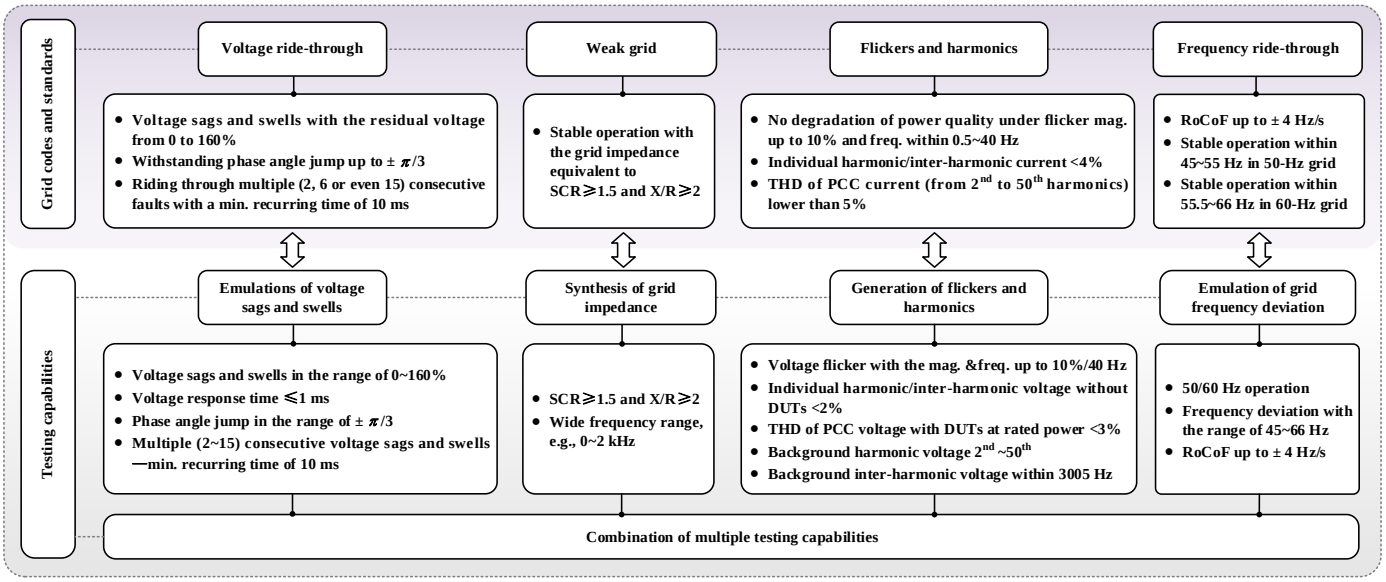

Fig. 2. Testing capability requirements of grid emulators, which are built on the latest updates of grid codes and standards.

The challenges posed by these dynamic interactions and the state-of-the-art solutions to address them are thoroughly examined. The open issues that require further research to overcome the dynamic challenges are then identified. Lastly, insights on the future prospects of testing capabilities for grid emulators are shared.

II. Testing Capability Requirements

This section discusses the testing capability requirements of grid emulators in five aspects, as illustrated in Fig. 2. All are built on the latest updates of grid codes and standards.

A. Emulations of Voltage Sags and Swells

1) Depth, duration time and response time: DUTs should ride through undervoltage and overvoltage faults following the recent requirements, e.g., IEC 61400-21 [22], IEEE 1547.1 [23], IEEE 2800 [24], FGW TR3 [25], DNV-GL TN066 [26] and national grid codes [4], [27]-[33]. Table I summarizes these low-voltage ride-through (LVRT) and high-voltage ride-through (HVRT) requirements with regards to the minimum time duration of DUTs operating under different residual voltages at the point of common coupling (PCC). It is important for a grid emulator to cover the full range of voltage sags/swells and operate continuously with DUTs within the required duration time.

Fig. 3 depicts the allowed tolerances on the root-mean-square (RMS) value of the positive sequence voltage at the PCC in an LVRT test [22]. This requirement is commonly followed by the existing grid emulators to generate voltage sags within the response time of t_{res}=20 ms. Similarly, the response time of reproducing voltage swells for HVRT tests is also within 20 ms [22]. Yet, to reproduce a real-world fault, a more stringent requirement on the response time of t_{res}=1 ms is imposed by DNV for grid emulators [6], [26].

TABLE I
LVRT and HVRT Requirements for DUTs

Types	Residual voltage (V_{pcc}/V_N)	Duration time [ms]
LVRT	<0.05	≥150
	0.20-0.30	≥625
	0.45-0.60	≥1371
	0.70-0.80	≥2389
	0.85-0.90	≥60000
HVRT	1.10-1.15	≥10000
	1.20-1.25	≥1000
	1.25-1.30	≥500
	1.30-1.60	≥50

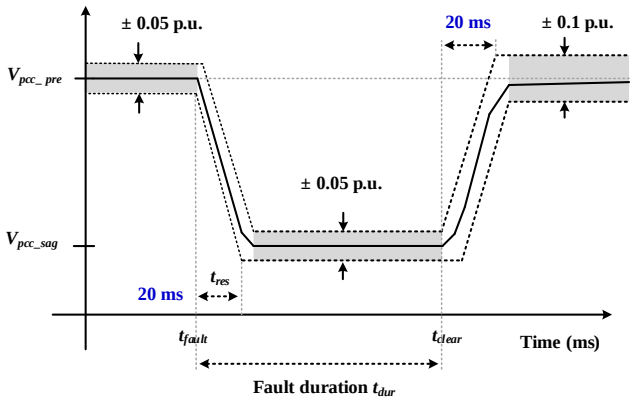

Fig. 3. The allowed tolerances on the RMS value of the positive sequence voltage for grid emulators in an LVRT test [22].

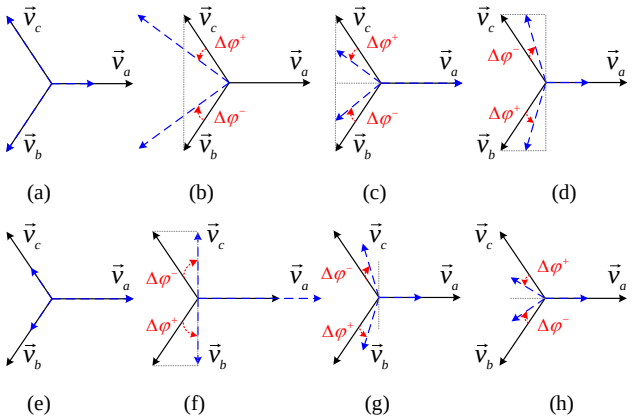

Fig. 4. Phasor diagrams of typical unbalanced voltage sags/swells [34]-[36]. (a) Single-phase-to-ground fault. (b) Single-phase-to-ground fault in the isolated neutral system. (c) Phase-to-phase fault. (d) Single-phase-to-ground fault after two Δ-Y transformers. (e) Two-phase-to-ground fault. (f) Two-phase-to-ground fault in the isolated neutral system. (g) Two-phase-to-ground fault after one Δ-Y transformer. (h) Two-phase-to-ground fault after two Δ-Y transformers.

2) Phase jump: Fig. 4 shows the phasor diagrams of eight typical unbalanced voltage sags/swells [34]-[36], where $\vec{v}_a$, $\vec{v}_b$ and $\vec{v}_c$ are three-phase voltage vectors. $\Delta\varphi^+$ and $\Delta\varphi^-$ represent the angles of phase jump. The phase jump often occurs in a phase-to-phase fault and during fault propagation of phase-to-ground faults. The maximum angle of phase jump in an unbalanced fault is $\pm\pi/3$. For the phase jump in balanced faults, DUTs must also be able to ride through a maximum angle of phase jump of $\pm\pi/3$ [5]. Therefore, a grid emulator should be able to reproduce the phase-jump angle in the range of $\pm\pi/3$.

3) Multiple consecutive voltage sags and swells: Table II lists typical multiple-fault ride-through (MFRT) requirements for DUTs [5], [29], [37]. In the Danish grid codes, DUTs must withstand at least two/six consecutive faults during 2-min/5-min intervals, with each fault lasting 100 ms and followed by a new fault after 300-500 ms [29]. Recently, a more stringent requirement is imposed by AEMO, i.e., DUTs must ride through 15 consecutive balanced and unbalanced faults, of which, the recurring time between the first 8 faults is as low as 10 ms [5], [37]. Thus, grid emulators should operate stably

TABLE II
MFRT REQUIREMENTS FOR DUTS

Grid codes	Numbers of faults		Duration of each fault [ms]	Recurring time [ms]
Danish	At least 2 times within 2 min		100	300-500
	At least 6 times within 5 min		100	300-500
AEMO	15 times within 1 min	8	120	2*10, 2*200 2*500, 750 1000
		6	220	1500, 2*2000, 3000, 5000, 7000
		1	430	10000

when reproducing 15 consecutive voltage sags and swells, even if the minimum interval between each fault is lower than 10 ms.

B. Synthesis of Grid Impedance

The power grid is generally emulated as a voltage source behind a grid impedance, which is either constant or frequency-dependent, composed by resistance, inductance or capacitance (*RLC*), or various combinations of *RLC* [10]. DUTs can interact with a weak (high-impedance) grid, causing harmonic instability issues [38]. Hence, grid operators specify several metrics to reflect the grid strength for assessing the stability of DUTs in weak grids [22], [24].

The short-circuit ratio (SCR) is a commonly used metric [24], which is defined as

$$\mathrm{SCR}=\frac{S_f}{P_{dN}}=\frac{V_g^2}{P_{dN}}\times\frac{1}{Z_g}=\frac{1}{Z_{g\_\mathrm{p.u.}}} \tag{1}$$

where S_f and P_{dN} represent the short-circuit power of grid and the active power rating of grid-connected devices. V_g and Z_g denote the ideal grid voltage and grid impedance. $Z_{gp.u.}$ is the per-unit (p.u.) value of grid impedance.

In addition, the X/R ratio is another critical parameter for the grid impedance. In the FGW TR3, DUTs are required to stably operate at a minimum SCR of 2 and an X/R ratio of at least 3 [7], [39]. Recently, a more stringent requirement has been introduced by AEMO, i.e., the minimum SCR and X/R ratio are reduced to 1.5 and 2, respectively [40].

Therefore, a grid emulator should be able to synthesize the grid impedance with SCR≥1.5 and X/R≥2. However, differing from synchronous generators, the short-circuit capacity of a power-electronic-based grid emulator is limited by the overloading capability of power semiconductor devices. As a result, the short-circuit capacity of grid emulator may not fully reflect the grid strength. Instead, the SCR=1/$Z_{gp.u.}$ is merely used to indicate the impedance synthesized by grid emulators in practice. For example, an "infinite" SCR, i.e., the ideally stiff grid, is realized in a 7 MVA grid emulator by setting $Z_{gp.u.}$=0 [6].

It is worth noting that a common practice is to use the SCR and the X/R ratio to define the impedance profile at the

fundamental frequency. However, to fully reproduce the grid-DUT interactions, the grid impedance emulation needs to cover a wide frequency range, e.g., 0~2 kHz [10], [41], due to the wide-timescale control dynamics of DUT.

C. Generation of Flickers and Harmonics

1) Voltage flickers: When low-frequency (i.e., 0.5 Hz~40 Hz) voltage fluctuations within 10% of normal voltage occur at the PCC, DUTs are required to maintain stable operation without deteriorating the power quality of the power grid [22], [42]. To assess the impact of such voltage flicker on DUTs, a typical voltage reference for a grid emulator is given by

$$V_{j\_ref} = \left[1 + A_m \sin\left(2\pi f_m t\right)\right] V_N \sin\left(2\pi f_1 t + \varphi_j\right) \tag{2}$$

where A_m and f_m are the magnitude of voltage fluctuation and flicker frequency, respectively. f_1 and φ_j are the fundamental frequency and initial phase angle. Generally, f_m ranges from 0.5 Hz to 40 Hz and A_m is lower than 10% [22], [42].

2) Total harmonic distortion (THD) with and without DUTs: The current harmonic emissions of DUTs should comply with grid-code requirements, which specify that the individual harmonic distortion and the THD (from 2nd to 50th harmonics) of PCC current must be lower than 4% and 5%, respectively [24]. In addition, the non-integer harmonic (inter-harmonic) current between hf_1±5 Hz should be also within 4%, where h is the individual harmonic order [24]. However, the switching operation of a power-electronic-based grid emulator may lead to additional current harmonics. Thus, IEEE 1547.1 requires that the individual harmonic and inter-harmonic voltage distortion of the grid emulator without DUTs must not exceed 2% [23]. Further, when a grid emulator is operating with DUTs in steady state at rated power, the THD of PCC voltage should be lower than 3% [23].

3) Background harmonic voltage: For on-site operation of a DUT, the THD of PCC current is influenced by dynamic interactions between the DUT and the power grid [24]. To reproduce this impact of background grid voltage harmonics on DUTs, a grid emulator should be able to synthesize the harmonic voltages covering 2nd~50th and inter-harmonic voltages up to 3005 Hz [22], [24]. The specific harmonic magnitudes are commonly provided by grid operators.

D. Emulation of Grid Frequency Deviation

Table III summarizes the typical requirements of operating frequency range and maximum rate of change of frequency (RoCoF) that DUTs shall not trip [4], [29]. To evaluate the active power responses of DUTs under the grid-frequency dynamics, a grid emulator needs to operate continuously at 45~66 Hz and generate a RoCoF up to ±4 Hz/s.

E. Combination of Multiple Testing Capabilities

In actual power grids, the simultaneous changes of voltage magnitude, impedance, frequency, phase angle and harmonics may occur. The combination of multiple testing capabilities is, therefore, important for a grid emulator.

A conventional solution is based on the shunt impedance as shown in Fig. 5(a) [22], where Z_g, Z_1 and Z_2 are the grid impedance, series impedance and fault impedance. Fig. 5(b) shows the time sequence of the voltage-magnitude changes and the impedance variation [7], [43], [44]. Hence, the MFRT

TABLE III
OPERATING FREQUENCY RANGE AND MAX ROCOF FOR DUTS

Fundamental frequency (Hz)	Operating frequency range (Hz)		Max RoCoF (Hz/s)
	Min	Max	
50	45	55	±4
60	55.5	66	±4

test can be realized by shunting multiple impedances [5]. The drawback of this method is the extensive energy loss as the power capacity of DUT increases. In contrast, a power-electronic-based grid emulator can reduce the loss with more controllability to follow the principle shown in Fig. 5(b).

For three-phase balanced fault emulation, the relationship between emulated impedance and residual voltage at the PCC is expressed as [5]

$$\frac{V_{pcc\_sag}}{V_g} = \frac{Z_2}{Z_g + Z_1 + Z_2} \tag{3}$$

where V_{pcc_sag} is the residual voltage at the PCC.

Further, the voltage-magnitude change and impedance variation are often accompanied by a phase jump in unbalanced faults [44]. In Fig. 5(a), the fault depth and phase jump are inherently dependent on the size and X/R ratio of Z_g, Z_1 and Z_2. For a power-electronic-based grid emulator, correct input references of voltage and impedance are critical to the emulation of unbalanced faults. Taking the phase-to-phase fault in Fig. 4 (c) as an example, the three-phase voltage vectors and angles of phase jump are given by [45]

$$\begin{cases} \vec{v}_a = V_g \\ \vec{v}_b = 0.5\left(-1 - j\sqrt{3}K_f\right)V_g \\ \vec{v}_c = 0.5\left(-1 + j\sqrt{3}K_f\right)V_g \end{cases} \tag{4}$$

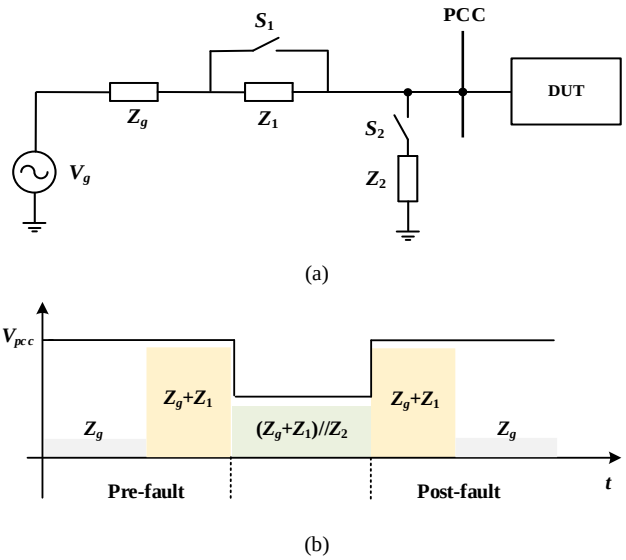

Fig. 5. Typical co-emulation of voltage sags with impedance variation. (a) Shunt-impedance-based grid emulator [22]. (b) Time sequence of impedance variation and voltage-magnitude changes [7].

$$\Delta\varphi^{+} = -\arctan\left(\sqrt{3}K_f\right) + \pi/3 \tag{5}$$

$$\Delta\varphi^{-} = \arctan\left(\sqrt{3}K_f\right) - \pi/3 \tag{6}$$

where K_f is the fault factor related to the depth of voltage sags.

Consequently, the input voltage-magnitude references for a grid emulator are derived as

$$\begin{cases} v_a(t) = V_g \cos\left(2\pi f_1 t\right) \\ v_b(t) = 0.5\sqrt{1+3K_f^2}V_g \cos\left[2\pi f_1 t + \arctan\left(\sqrt{3}K_f\right) - \pi\right] \\ v_c(t) = 0.5\sqrt{1+3K_f^2}V_g \cos\left[2\pi f_1 t - \arctan\left(\sqrt{3}K_f\right) + \pi\right] \end{cases} \tag{7}$$

Besides, according to the sequence decomposition theory [46], the relationship between the required input reference of fault impedance and fault factor is expressed as

$$Z_2 = \frac{K_f}{1-K_f}\left(Z_g + Z_1\right) \tag{8}$$

The combination of other testing capabilities, e.g., the emulation of impedance, frequency deviation and harmonics, is of important for next-generation versatile grid emulators.

III. Dynamic Interactions and Solutions

Fig. 6 illustrates four types of dynamic interactions that challenge the dynamic performance of grid emulators. This section first describes how the latest testing capabilities give rise to these dynamic interactions, and then thoroughly discusses state-of-the-art solutions to address them.

A. Interactions Within CVG Caused by Fault Current Injection of DUT

In FRT tests, the fault current injected by the type-4 WTs and the type-3 WTs can be up to 2 p.u. and 7 p.u., respectively [47]. The fault-current injection brings internal-external dynamic interactions in three typical grid emulators, i.e., the cascaded/interleaved NPC-, CHB- and MMC-based grid emulators. The emulated PCC voltage and fault current may result in distorted and different charging/ discharging currents of NP/cell/SM capacitors, causing their voltage fluctuations and imbalance. In turn, the ripple and imbalance of these internal capacitor voltages may further disturb ac output dynamics or even trip the CVG.

The impact of internal capacitor voltage fluctuations on the external output of CVG can be mitigated by feeding these capacitor voltages forward to the modulation link of CVG [12], [15], [16]. In respect to the voltage imbalance in the internal capacitors, the NPC-, CHB-based grid emulators differ from the MMC-based grid emulators.

1) Cascaded/ interleaved *NPC:* The commercial ACS6000 [6], [48], [49] or MV7000 [8], [50] converters are generally employed in NPC-based grid emulators. The NP capacitors in these converters are often paralleled with resistors to balance capacitor voltages. Further, the vector regulation and injecting zero-sequence voltage in modulation are common practices in NPC converters to mitigate voltage imbalance in the NP capacitors [18]. Fig. 7 shows a commercial grid emulator [49], where both the AFE and CVG share a single NP, enhancing the control flexibility of NP capacitor voltages [51]. Hence, the problems driven by voltage imbalance of NP capacitors have not been previously reported in commercial NPC-based grid emulators [6]-[10], [48]-[50].

2) CHB: Fig. 8 shows a commercial CHB-based grid emulator, which is composed by an input multi-winding transformer, nine H-bridge cells, ac filters and an output transformer [12]. Each cell is supported by an individual three-phase AFE converter, utilizing the same dc-link voltage control. Thus, each AFE converter can be equivalent as a dc voltage source, which can suppress the common-mode current

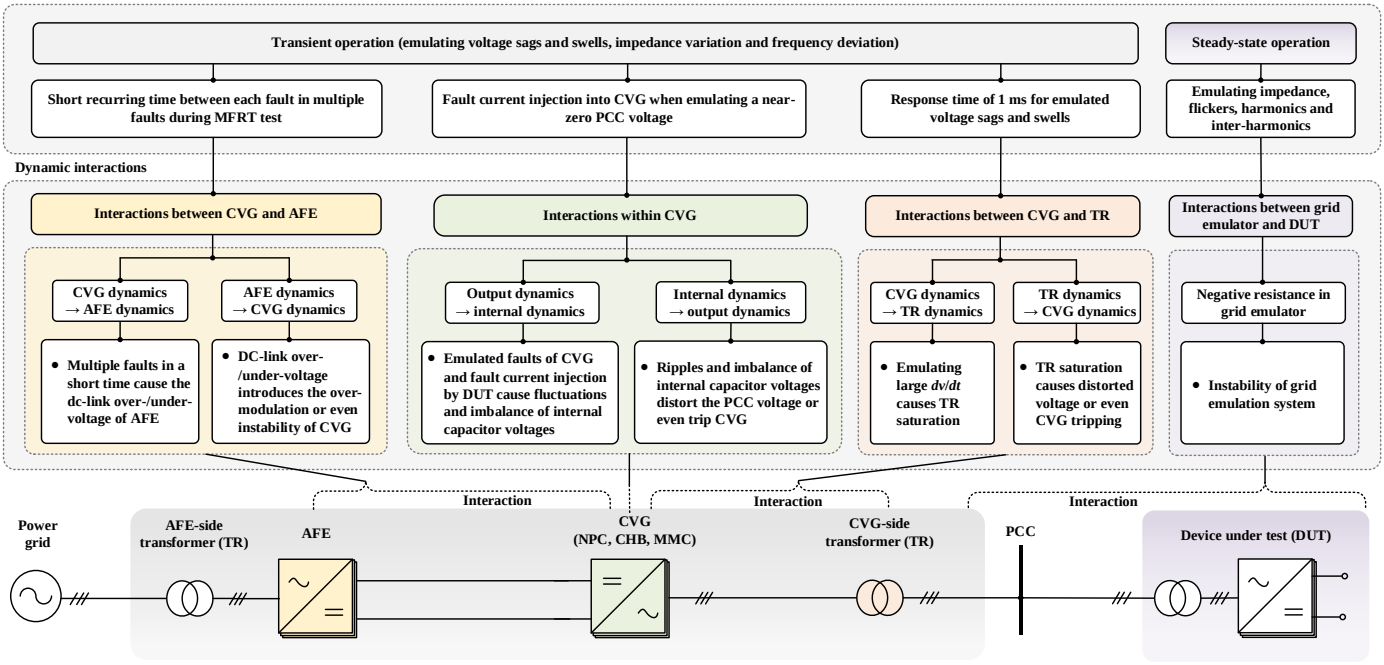

Fig. 6. Dynamic interactions for a scalable and versatile power-electronic-based grid emulator.

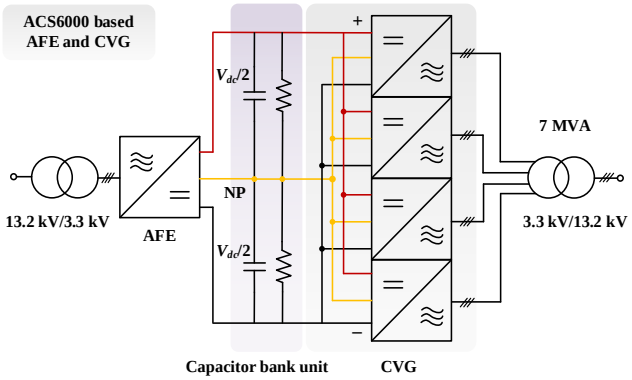

Fig. 7. A commercial NPC-based grid emulator [49].

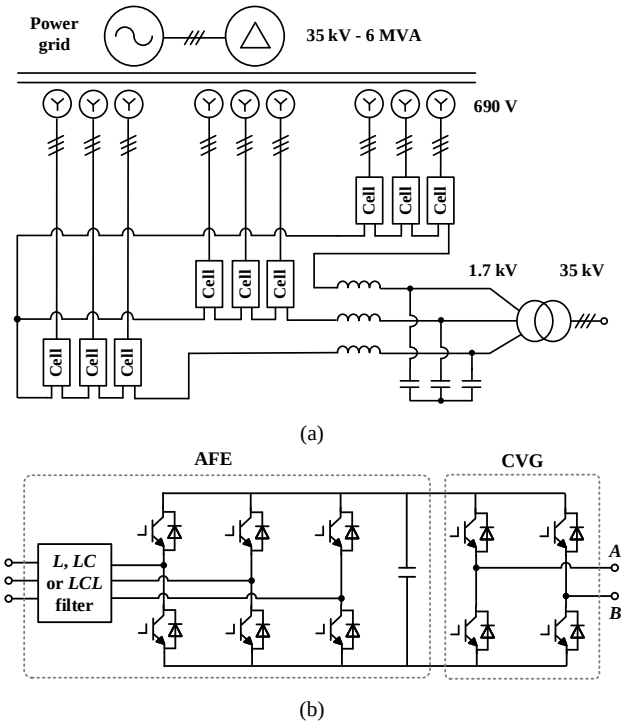

Fig. 8. A commercial CHB-based grid emulator [12]. (a) General structure. (b) Cell topology.

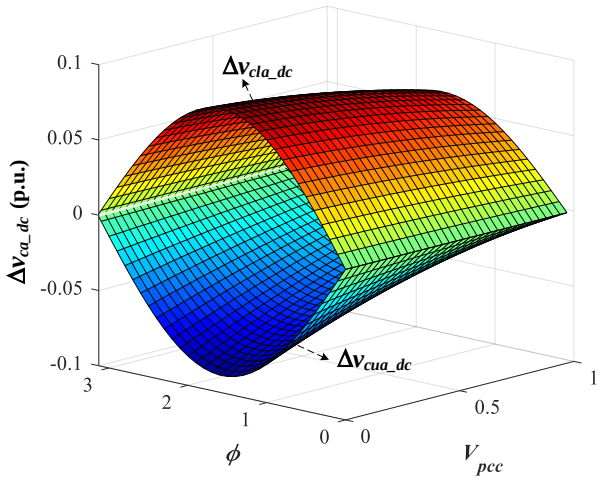

Fig. 9. Relationship among dc component variations of SM capacitor voltages, PCC voltage V_{pcc} and power factor angle φ [17].

sharing between the H-bridge arms [51], [52]. Therefore, the voltage imbalance issues in cell capacitors can be addressed in CHB-based grid emulators [11]-[13], [53].

3) MMC: The MMC is emerging as a promising topology for the medium-voltage MW grid emulator, thanks to its modularity and scalability. The MMC-based grid emulator typically employs 5~20 floating SMs per arm to achieve a 3.3 kV~13.8 kV output at the inverter side [17], [54]. In [17], an average model of the floating SM capacitor voltages during the LVRT test has been established. The SM capacitor voltages of upper arm and lower arm in phase-a are expressed as [17]

$$\begin{aligned} v_{cua} &= V_c + \frac{1}{C_{sm}}\int_{t_0}^{t} n_{ua} i_{ua}\, dt \\ &= V_c + \frac{V_{dc}}{2NV_c\omega_1 C_{sm}}\left[\begin{array}{l} \frac{I_o}{2}\sin(\omega_1 t-\varphi) - \frac{m^2 I_o \cos\varphi}{4}\sin(\omega_1 t) \\ -\frac{mI_o}{8}\sin(2\omega_1 t-\varphi) \end{array}\right]_{t_0}^{t} \\ &= V_c + \underbrace{f_{cua}(t)}_{\Delta v_{cua\_ac}} \underbrace{-f_{cua}(t_0)}_{\Delta v_{cua\_dc}} \end{aligned} \quad (9)$$

$$\begin{aligned} v_{cla} &= V_c + \frac{1}{C_{sm}}\int_{t_0}^{t} n_{la} i_{la}\, dt \\ &= V_c + \frac{V_{dc}}{2NV_c\omega_1 C_{sm}}\left[\begin{array}{l} -\frac{I_o}{2}\sin(\omega_1 t-\varphi) + \frac{m^2 I_o \cos\varphi}{4}\sin(\omega_1 t) \\ -\frac{mI_o}{8}\sin(2\omega_1 t-\varphi) \end{array}\right]_{t_0}^{t} \\ &= V_c + \underbrace{f_{cla}(t)}_{\Delta v_{cla\_ac}} \underbrace{-f_{cla}(t_0)}_{\Delta v_{cla\_dc}} \end{aligned} \quad (10)$$

where n_{ua}/n_{la} and i_{ua}/i_{la} are the insertion index of SMs and arm current in upper and lower arms, respectively. V_c and C_{sm} denote the rated voltage and capacitance of SM capacitors. N and V_{dc} represent the number of SMs per arm and the dc-link voltage. m is the modulation index, which is dependent on the emulated V_{pcc}. I_o and φ are the PCC current and power factor angle. t_0 is the instant of maximum transient fault current. $\Delta v_{cua\_ac}/\Delta v_{cla\_ac}$ and $\Delta v_{cua\_dc}/\Delta v_{cla\_dc}$ denote the ac fluctuation and the dc component variation of SM capacitor voltages, respectively.

Fig. 9 shows the relationship among $\Delta v_{cua\_dc}/\Delta v_{cla\_dc}$, V_{pcc} and φ [17]. The sign of Δv_{cua_dc} and Δv_{cla_dc} is converse, which means the voltage imbalance of SM capacitors between the upper and lower arms. Further, the difference between Δv_{cua_dc} and Δv_{cla_dc} becomes larger as the emulated V_{pcc} decreases, causing over-/under-voltage of SM capacitors or even tripping the grid emulator.

To handle the imbalance and fluctuation of SM capacitor voltages on the output dynamics of MMC-based CVG, the closed-loop modulation is a practical solution, i.e., the controlled arm voltage divided by the sum of SM capacitor voltage per arm [55]. Yet, the energy-based phase and arm balancing control have to be employed to ensure system stability, as shown in Fig. 10 [14]. The phase balancing control is used to produce the dc component of the circulating current to regulate the average SM capacitor voltage. By multiplying the external control output v_{ex}^{*}, the arm balancing

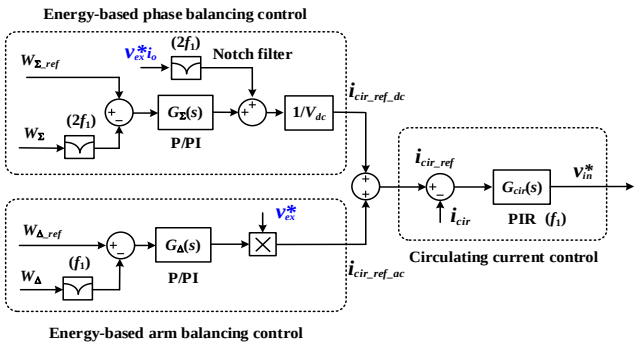

Fig. 10. Energy-based internal control scheme for MMC-based CVG [14].

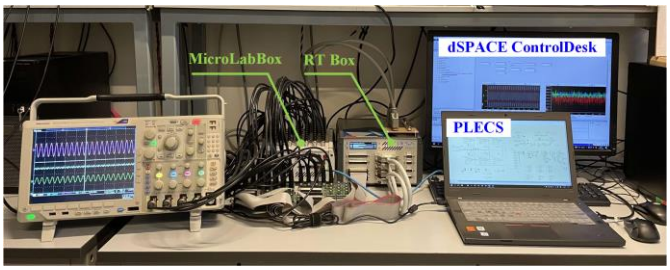

Fig. 11. CHIL-based experimental setup.

Table IV
PARAMETERS OF THE MMC-BASED GRID EMULATOR

Symbol	Meaning	Realistic value	CHIL value
V_{pccll}	PCC voltage (l-l, rms)	11 kV (1 p.u.)	11 kV (1 p.u.)
V_{dc}	DC-link voltage	12 kV	12 kV
P_o	Rated power of DUT	4 MVA (1 p.u.)	4 MVA (1 p.u.)
L_{arm}	Arm inductance	9.8 mH (0.1 p.u.)	9.8 mH (0.1 p.u.)
N	SM number per arm	16	4
C_{sm}	SM capacitance	4 mF	1 mF
C_{eq}	Equivalent capacitance of each arm C_{sm}/N	0.25 mF	0.25 mF
f_{sa}	Sampling frequency	10 kHz	10 kHz
f_c	Carrier frequency	500 Hz	2 kHz
f_{sw}	Equivalent switching frequency $2Nf_c$	16 kHz	16 kHz
α_v	Bandwidth of ac voltage control	3000π rad/s	3000π rad/s
α_Σ	Bandwidth of phase balancing control	80π rad/s	80π rad/s
α_Δ	Bandwidth of arm balancing control	40π rad/s	40π rad/s
α_{cir_dc}	Bandwidth of i_{cir_dc} control	600π rad/s	600π rad/s
α_{cir_ac}	Bandwidth of i_{cir_ac} control	100π rad/s	100π rad/s

control can generate a fundamental-frequency circulating current to balance the SM capacitor voltages between the upper and lower arms [14], [15]. In this case, the insertion index and arm currents can be expressed as

$$n_{ua} \approx \frac{V_{dc}}{2NV_c}\left[1-m\cos(\omega_1 t)\right] \tag{11}$$

$$n_{la} \approx \frac{V_{dc}}{2NV_c}\left[1+m\cos(\omega_1 t)\right] \tag{12}$$

$$i_{ua} = I_{cir\_dc} + \frac{1}{2}I_o\cos(\omega_1 t+\varphi) + I_{cir\_ac}\cos(\omega_1 t+\varphi_c) \tag{13}$$

$$i_{la} = I_{cir\_dc} - \frac{1}{2}I_o\cos(\omega_1 t+\varphi) + I_{cir\_ac}\cos(\omega_1 t+\varphi_c) \tag{14}$$

where I_{cir_ac} and φ_c are the magnitude and phase angle of injected fundamental-frequency circulating current. I_{cir_dc} is the dc component of circulating current.

The charging and discharging current of SM capacitors in the upper and lower arms are given by

$$n_{ua}i_{ua} = \frac{V_{dc}}{2NV_c}\begin{bmatrix} I_{cir\_dc} - \dfrac{mI_o}{4}\cos(\varphi) - \dfrac{mI_{cir\_ac}}{2}\cos(\varphi_c) \\ +\dfrac{1}{2}I_o\cos(\omega_1 t+\varphi) + I_{cir\_ac}\cos(\omega_1 t+\varphi_c) \\ -mI_{cir\_dc}\cos(\omega_1 t) - \dfrac{mI_o}{4}\cos(2\omega_1 t+\varphi) \\ -\dfrac{mI_{cir\_ac}}{2}\cos(2\omega_1 t+\varphi_c) \end{bmatrix} \tag{15}$$

$$n_{la}i_{la} = \frac{V_{dc}}{2NV_c}\begin{bmatrix} I_{cir\_dc} - \dfrac{mI_o}{4}\cos(\varphi) + \dfrac{mI_{cir\_ac}}{2}\cos(\varphi_c) \\ -\dfrac{1}{2}I_o\cos(\omega_1 t+\varphi) + I_{cir\_ac}\cos(\omega_1 t+\varphi_c) \\ +mI_{cir\_dc}\cos(\omega_1 t) - \dfrac{mI_o}{4}\cos(2\omega_1 t+\varphi) \\ +\dfrac{mI_{cir\_ac}}{2}\cos(2\omega_1 t+\varphi_c) \end{bmatrix} \tag{16}$$

Thus, the injected ac circulating current exhibits opposite dc charging/discharging currents to balance the SM capacitor voltages of the upper and lower arms. According to Fig. 10, injected I_{cir_ac} becomes to zero once the SM capacitor voltages are balanced. However, the balancing effect is weaker as the emulated voltage, i.e., m and v_{ex}^*, decreases.

Fig. 11 depicts a controller-hardware-in-the-loop (CHIL)-based experimental setup and Table IV shows an example of parameters for both realistic and simulated MMC-based grid emulators [17]. The control system of MMC is distributed in the MicroLabBox, while the power circuit of MMC with 4 full-bridge submodules per arm and a grid-following DUT system are arranged in the RT Box.

Fig. 12 shows experimental results of an MMC-based grid emulator during LVRT tests [17]. V_{cu_av} and V_{cl_av} are the average SM capacitor voltages of the single-phase upper and lower arms. i_o is the output current of the DUT. It is clear that the transient fault current injected by DUT causes the voltage imbalance of SM capacitors. The balancing effect of SM capacitor voltages between upper and lower arms becomes weaker as the emulated PCC voltage decreases. Addressing this issue requires a deliberate tuning of parameters for the

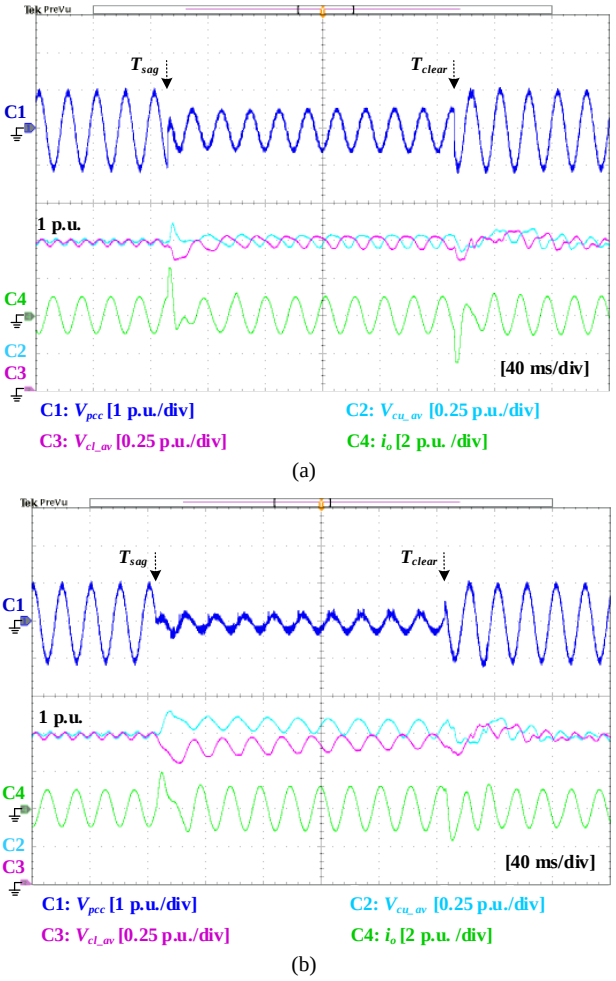

Fig. 12. The CHIL experimental results of an MMC-based grid emulator during LVRT tests. (a) V_{pcc}=0.5 p.u. during fault. (b) V_{pcc}=0.2 p.u. during fault.

arm balancing control or the injection of the fundamental-frequency circulating current [55].

B. Interactions Between CVG and AFE During MFRT Test

In FRT tests, the DUT should inject reactive current within 20 ms to support the PCC voltage, while the active current delivered to the grid emulator is immediately reduced [29]. Consequently, the dc current flowing into the AFE drops correspondingly, causing an overvoltage of the dc link due to the inability of power to suddenly change, at the instant of the emulated fault [13], [20]. Similarly, the dc-link voltage of AFE generally shows undervoltage after clearing the emulated fault. An over-/under-voltage at the dc link may cause overmodulation of the CVG, leading to the voltage distortion at the PCC or even instability [56].

To mitigate the over-/under-voltage, the dc-link voltage control and ac current control are commonly adopted in AFE [12], [13], [53]. Due to the limitation of the AFE control bandwidth, the settling time of dc-link voltage in grid emulators generally ranges from 20 ms to hundreds of milliseconds [13], [53]. By increasing the control bandwidth of AFE control for a settling time of 20~100 ms, it is possible to reproduce 6 consecutive faults, due to the fact that the time duration of a single fault is larger than 100 ms and the recurring time of each fault is greater than 300 ms [29].

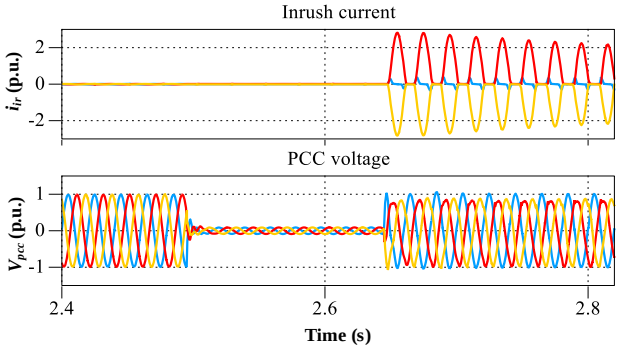

Fig. 13. An LVRT test considering saturation of CVG-side transformer.

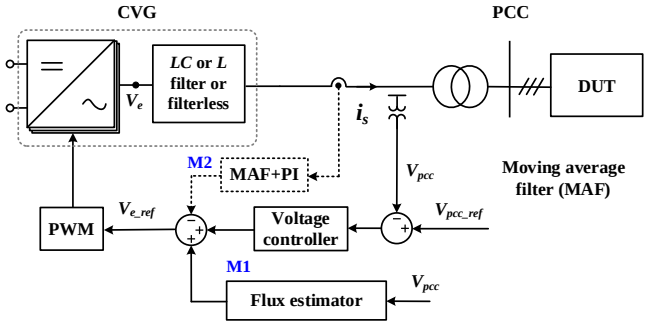

Fig. 14. Anti-saturation control configuration of transformer.

C. Interactions Between CVG and CVG-Side Transformer When Emulating Large dv/dt

To achieve a response time of voltage sag/swell less than 1 ms, the grid emulator should ensure that the slew rate (SR) of PCC voltage, i.e., *dv/dt*, can be up to 20 p.u./cycle (e.g., for a 50 Hz system) [6]. This high SR gives rise to the CVG-side transformer saturation due to the dc offset of magnetic flux [20], [57].

Fig. 13 demonstrates an LVRT test considering the core saturation of the CVG-side transformer. The magnetizing current of transformer, i.e., the inrush current, can be much higher than the nominal value, distorting the output voltage of CVG or even tripping the system.

Fig. 14 illustrates two anti-saturation control methods for grid emulators. They are 1) adding the flux estimator to inject the dc voltage component to counteract the dc offset [6], [48], [58], and 2) using a current feedforward control, e.g., based on a moving average filter with a proportional-integral (PI) controller, to eliminate the dc component of the transformer excitation current [59]. Although effective, the nonlinear dynamics of transformer and overlarge *dv/dt* during transient events complicate the design of these anti-saturation controls.

D. Interactions Between Grid Emulator and DUT Under Steady-State Operation

For steady-state emulation of voltage magnitude, impedance, flickers, harmonics and inter-harmonics, the time delay in the digital control system can introduce a negative resistance (-*R*) of output impedance for a grid emulator [60], [61]. The -*R* may interact with the control system of DUT, causing harmonic instability problems [16], [38], [61].

To regulate the voltage magnitude at PCC, a single-loop voltage-controlled inverter based on a fundamental-frequency resonant controller is adopted in [60], [61], where the sign of real part of output impedance Z_o is expressed as

$$\mathrm{sgn}\{\mathrm{Re}\{Z_o(j\omega)\}\} \approx \mathrm{sgn}\{-L_s K_{r1}\cos(\omega T_d)\} \tag{17}$$

where sgn $\{\cdot\}$ represents the sign function. L_s is the inductance of L filter. T_d and K_{r1} are the time delay and resonant gain. It implies a negative-resistance frequency region within $1/(4T_d)$. To address this issue, the dual-loop voltage control is usually used, where the sign of real part of output impedance is simplified as [60], [62]

$$\mathrm{sgn}\{\mathrm{Re}\{Z_o(j\omega)\}\} \approx \mathrm{sgn}\{K_{pc}(1-K_{r1}L_s)\cos(\omega T_d)\} \tag{18}$$

where K_{pc} is the proportional gain of inner current control. Since $K_{r1}L_s$ needs to be lower than 1 for internal stability [60], the $-R$ appears in $[1/(4T_d), f_s/2]$, where $f_s/2$ is the Nyquist frequency. Thus, the inner current control can counteract the $-R$ within $1/(4T_d)$.

Similarly, the virtual impedance (VI) and single-loop voltage control (VC) are used for synthesizing impedance [43], [63], which can also provide damping to mitigate the $-R$ within $1/(4T_d)$. However, as emulated impedance increases, $-R$ within $[1/(4T_d), f_s/2]$ becomes larger, which exacerbates the risk of high-frequency instability [64].

Regarding the emulation of voltage flickers, the reference in (2) can be expanded as [12]

$$\begin{aligned} V_{j\_ref} = {} & V_N \sin\left(2\pi f_1 t+\varphi_j\right)+0.5V_N A_m \cos\left[2\pi\left(f_1-f_m\right)t+\varphi_j\right]- \\ & 0.5V_N A_m \cos\left[2\pi\left(f_1+f_m\right)t+\varphi_j\right] \end{aligned} \tag{19}$$

Thus, a grid emulator must have accurate voltage control at the fundamental frequency (f_1) and two inter-harmonics (f_1-f_m and f_1+f_m) [12]. To emulate harmonics and inter-harmonics, resonant controllers are usually used with grid emulators [15], [65], [66]. Yet, the phase response of a resonant controller steps from $\pi/2$ to $-\pi/2$ at the harmonic frequency [67]. Consequently, the phase angle of output impedance at the harmonic frequency will shift π radians [61]. Considering the extra phase lag caused by T_d, $-R$ is usually introduced around the harmonic frequency [61], [68].

To handle these control interactions posed by the $-R$, the impedance-passivity-based design method is an effective solution [69]. The general idea is to shape the output impedance with a non-negative real part, such that the control of a grid emulator does not destabilize system.

Several efforts have been made on the impedance passivity-based design of a single-loop voltage-controlled inverter, the active damping (AD) control based on the feedforward of output current is a simple solution. Yet, its effect relies on the ac filters. For instance, in the LC-filtered inverter, the passive region of output impedance can be extended to $f_s/2$ [60]. Conversely, for the L-filtered inverter, the $-R$ within $[1/(4T_d), f_s/2]$ is not mitigated [61]. Additionally, the $-R$ also appears within $[1/(4T_d), f_s/2]$ for the voltage-magnitude emulation by the dual-loop voltage control [60] and the impedance emulation [63]. Thus, reducing time delay is a direct method to mitigate $-R$.

Fig. 15 shows the time-delay distribution of typical grid emulators, where two control structures are used, i.e., the centralized control and the distributed control [12], [49], [53], [54]. T_{sa} and T_{com} are the sampling period and communication

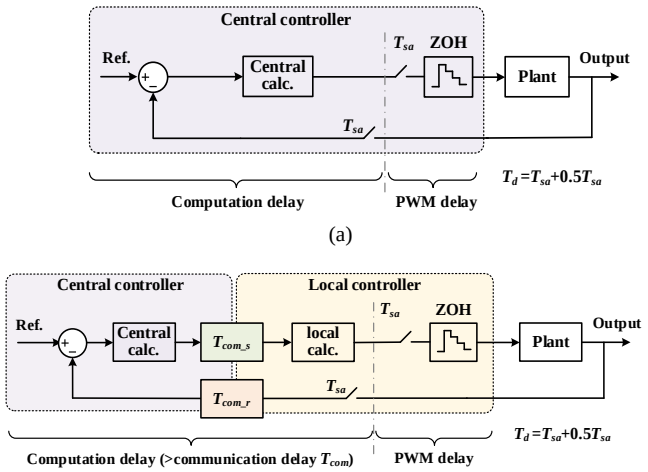

Fig. 15. Time-delay distribution of typical grid emulators [12], [49], [53], [54]. (a) Time delay in the centralized control structure. (b) Time delay in the distributed control structure.

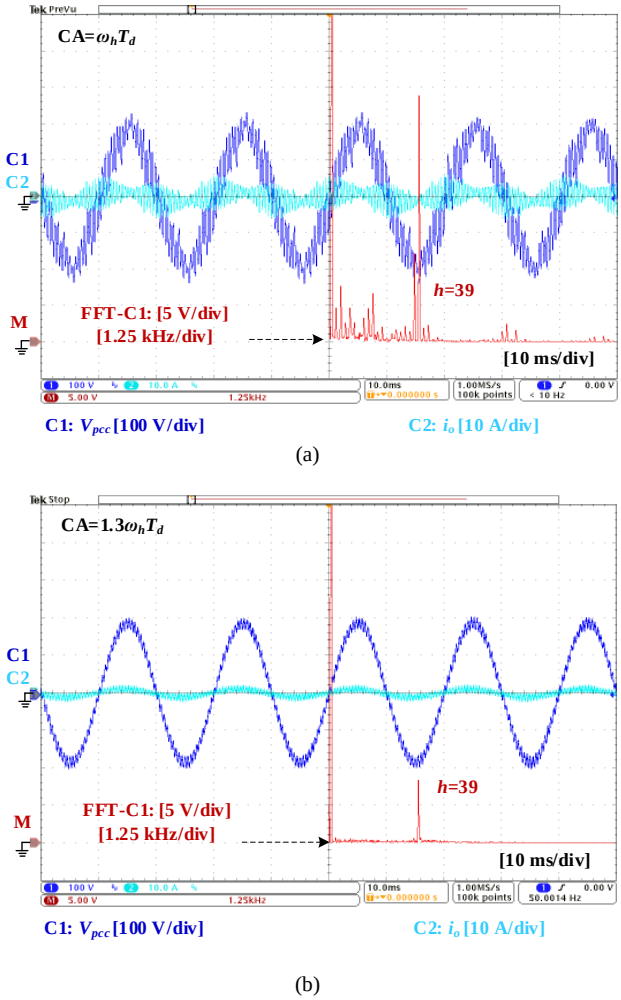

Fig. 16. Down-scaled experimental results of harmonic voltage emulation based on the resonant controller with different design of CAs. (a) Conventional design of CA. (b) Designed CA in [61].

delay [70]. The time delay consists of the computation delay (T_{sa}) and the pulse width modulation (PWM) delay ($0.5T_{sa}$) [71]. The difference of time delay in two control structures lies in different sampling periods. To reduce the time delay, increasing the sampling frequency is a simple way [72], [73]. Yet, it is limited by the computation of control algorithms and the communication delay. As a consequence, methods for compensating time delay are inevitable [74].

However, the time delay cannot be eliminated, which still introduces -R at certain harmonic frequencies when grid emulators perform the harmonic emulation based on resonant controllers [69]. To address this issue, the harmonic resonant controllers with phase-lead compensation angles (CAs) are commonly used [61], [68], [75]. However, the conventional design of CAs ($\omega_h T_d$) are not always effective to ensure the impedance passivity around harmonic frequencies, especially when the AD control is used. Fig. 16 presents experimental results of the harmonic voltage emulation based on resonant controllers with different design of CAs [61]. A conventional design of CA cannot guarantee system stability when passive loads are connected to the grid emulator. In [61], the alternative CAs for each resonator are selected based on the theory of linear fitting, which can achieve passive harmonic impedance till the critical frequency $1/(4T_d)$.

IV. Open Issues and Emerging Trends

Following the review of state-of-the-art solutions, four open issues that require further research to address the challenges with dynamic interactions are discussed in this section. Then, perspectives on two emerging trends, i.e., the reproduction of low-frequency oscillations during FRT tests and the co-emulation of multiple testing capabilities, are further shared.

A. Open Issues

1) Balancing SM capacitor voltages of MMC-based grid emulators when emulating a zero voltage: Fig. 17 shows a CHIL experimental result for the MMC-based grid emulator during the zero-voltage ride-through test [17]. According to (15) and (16), injecting circulating current cannot introduce dc charging/ discharging current for SM capacitor voltages when emulating a zero voltage, i.e., m=0. The effective methods for balancing SM capacitor voltages are still missing.

2) Mitigation of dc-link over-/under-voltage during the emulation of 15 consecutive faults: In 15 consecutive faults, the recurring time in the first 8 faults is 10 ms, lower than the settling time for the dc-link voltage regulated by AFE, which trends to cause consecutive over-/under-voltage in the dc link [37], [40].

Enabling a dc-link chopper is a simple solution to prevent the dc-link overvoltage. Fig. 18(a) shows a commercial chopper based on an integrated gate commutated thyristor (IGCT) and resistors, which is generally used in NPC-based grid emulators [49]. Fig. 18(b) shows a modular chopper composed of series-connected SMs, a resistor and an inductor, which may be used in the MMC-based grid emulator [76]. Yet, installing a chopper in each cell of a CHB-based grid emulator is infeasible from the perspective of volume and footprint.

Increasing dc-link capacitance is a practical, albeit costly, solution to mitigate both overvoltage and undervoltage. Yet,

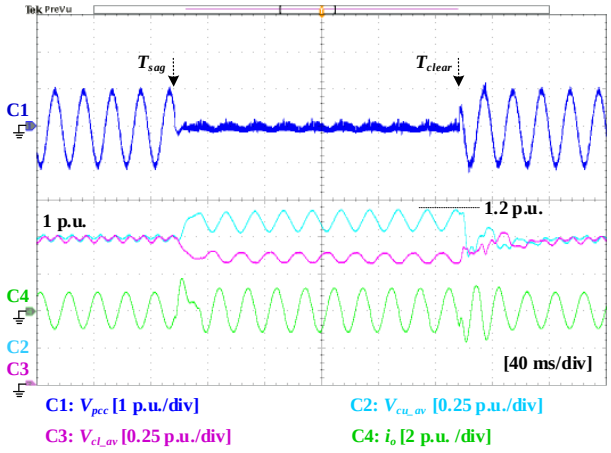

Fig. 17. The CHIL experimental result of the MMC-based grid emulator when emulating a zero voltage [17].

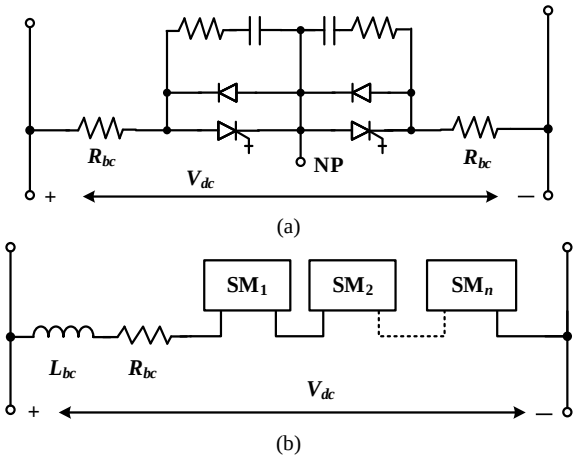

Fig. 18. DC-link choppers. (a) Commercial chopper for cascaded NPC-based grid emulators [49]. (b) Modular chopper for MMC-based grid emulators [76].

for the NPC- and CHB-based grid emulators, how to quantify dc-link capacitance to avoid undesired overdesign remains unclear.

In addition, there are no common dc-link capacitors in the MMC-based grid emulator [17], [54] and its equivalent dc-link capacitance C_{eq_dc} is proportional to the SM capacitance divided by the number of SMs per arm [77]. Generally, dozens of SMs are typically employed to increase the number of output voltage levels for achieving low THD at the PCC [76], but it comes at the cost of a significant reduction in C_{eq_dc}. To increase C_{eq_dc}, larger capacitances of SMs may be required, which can dramatically increase the cost, footprint and volume of the grid emulator.

3) Anti-saturation of CVG-side transformer: Fig. 19 depicts the PCC voltage of CVG after using the anti-saturation control that is based on a current feedforward control. Limited by the bandwidth of anti-saturation control and the emulated high SR, the magnetic flux deviation is usually reduced within 40 ms to mitigate the transformer saturation [6], [48]. Yet, this causes the response time of voltage sag longer than the required 1 ms. There is, thus, a tradeoff between the speed of desaturating transformer-core and the required response time of voltage during the FRT test.

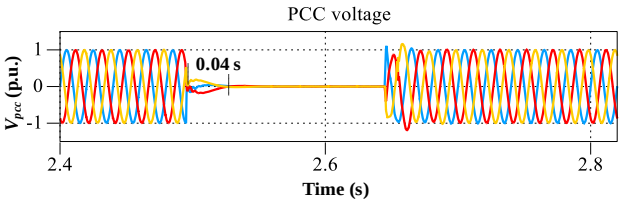

Fig. 19. PCC voltage of CVG after using the anti-saturation control based on a current feedforward control.

4) Mitigation of negative resistance when emulating multi-harmonics: The multi-resonant controller is often employed to synthesize multiple voltage harmonics [15], [65], [66]. It is shown in [67] that the lower-order resonant controller can introduce an additional phase lag to adjacent higher-order resonant controller. To address this issue, using a small and identical resonant gain for multi-harmonic resonant controller is a simple solution, yet it weakens the transient dynamics of harmonic voltage control [78]. Thus, a recursive design approach of resonant gains based on the gain margin of open-loop gain is reported in [67]. Unfortunately, the *-R* may still appear around the harmonic frequencies [68]. A co-design the resonant gains and CAs of the multi-resonant controller is needed to prevent the *-R*.

B. Emerging Trends

1) Reproduction of low-frequency oscillations during FRT tests: In actual grid faults, the transient overvoltage and low-frequency (<100 Hz) oscillations often occur at the PCC, especially for the grid with a low SCR at the post-fault process [64]. To reproduce these phenomena, it is important for a grid emulator to guarantee the accuracy of synthesized low-frequency impedance with low SCR.

However, a grid emulator based on conventional VC and VI control commonly exhibits the inaccuracy of low-frequency impedance emulation [10], [63], [64]. Fig. 20 shows the control diagram and simulation results of a grid emulator with an *L* filter [64]. $Z_{op}(s)$ and $Z_v(s)$ represent the open-loop impedance and VI. $G_v(s)$ and $H(s)$ denote the VC based on a proportional-resonant (PR) controller and a low-pass filter (LPF). The open-loop gain of the VC loop is

$$G_{opvc}(s)=\left(K_{pv}+\frac{K_{rv}s}{s^2+\omega_1^2}\right)e^{-sT_d} \tag{20}$$

where K_{pv} and K_{rv} are the proportional gain and resonant gain of voltage controller.

To guarantee the internal stability of system, the gain margin (GM) and phase margin (PM) of $G_{opvc}(s)$ should be larger than zero. Thus, K_{pv} and K_{rv} should satisfy

$$\begin{cases}\mathrm{GM}\approx -20\lg\left[\sqrt{\left(K_{pv}\right)^2+\left(\dfrac{K_{rv}}{2\pi f_{cv}}\right)^2}\right]>0\\ \mathrm{PM}\approx \pi-\arctan\left(\dfrac{K_{rv}}{2\pi K_{pv}f_{cv}}\right)-2\pi f_{cv}T_d>0\end{cases}\Rightarrow\begin{cases}K_{pv}<1\\ K_{rv}<\dfrac{\pi}{2T_d}\end{cases} \tag{21}$$

The output impedance of system is expressed as

$$Z_{GE}(s)=Z_{op}(s)+\frac{G_{opvc}(s)}{1+G_{opvc}(s)}\left[Z_v(s)H(s)-Z_{op}(s)\right] \tag{22}$$

At the low-frequency range, the time delay $G_d(s)$ is close to 1 and $G_v(s)$ approaches to K_{pv}. In (21), since K_{pv}<1, system closed-loop gain $G_{opvc}(s)/[1+G_{opvc}(s)]$ is less than 1, which results in $Z_{GE}(s)\neq Z_v(s)$. The error of emulating impedance increases as the SCR decreases. Fig. 20 (b) and Fig. 20 (c) illustrate two LVRT tests with post-fault SCR=3 and SCR=2, respectively. Compared to the shunt-impedance-based LVRT test, the low-frequency oscillations under a lower SCR cannot be fully reproduced by the converter-based grid emulators.

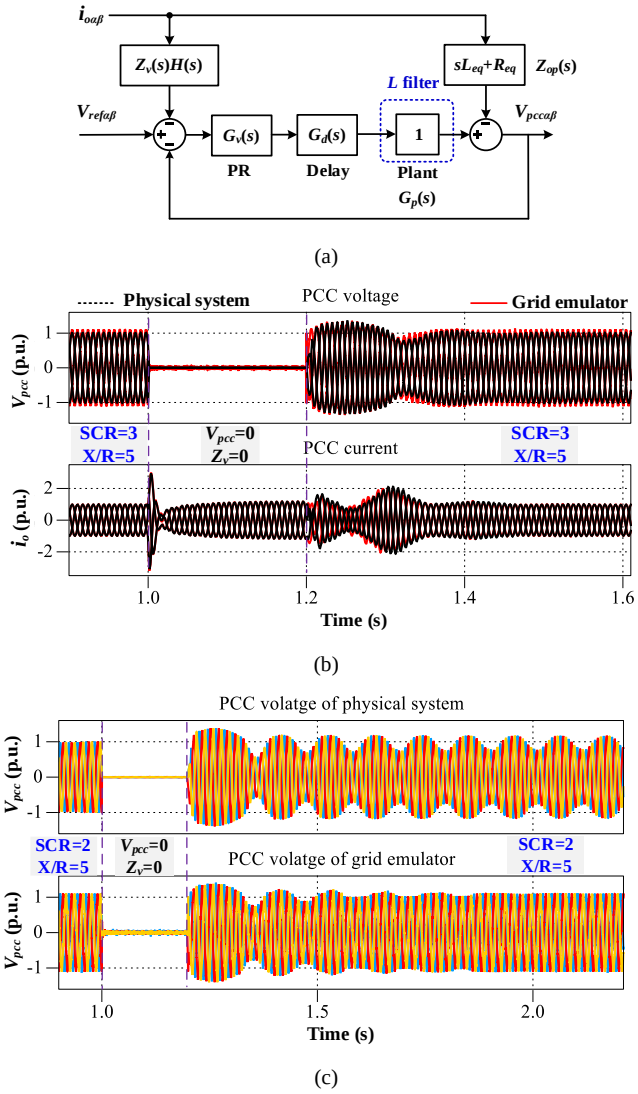

Fig. 20. The VC and VI control for impedance emulation in [64]. (a) Control diagram. (b) An LVRT test with post-fault SCR=3. (c) An LVRT test with post-fault SCR=2.

To address this issue, the virtual admittance (VA) control and current control (CC) is introduced in [63], [64]. Fig. 21 shows the control diagram and simulation results of LVRT tests for the grid emulator with an *L* filter. $Y_v(s)$ and $G_i(s)$ represent the VA and PR controller based current control. The open-loop gain of the VA control is given by

$$G_{opva}(s)=\frac{1}{R_v+sL_v}\left(K_{pc}+\frac{K_{rc}s}{s^2+\omega_1^2}\right)e^{-sT_d} \tag{23}$$

where R_v and L_v are the virtual resistance and inductance. K_{pc} and K_{rc} are the proportional gain and resonant gain of CC.

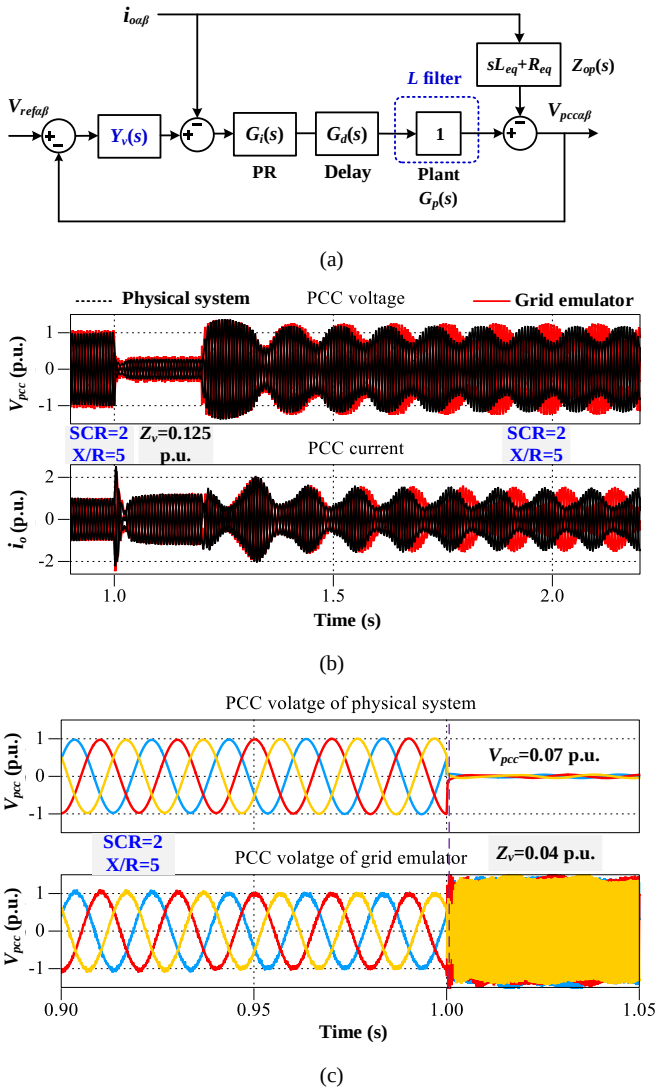

Fig. 21. The CC and VA control for impedance emulation in [64]. (a) Control diagram. (b) An LVRT test with post-fault SCR=2. (c) Emulating V_{pcc}=0.07 p.u. with small impedance during fault.

Generally, K_{rc} exhibits minimal phase delay at the phase-crossover frequency f_{cva}, i.e., $K_{rc}/(2\pi f_{cva})=K_{pc}/(10\sim20)$ [79]. To assure internal stability of system, K_{pc} should satisfy

$$\begin{cases} \mathrm{GM} \approx -20\lg\left[\dfrac{K_{pc}}{2\pi f_{cva} L_v}\right] > 0 \\ \mathrm{PM} \approx \pi - \dfrac{\pi}{2} - 2\pi f_{cva} T_d > 0 \end{cases} \Rightarrow K_{pc} < \frac{\pi L_v}{2T_d} \tag{24}$$

The output impedance of system is given by

$$Z_{GE}(s) = Z_v(s)\frac{Z_{op}(s)+G_i(s)G_d(s)}{Z_v(s)+G_i(s)G_d(s)} \overset{Low\ f}{\approx} Z_v(s)\frac{R_{eq}+K_{pc}}{R_v+K_{pc}} \tag{25}$$

Due to K_{pc}>>R_v, $Z_{GE}(s)$=$Z_v(s)$ can be guaranteed at the low-frequency range. Fig. 21(b) shows an LVRT test with post-fault SCR=2. Although the instability phenomenon is reproduced, the oscillating frequency in the converter-based grid emulation system cannot match that of the physical system. This is because the fundamental-frequency PR controller of the grid emulator cannot achieve the zero-error control of voltage fluctuation with divergent oscillating frequencies. The uncertainty of oscillations can further complicate the accurate emulation of grid impedance. Fig. 21(c) shows an LVRT test with Z_v=0.04 p.u. during fault. Emulating a small impedance by VA control tends to enlarge the open-loop gain $G_{opva}(s)$, causing the internal instability.

Similarly, in the *LC*-filtered grid emulator, the inaccurate low-frequency impedance emulation based on VC and VI control has been demonstrated in [10], [63]. Although the CC and VA control can also enhance the accuracy of the emulated impedance with a low SCR, emulating nearly zero impedances remains a challenge.

2) Co-emulation of multiple testing capabilities: Besides the co-emulation of voltage sags/swells and impedance variation, several studies also have explored the combination of other testing capabilities, e.g., flicker with frequency deviation [12], unbalance fault with harmonics [80], etc.

Generally, combining the control schemes required for individual testing capability can achieve the simultaneous emulation of multiple testing capabilities. Yet, two testing scenarios may complicate the parameterization of resonant controllers widely used in grid emulators. First, to combine the frequency deviation and other testing capabilities, the center frequencies of resonant controllers may need to vary with the frequency of reference signals [12]. The controller parameters based on the small-signal modeling may not work under large disturbances [81], [82]. Second, to simultaneously emulate flicker and inter-harmonics/harmonics, the center frequencies of resonant controllers may be close to each other, which may aggravate dynamic interactions among the adjacent resonant controllers, introducing more -*R* around harmonic frequencies.

V. Conclusion

This paper has discussed the testing capability requirements of power-electronic-based grid emulators, based on the recent developments of grid codes and standards. It has been pointed out that simultaneously realizing multiple testing capabilities can challenge the controllability and dynamic performance of converter-based grid emulators. Four types of dynamic interactions and corresponding solutions in the cascaded/interleaved NPC-, CHB- and MMC-based grid emulators has been thoroughly discussed. Open issues and emerging trends with the component design (e.g., NP/cell/SM capacitors and CVG-side transformer) and control improvement of converter-based grid emulators have been identified.

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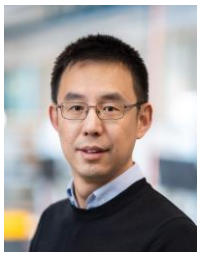

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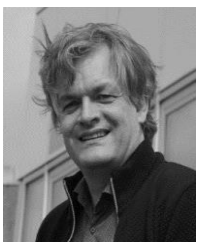

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