Triple-Mode Flying Inductor Common-Ground PV Inverter With Reactive Power Capability and Low Semiconductor Component Count

Hamed Heydari-doostabad, *Senior Member, IEEE*, Maryam Pourmahdi, Mohammad Monfared, *Senior Member, IEEE*, and Terence O'Donnell, *Senior Member, IEEE*

***Abstract*— This article proposes the flying inductor (FI)-based common-ground single-phase photovoltaic (PV) inverter which can support reactive power to the ac grid. The proposed buck-boost transformerless PV inverter eliminates the leakage current and is suitable for use in on-grid applications that require active and reactive power support. The proposed converter also features a low number of semiconductor devices, no ac type capacitor, acceptable quality of the grid-side current even during nonunity power factor operations, reducing switching loss by adopting a time-sharing technique, and high efficiency. The converter uses a dead-beat controller in the control loop which has a smooth, accurate, and fast response. Experimental results for a 500 W, 100 Vdc, and 180 Vdc to 110 Vrms prototype are provided in a closed-loop system in the presence of the proposed dead-beat controller. The results from the prototype validate the theoretical analysis and the applicability of the proposed structure. The converter exhibits the capability for stepping up the dc to ac power conversion and demonstrates a peak efficiency of 97.2% and 96.8% from 180 and 100 Vdc, respectively.**

***Index Terms*— Common-ground inverter, flying inductor (FI) converter, reactive power capability (RPC), transformerless photovoltaic (PV) inverter.**

I. Introduction

COMMON-GROUND transformerless photovoltaic (PV) inverters are fast becoming the dominant solution for distributed energy resources (DERs) due to their many advantages, including reduced electromagnetic interference (EMI) noise, elimination of leakage current, and higher efficiency.

In addition to reducing the EMI noise and leakage current, other requirements for the grid-connected PV inverters

Manuscript received 7 December 2023; revised 24 March 2024; accepted 17 April 2024. Date of publication 25 April 2024; date of current version 4 June 2024. This work was supported in part by a Grant from Science Foundation Ireland under Grant SFI/21/SPP/3756. Recommended for publication by Associate Editor Herbert Ho-Ching Iu. *(Corresponding author: Hamed Heydari-doostabad.)*

Hamed Heydari-doostabad, Maryam Pourmahdi, and Terence O'Donnell are with the School of Electrical and Electronic Engineering, University College Dublin (UCD), Dublin 4, D04 V1W8 Ireland (e-mail: hamed.heydari-doostabad@ucd.ie; maryam.pourmahdi-torghabe@ucdconnect.ie; terence.odonnell@ucd.ie).

Mohammad Monfared is with the Department of Electronic and Electrical Engineering, Swansea University, SA2 8PP Swansea, U.K., and also with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad 9177948974, Iran (e-mail: mohammad.monfared@swansea.ac.uk).

This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/JESTPE.2024.3393617.

Digital Object Identifier 10.1109/JESTPE.2024.3393617

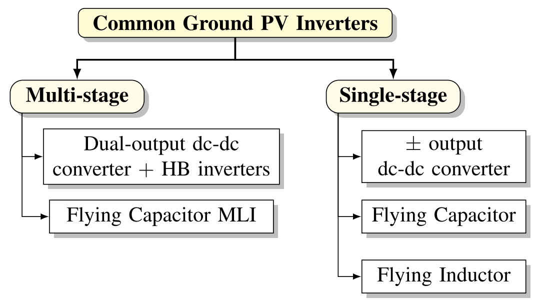


Fig. 1. Classification of common-ground inverters.

include: 1) the ability to provide reactive power to the ac grid as requested by IEEE 1547-2018 [1]; 2) a low active component count; and 3) buck-boost capability.

Different types of common-ground inverters have been reported in the literature, and based on their configuration, as shown in Fig. 1, they can be classified into the following list.

1) Single-stage inverters can be further classified as dc–dc converters with positive and negative voltage outputs, flying capacitor (FC), or flying inductor (FI) inverter configurations.
2) Multistage inverters can be further classified as the integration of a dual-output dc–dc converter and a half-bridge (HB) inverter and FC multilevel inverter (MLI) configurations.

In the case of the dual-output dc–dc converter in series with an HB inverter, a dc–dc converter with a midpoint at the output dc side is typically adopted as a prefront stage for different types of HB inverters. The converter in [2] employs two buck-boost dc–dc converters to regulate the dc bus voltage with positive, zero, and negative voltages and a conventional HB inverter generates sinusoidal output voltage. The converters in [3], [4], [5], and [6] have used the input and the output of the conventional buck-boost dc–dc converter as the prefront stage of the conventional HB, T-type, dual-buck, and buck inverter, respectively. Among all the converters in [2], [3], [4], [5], and [6], only [4] can generate reactive power, which is usually referred to as reactive power capability (RPC) for the ac grid. As regards buck-boost capability, the converter in [2] achieves this by using two buck-boost dc–dc converters, and the converter in [7] adopts one boost and one buck-boost converter in the input stage which gives stepping-up operation with no RPC.

dc–dc converters with positive and negative voltage gain ratios can also be used as inverters such as the topologies suggested in [8], [9], [10], and [11]. The voltage gain ratio of the converters in [8] and [9] (and also in [10]) is $(1 - 2d)/(d - d^2)$ [and $(1 - 2d)/(1 - d)$] and therefore the voltage gain is lower and more sensitive than that of the conventional buck-boost voltage gain ratio, that is, $d/(1-d)$. Moreover, the application of converters in [8], [9], and [10] is limited only to off-grid PV inverters since they are incapable of meeting the volt-var settings required by IEEE 1547-2018. As a successful solution, the converter in [11] has improved the voltage gain ratio and provided RPC at the cost of using nine semiconductor devices, three capacitors, and three inductors.

The FC common-ground inverters have been proposed in [12], [13], and [14] which require the input dc voltage level to be higher than the peak value of ac voltage, in other words, they are step-down converters. Moreover, the voltage ripple across the grid-side filter varies between zero and the dc-side voltage level. Hence, the grid-side filter is relatively large, and due to the larger current ripple of the FC converters, one can expect more core losses [15]. Recently, improved FC common-ground inverters have been reported such as the FC MLI in [16] and [17] and the integrated boost FC inverter in [18], [19], and [20]. However, the high number of active and passive components increases the volume and adds complexity to modulation and control algorithms. Furthermore, the large capacitor demands a significant amount of charging current which could damage the active components of the circuit.

The FI inverter is another type of common-ground inverter that provides the charging and discharging circuit loop for an inductor through both positive and negative half-cycles of ac grid. In other words, an inductor flies between connection to the input side and connection to the output side with the ability to connect it to the output positively or negatively during the positive or negative half-cycles. Consequently, FI-type inverters have a significant advantage that the ac-side current filter can be considerably smaller. In addition, they do not have the large capacitor and associated charging current requirements of the FC type converters.

With regard to the FI common-ground inverters, the first such inverter was proposed in [21]. The Karschny-inverter is based on a current source inverter with seven semiconductor devices and is capable of stepping-up the input dc voltage. However, the inability to support the ac grid by reactive power limits the use of the Karschny-inverter only for off-grid applications. Another FI inverter with five switches and three diodes has been proposed in [22] which offers the buck-boost voltage gain ratio, that is, $\pm d/(1-d)$, during either positive or negative half-cycle. The structure [22] has been updated by reverse blocking insulated gate bipolar transistors (RB-IGBTs) to reduce the number of semiconductor devices. However, the switching performance of the RB-IGBT is not optimized, and the reverse recovery current of the internal diode and turn-on losses of the associated IGBT are greater compared to standard fast freewheel diodes [23].

The converter in [24] uses only MOSFET switches and the converter in [25] uses MOSFET and discrete diodes in the structure of [22] and offers soft switching and the triple-mode switching strategy, respectively to improve the efficiency. However again, due to the inability of the FI-based converters in [22], [24], [25], and [26] to inject or absorb reactive power, they are not suitable for connection to the ac network.

Recently, the structure of [24] was further improved by a bidirectional MOSFET switch in [27]-type-1 and so it has nine semiconductor devices. The new FI-based converters have been presented as type-3 and type-4 in article [27] which both have six semiconductor devices. All the common-ground FI inverters in [27] use bidirectional MOSFET switches, they can support the ac grid with reactive power.

The converter described in [28] features eight switches, one diode, three capacitors, and two inductors. Operating with a two-stage power processing method, it offers the buck-boost capability and utilizes a five-level switched capacitor inverter that includes reactive power exchange capability. Moving on to [29], this converter is equipped with six switches, two diodes, two capacitors, and one inductor. Despite providing a voltage gain ratio of 2 through its switched capacitor design, it lacks reactive power exchange capability. Another noteworthy converter is discussed in [30], which has nine switches, two diodes, three capacitors, and one inductor. Offering reactive power exchange capability and a voltage gain ratio of 4, it operates as a switched capacitor nine-level inverter. In [31], an eight-switch configuration is combined with two diodes and two capacitors, featuring a switch capacitor type inverter capable of nine-level operation with RPC. Furthermore, the converter detailed in [32] incorporates eight switches, two diodes, three capacitors, and one inductor, providing both RPC and boost capability through its switch capacitor inverter design. Wang and Shan [33] present a converter comprising six switches, three diodes, three capacitors, and one inductor, offering both buck-boost capability and reactive power exchange capability.

In this article, a novel triple-mode FI common-ground (TMFICG) single-stage PV inverter is proposed. Significantly, this is an FI converter with RPC. In addition, it has a lower semiconductor device count compared to the previously published FI common-ground inverters, and unlike the previous converters, it does not require an ac type capacitor. Using a dc capacitor instead of ac capacitors offers several advantages, including reduced size and weight, lower cost, and enhanced reliability. DC capacitors are subjected to less voltage stress compared to ac capacitors, leading to increased longevity and improved performance. The proposed converter comprises a total of seven semiconductor devices (six switches and one diode). Despite this count, compared to the main common-ground FI inverters, the proposed inverter falls into the low-number category. This suggests that the proposed converter offers a relatively reduced semiconductor device count compared to typical common-ground FI inverters. To control the proposed inverter, the FI current indirect dead-beat controller (IDBC) and the grid-side current direct dead-beat controller are adopted during the positive and negative power regions (NPRs), respectively, which achieves

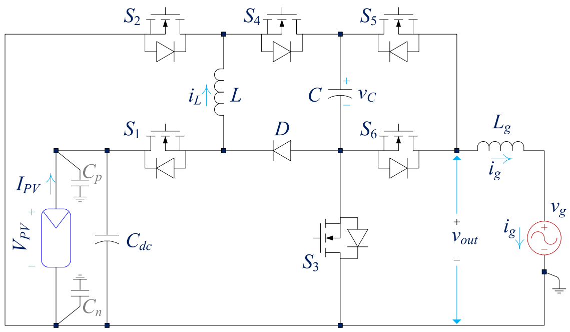


Fig. 2. Proposed TMFICG PV inverter.

accurate, fast, and smooth operation under different states of operation.

The rest of this article is organized as follows. The proposed FI common-ground inverter is presented in Section II. Section III is devoted to the practical considerations and design calculations for the proposed converter. A comprehensive comparative study with the state-of-the-art is presented in Section IV, the proposed dead-beat controller description is given in Section V and the experimental verification is provided in Section VI. Finally, Section VII concludes the article.

II. Proposed FI Common-Ground Inverter Operation Analysis

Fig. 2 shows the proposed flying-inductor common-ground PV inverter structure. V_{PV}, v_{out}, and v_g denote the PV voltage, the output voltage of the inverter, and the ac grid voltage, respectively. The proposed inverter consists of two inductors L and L_g, two capacitors C and C_{dc}, six switches S_1, S_2, S_3, S_4, S_5, and S_6, and one diode D. It is worth noting that the parasitic capacitor of the positive (C_p) and the negative rails (C_n) of the PV side are not actual capacitors; in fact, they are unintended capacitances inherent in the circuit design and physical configuration. These capacitances arise due to the stray capacitance between the cell-to-frame, cell-to-rack, and cell-to-ground [34]. These capacitors are not necessary for the operation of the proposed PV inverter but are essentially a result of the mechanical structure of the PV modules and their installation.

The proposed PWM scheme is shown in Fig. 3. The equivalent circuit for dual operation modes (buck and boost) during the positive half-cycle and single mode of buck-boost operation during the negative half-cycle of the grid-side ac voltage are shown in Fig. 4(a)–(c), respectively. Moreover, the steady-state operation modes during the NPR are shown in Fig. 4(d). To support the ac grid with the reactive power, during the NPRs, the proposed inverter injects negative (positive) current during the positive (negative) half-cycle of the ac voltage.

Four states for operation during the positive and the two states for the negative half-cycle are defined as follows.

A. Positive and Negative Half-Cycle Operation Modes

Mode-I [t_0–t_1] and [$t_2 - t_3$]: During $0 \le t \le dT_s$ (d represents the duty cycle) or state-1 of mode-I and according to Fig. 3, when the instantaneous ac grid voltage is lower than the input dc voltage level, the switches S_3 and S_5 are turned on and S_1 is PWM controlled while S_2, S_4, and S_6 are turned off.

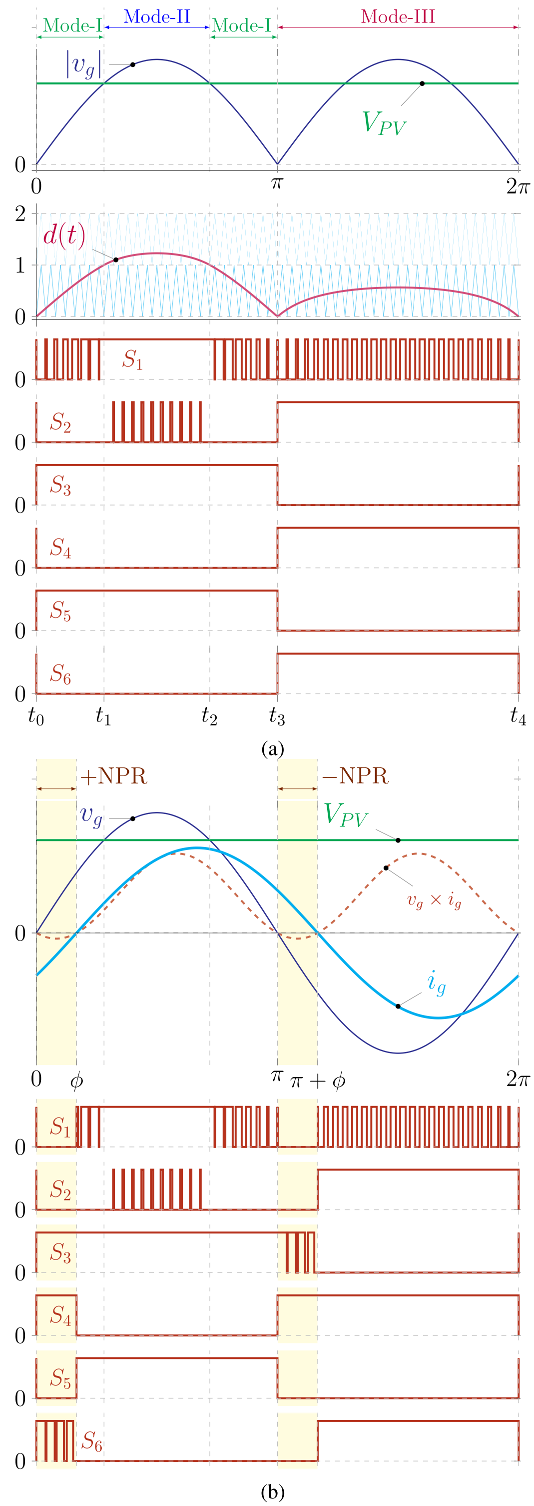


Fig. 3. Different modes of operation and PWM signals during (a) unity and (b) nonunity power factor.

As shown in Fig. 4(a) left, the FI L is charged from the input dc source, that is, V_{PV}. Furthermore, V_{PV} transfers the energy to v_g and the inductor filter L_g, through S_1, S_5, and the body diode of S_4. Moreover, the proposed converter is connected

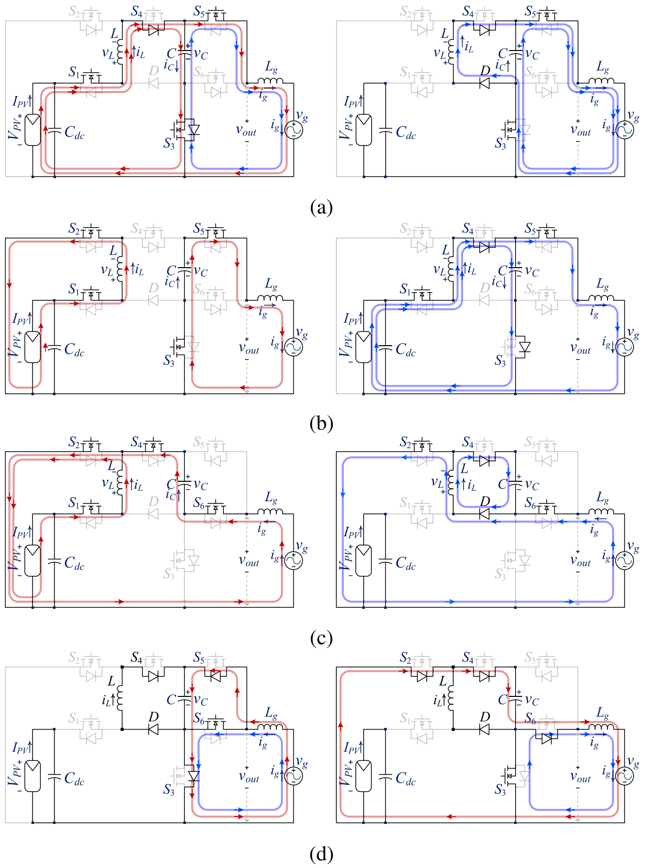


Fig. 4. Equivalent circuit of the proposed converter during the positive half-cycle: (a) mode-I and (b) mode-II. The negative half-cycle: (c) mode-III and (d) NPR (left: state-1 and right: state-2).

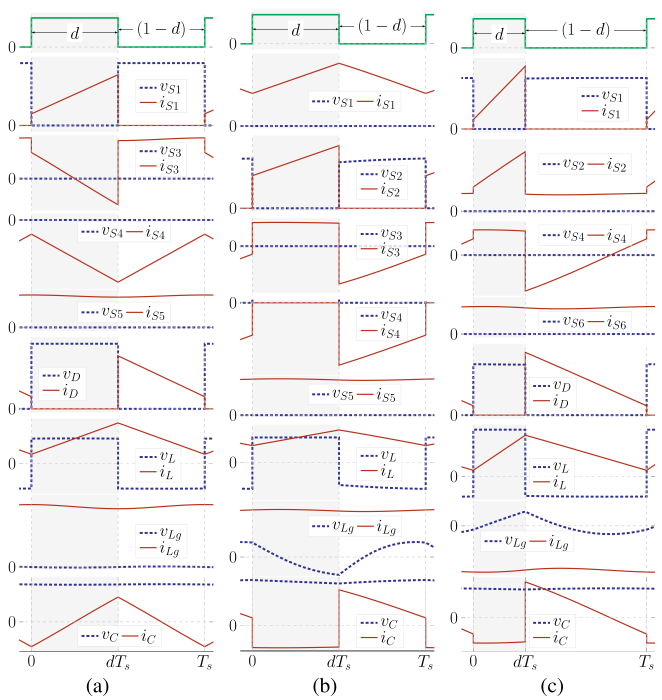


Fig. 5. Typical time-domain waveforms mode: (a) I, (b) II, and (c) III.

to the ac system via a dc-type capacitor, denoted as C. This dc capacitor charges and discharges from the dc side through the ac side during the positive half-cycle. Conversely, during the negative half-cycle, the converter switches the capacitor to discharge through the negative terminal of the ac grid. The capacitor C is first discharged into L_g and v_g through S_3 and S_5 and then charged from V_{PV} and L through S_1 and body diodes of S_3 and S_4. According to the typical time-domain waveforms in Fig. 5(a), the current through L increases, and the energy of L_g is increased from the input source and L. Thus, the derived voltage and current equations are

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = V_{\mathrm{PV}} - v_C = V_{\mathrm{PV}} - v_{\mathrm{out}} \\ i_C = C\dfrac{dv_C}{dt} = i_L - i_g. \end{cases} \tag{1}$$

During $dT_s \le t \le T_s$ or state-2 of mode-I as shown in Fig. 4(a) right, S_3 and S_5 are turned on, whereas S_1, S_2, S_4, and S_6 are turned off. During this state, L releases its energy to v_g and L_g, through S_3, S_5, D, and body diode of S_4. Moreover, C is discharged to the grid side through S_3 and S_5. According to the typical time-domain waveforms in Fig. 5(a), the current through L decreases, and the energy of L_g is released to the ac grid. Thus, the derived equations are

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = -v_C = -v_{\mathrm{out}} \\ -i_C = -C\dfrac{dv_C}{dt} = i_g - i_L. \end{cases} \tag{2}$$

By applying the volt-second and amp-second balances to L and C, respectively

$$d(V_{\mathrm{PV}} - v_C) + (1-d)(-v_C) = 0 \tag{3}$$

$$d(i_L - i_g) - (1-d)(i_g - i_L) = 0 \tag{4}$$

where $v_C = v_{\mathrm{out}}$.

From (3) and (4), the voltage conversion ratio of the proposed converter and i_L during the step-down mode-I for the positive half-cycle operation can be calculated as follows:

$$M_{\text{mode-I}} = \frac{v_{\mathrm{out}}}{V_{\mathrm{PV}}} = d \tag{5}$$

$$i_L = i_g. \tag{6}$$

Mode-II [t_1–t_2]: During $0 \le t \le dT_s$ or state-1 of mode-II and according to Fig. 3, when the instantaneous grid voltage is higher than the input dc voltage level, the switches S_1, S_3, and S_5 are turned on and S_2 is PWM controlled, while S_4 and S_6 are turned off. In Fig. 4(b) left, L is charged by V_{PV} and C releases its energy to L_g and v_g. Thus, the current through L increases, while the energy of L_g decreases. According to the typical time-domain waveforms in Fig. 5(b), the derived equations are

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = V_{\mathrm{PV}} \\ i_C = C\dfrac{dv_C}{dt} = i_g. \end{cases} \tag{7}$$

During $dT_s \le t \le T_s$ or state-2 of mode-II, as shown in Fig. 4(b) right, S_2, S_3, S_4, S_6, and D are turned off, whereas the body diode of S_3 and S_4 are conducting and the switches S_1 and S_5 are turned on. The inductor L in series with V_{PV}

releases its energy into C, L_g, and the ac grid. Hence, we have

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = V_{\rm PV} - v_C \\ i_C = C\dfrac{dv_C}{dt} = i_L - i_g. \end{cases} \tag{8}$$

Now the volt-second and amp-second balances are applied to L and C

$$d(V_{\rm PV}) + (1-d)(V_{\rm PV} - v_C) = 0 \tag{9}$$
$$d(i_g) + (1-d)(i_L - i_g) = 0. \tag{10}$$

As a result, the voltage gain ratio and i_L are

$$M_{\text{mode-II}} = \frac{v_{\rm out}}{V_{\rm PV}} = \frac{1}{1-d} \tag{11}$$
$$i_L = \frac{1}{1-d} i_g. \tag{12}$$

Mode-III [t_3–t_4]: During $0 \le t \le dT_s$ or state-1 of mode-III and according to Fig. 3, the switches S_2, S_4, and S_6 are turned on and S_1 is PWM controlled, while S_3 and S_5 are turned off and D is not conducting. In Fig. 4(c) left, the FI L is charged from $V_{\rm PV}$. Moreover, L_g is charged by the released energy from C. Thus, the current through L and L_g increases. According to the typical time-domain waveforms in Fig. 5(c), the derived equations are

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = V_{\rm PV} \\ i_C = C\dfrac{dv_C}{dt} = -i_g. \end{cases} \tag{13}$$

During $dT_s \le t \le T_s$ or state-2 of mode-III as shown in Fig. 4(c) right, the switches S_1, S_3, S_4, and S_5 are turned off, while S_2, S_6, D, and the body diode of S_4 are on. In this period, L and L_g are discharged to v_g. Moreover, C is charged by the released energy from L. In this state, the derived current and voltage equations are

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = -v_C \\ i_C = C\dfrac{dv_C}{dt} = i_L - i_g. \end{cases} \tag{14}$$

Again from the volt-second and amp-second balances, one can obtain

$$d(V_{\rm PV}) + (1-d)(-v_C) = 0 \tag{15}$$
$$d(-i_g) + (1-d)(i_L - i_g) = 0. \tag{16}$$

Therefore, the voltage conversion ratio of the proposed converter during the negative half-cycle and i_L can be calculated as follows:

$$M_{\text{mode-III}} = \frac{v_{\rm out}}{V_{\rm PV}} = \frac{-d}{1-d} \tag{17}$$
$$i_L = \frac{1}{1-d} i_g. \tag{18}$$

B. NPR Operation Modes

During the positive half-cycle of the grid voltage, Fig. 4(d) left, and when i_g is negative, as shown in Fig. 3, S_6 is PWM controlled and when it turns off, the current through L_g increases in the circuit consisting of C, and the antiparallel diodes of S_3 and S_5. When S_6 is turned on, the negative current can flow in the freewheeling circuit consisting of S_6 and the body diode of S_3.

During the negative half-cycle of the grid voltage, Fig. 4(d) right, and when i_g is positive when S_3 is off, the current can increase and flowthrough L_g in the circuit consisting of C the antiparallel diodes of S_2, S_4, and S_6. When S_3 is turned on the negative current decreases and flows the freewheeling circuit consisting of S_3 and body diode of S_6.

By using the switching strategy as described, the proposed FI converter can inject or absorb reactive power to the ac grid while preserving the quality of the grid current. Therefore, the proposed converter can satisfy the volt-var setting requirements of standards such as IEEE 1547-2018.

III. Design Considerations

A. Passive Components Design

$C_{\rm dc}$ acts as a buffer for the instantaneous power difference between the ac grid and the dc side of PV. Thus, to maintain the ripple of the dc-link voltage ($\Delta V_{\rm dc}$) below a specific value, the required $C_{\rm dc}$ is

$$C_{\rm dc} = \frac{P_{\rm PV}}{\omega_0 V_{\rm PV} \Delta V_{\rm dc}} \tag{19}$$

where $P_{\rm PV}$ is the average output power of the PV, ω_0 is the grid angular frequency, and $V_{\rm PV}$ is the PV-side dc voltage.

The FI L performs the role of either step-down or step-up for the positive and step-down-up for the negative half-cycles. For all three operation modes, L can be decided with respect to the tolerable current ripple Δi_L. Δi_L in each operation mode can be calculated as follows:

$$\Delta i_{L,\text{mode-I}} = \frac{(V_{\rm PV} - |v_g|)|v_g|}{V_{\rm PV} L} T_s \tag{20}$$
$$\Delta i_{L,\text{mode-II}} = \frac{V_{\rm PV}(|v_g| - V_{\rm PV})}{|v_g| L} T_s \tag{21}$$
$$\Delta i_{L,\text{mode-III}} = \frac{V_{\rm PV}|v_g|}{(V_{\rm PV} + |v_g|)L} T_s. \tag{22}$$

In the above equations, T_s is the switching period. Thus, after deciding the permissible Δi_L, one can calculate L

$$L_{\text{mode-I}} \ge \frac{|v_g|(V_{\rm PV} - |v_g|)}{V_{\rm PV} \Delta i_L} T_s \tag{23}$$
$$L_{\text{mode-II}} \ge \frac{V_{\rm PV}(|v_g| - V_{\rm PV})}{|v_g| \Delta i_L} T_s \tag{24}$$
$$L_{\text{mode-III}} \ge \frac{V_{\rm PV}.|v_g|}{(V_{\rm PV} + |v_g|)\Delta i_L} T_s. \tag{25}$$

The inductor can, therefore, be chosen to be greater than the largest of these which depends on the specific application values of $V_{\rm PV}$ and amplitude of v_g.

Similarly, the value of grid-side inductor, L_g, is chosen from the maximum allowed current ripple, Δi_g, as follows:

$$L_g \geq \frac{\Delta v_C}{2\Delta i_g} T_s. \tag{26}$$

Equation (27) indicates that the current ripple during the positive power region (PPR) is influenced by the difference between v_C and v_g, while during the NPR, it is primarily influenced by v_g. Therefore, during the NPR, the grid-side experiences more ripple

$$\begin{cases} \Delta i_g = \dfrac{(1 - d_{\text{mode-I,III}})T_s|v_C - v_g|}{2L_g}, & \text{PPR} \\ \Delta i_g = \dfrac{(1 - d_{\pm\text{NPR}})T_s v_g}{2L_g}, & \text{NPR.} \end{cases} \tag{27}$$

To keep the output voltage ripple (Δv_C) below a certain value, the capacitor C must satisfy

$$C \geq \frac{\Delta Q_C}{\Delta v_C} \tag{28}$$

where ΔQ_C is the total capacitor charge change and can be calculated as follows:

$$\Delta Q_{C,\text{mode-I}} = \frac{(V_{\text{PV}} - v_g)v_g}{8LV_{\text{PV}}} T_s^2 \tag{29}$$

$$\Delta Q_{C,\text{mode-II}} = I_g \frac{v_g - V_{\text{PV}}}{v_g} T_s \tag{30}$$

$$\Delta Q_{C,\text{mode-III}} = I_g \frac{v_g}{V_{\text{PV}} + v_g} T_s. \tag{31}$$

Considering $P_{\text{PV}} = 500$ W, $v_g = 110\sqrt{2}\sin\omega_0 t$, and $V_{\text{PV}} = 100$ V, the value of $L = 1.0$ mH satisfies (23)–(25) for a current ripple below 20%.

From (26) and considering 4% as the maximum tolerable ripple of the injected current, the value of L_g is calculated as 400 μH. Replacing from (29) to (31) in (28) with the assumption that the maximum voltage ripple is 40%, then the required capacitance of C is about 2.2 μF.

B. Semiconductors Ratings

The average (over a switching cycle) ON-state current and average OFF-state voltage across the switches and the diode can be expressed as follows:

$$\text{Mode-I:} \begin{cases} V_{S1} = [1 - d(t)]V_{\text{PV}} \\ V_{S2} = V_{S6} = V_{\text{out}} \\ V_{S3} = V_{S4} = V_{S5} = 0 \\ V_D = [d(t)]V_{\text{PV}} \end{cases}, \begin{cases} I_{S1} = [d(t)]I_L \\ I_{S3} = I_D \\ \quad = [1 - d(t)]I_L \\ I_{S4} = I_{S5} = I_L \\ I_{S2} = I_{S6} = 0 \end{cases} \tag{32}$$

$$\text{Mode-II:} \begin{cases} V_{S2} = [1 - d(t)]V_{\text{out}} \\ V_{S1} = V_{S3} = V_{S5} = 0 \\ V_{S4} = [d(t)]V_{\text{out}} \\ V_{S6} = V_{\text{out}} \\ V_D = [d(t)]V_{\text{PV}} \end{cases}, \begin{cases} I_{S1} = I_L \\ I_{S2} = [d(t)]I_L \\ I_{S3} = [d(t)]I_g + \\ [1 + d(t)](I_L - I_g) \\ I_{S4} = I_{S5} = I_g \\ I_{S6} = I_D = 0 \end{cases} \tag{33}$$

$$\text{Mode-III:} \begin{cases} V_{S1} = [1 - d(t)] \\ (V_{\text{PV}} - V_{\text{out}}) \\ V_{S2} = V_{S4} = V_{S6} = 0 \\ V_{S3} = V_{S5} = -V_{\text{out}} \\ V_D = [d(t)] \\ (V_{\text{PV}} - V_{\text{out}}) \end{cases}, \begin{cases} I_{S1} = [d(t)]I_L \\ I_{S2} = I_L \\ I_{S3} = I_{S5} = 0 \\ I_{S4} = [d(t)]I_g \\ I_{S6} = I_g \\ I_D = [1 - d(t)]I_L. \end{cases} \tag{34}$$

Therefore, the rms value of total current stress (TCS) and total voltage stress (TVS) of semiconductor devices during each mode is

$$\text{Mode-I:} \begin{cases} \text{TVS}_{\text{rms}} = [2d + 1]V_{\text{PV}} \\ \text{TCS}_{\text{rms}} = \sqrt{16 - 7d}\, I_g \end{cases} \tag{35}$$

$$\text{Mode-II:} \begin{cases} \text{TVS}_{\text{rms}} = \dfrac{3 - d}{1 - d} V_{\text{PV}} \\ \text{TCS}_{\text{rms}} = \dfrac{\sqrt{d[4 - 2d]^2 + 9[1 - d]}}{1 - d} I_g \end{cases} \tag{36}$$

$$\text{Mode-III:} \begin{cases} \text{TVS}_{\text{rms}} = \dfrac{|2d + 1|}{1 - d} V_{\text{PV}} \\ \text{TCS}_{\text{rms}} = \dfrac{\sqrt{8d^3 - 23d^2 + 10d + 9}}{1 - d} I_g. \end{cases} \tag{37}$$

IV. Comparison of the Proposed FI Inverter to the State of Art

A comparative study of the main characteristics of the other successful common-ground FI PV inverters and the proposed inverter are provided in Table I.

The main point of Table I is that the proposed converter has the lowest semiconductor device count without any limitation on the ability to support ac grid with reactive power. The proposed FI converter has seven semiconductor devices and adapts the triple-mode operation to reduce unnecessary switching losses. The total semiconductor device count of FI inverters, that is, the proposed converter, and the converters in [21], [22], [25], [26], and [27] type-I, type-III, and type-IV is 7, 7, 8, 8, 8, 9, 8, and 8, respectively. Although the total semiconductor device count of the converter in [21] is similar to the proposed converter, it is not able to meet the requirements of IEEE 1547-2018 in terms of reactive power provision.

As shown in Table I, while the converters in [35] possess RPC functionality and the type-IV converter can be classified as an FI-based converter, their applications are limited due to their step-down voltage gain ratio.

The proposed converter has fewer elements compared to [11], however, it operates with all four semiconductor devices conducting in all modes, while [11] employs varying numbers of devices in different modes. Although the total harmonic distortion (THD) difference is minimal, it can be attributed to the transition from buck to boost mode in the proposed converter may also contribute to the slight THD increase.

Converter [36] also offers advantages such as a low number of semiconductor devices, which can help reduce costs and simplify the overall circuit design. However, it lacks the buck-boost operation of the proposed converter. Additionally, it operates in two stages of power processing, potentially impacting overall efficiency.

Converter [6], on the other hand, shares the advantage of a single-stage power conversion with the proposed converter, simplifying the design and reducing complexity. It also has a low number of semiconductor devices, contributing to cost savings. However, it lacks both the buck-boost operation and the RPC. Additionally, it employs an FC inverter, which may introduce core loss.

Converter [7] offers the advantage of buck-boost operation, similar to the proposed converter, allowing for voltage regulation. It also operates in a single stage, simplifying the circuit design. However, it lacks the RPC and has a high number of semiconductor devices, which can increase costs and complexity.

Converter [37] shares the advantages of buck-boost operation and RPC with the proposed converter. However, it employs an FC inverter and operates in two stages, potentially impacting efficiency and introducing complexity.

Another comparison can be made between the proposed converter and its main competitors based on the normalized rms value of TVS (TVS_{rms}/V_{PV}) and the normalized rms value of TCS of semiconductor devices (TCS_{rms}/I_g). The comparisons are presented in Table II and shown in Figs. 6 and 7, respectively, where TVS and TCS are plotted versus voltage gain ratio. It can be seen that depending on the voltage gain ratio, the proposed converter can be either better or worse than previous converters. At lower gains, the proposed converter outperforms the competitors. For example, the proposed converter offers the lowest TVS_{rms}/V_{PV} when the gain voltage in lower than 0.5 and 1.0 during positive and negative half-cycles, respectively.

Also, TCS_{rms}/I_g of the proposed converter is lower than converter in [21], [22], [26], and [27] type-III during the positive half-cycle and lower than TCS of [27] type-IV at the voltage gains higher than 2.0. It can be seen that TCS_{rms}/I_g of converters in [21], [22], and [26] and converter in [25] during the negative half-cycle is lower than the proposed converter although the converters in [22], [25], [26], and [27] have one more semiconductor device and are not able to support reactive power.

It is also useful to compare the high-frequency switching semiconductor device count of the proposed converter and the main competitors. As shown in Table I, it is clear that the proposed converter has only two high-frequency switching semiconductor devices during each mode which is the lowest compared to all the other FI PV inverters.

It is also worth noting that, unlike the previously published FI inverters, the proposed inverter uses only dc type capacitors in the structure which can reduce the volume and cost of the PV inverter.

Furthermore, as will be shown in Section VI, the measured maximum efficiency of the proposed converter is 97.2%, the leakage current is eliminated and it provides RPC. In summary, the proposed converter presents a good balance between the component count, number of high-frequency switching components, semiconductor device ratings, common ground between the PV side and the output terminals, and efficiency which makes it a practical solution for PV power converter units.

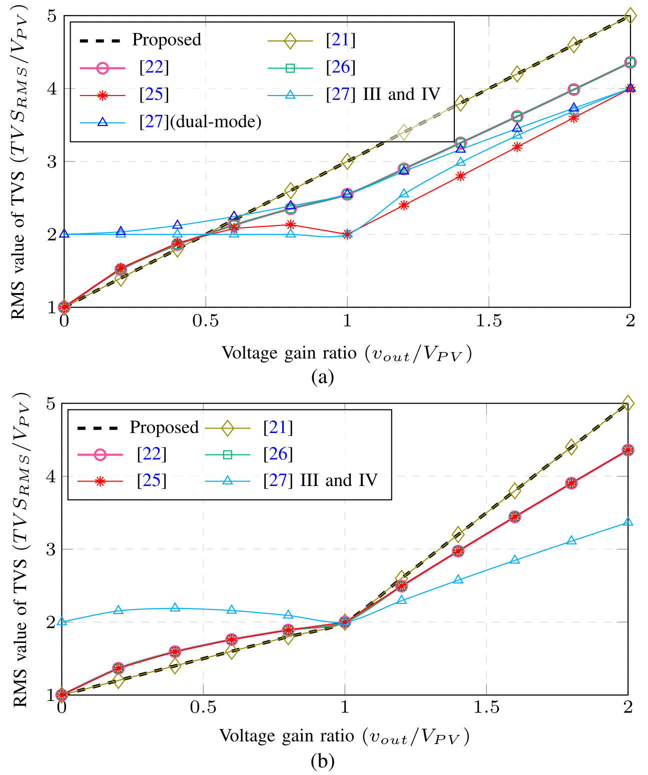


Fig. 6. RMS value of TVS during (a) positive and (b) negative half-cycles.

The advantages and disadvantages of the proposed converter, in comparison with the primary common-ground inverters, are outlined in Table III. Specifically, converters referenced in [21], [22], [24], [25], [26], and [37] lack the capability for reactive power exchange with the ac grid. Additionally, converters cited in [35] lack both buck and boost capabilities. Moreover, converters referenced in [11], [22], [24], [25], [26], [27], and [37] utilize a greater number of semiconductor devices compared to the proposed converter.

V. Control System Design

The control system is based on a deadbeat controller which includes the control of the grid-side current during both positive and NPRs. It is assumed that the reference value of grid-side current amplitude and phase, that is, I_g^* and ϕ^* is calculated by a maximum power point tracking (MPPT) loop and the volt-var setting of IEEE-1547-2018, respectively, which are not described here. As shown in Fig. 8(a), from v_g and i_g the duration of the positive or NPRs can be determined, and if the operation is in the NPR then NPR = 1. If NPR = 1, then the control diagram as shown in Fig. 8(b) applies and the duty cycle is calculated using (64) and (65) depending on whether the grid v_g voltage is positive or negative, respectively.

When NPR $\neq$ 1 and $v_g \geq 0$, then the converter will operate in either mode-I or mode-II depending on whether the instantaneous value of grid voltage is lower or higher than V_{PV}. The optimal duty cycle of mode-I or mode-II can be calculated using (61) and (62), respectively. Similarly, when NPR $\neq$ 1 and $v_g < 0$, the optimal duty cycle for mode-III operation will be calculated according to (63). The overall

TABLE I
COMPARISON AMONG MAIN COMMON-GROUND INVERTERS

Ref.	Number of Elements†	Conducting S or D @ modes and half-cycles	High Freq S or D @ modes and half-cycles	$\frac{v_{out}}{V_{PV}}$	Main test results RPC?
Proposed	6 S 1 D 2 L, 2 C	+, I: 4, 4 +, II: 4, 4 −, III: 4, 4	+, I: 2 +, II: 2 −, III: 2	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	180, $100V_{dc}$,$110V_{ac}$ $500W$,$20kHz$ η_{max}:97.2% THD:3.1% RPC:✓
[21]	5 S 2 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	NA RPC:×
[22]	5 S 3 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$92V_{dc}$,$100V_{ac}$ $193W$,$10kHz$ η_{max}:− THD:4.9% RPC:×
[26]	5 S 3 SD 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$200V_{dc}$,$220V_{ac}$ $200W$, $20kHz$ η_{max}:< 96% THD:− RPC:×
[24]	8 S 0 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$100V_{dc}$,$220V_{ac}$ $200W$, $10kHz$ η_{max}:95% THD:3.3% RPC:×
[25]	5 S 3 D 2 L, 2 C	+, I: 3, 4 +, II: 2, 3 −, III: 2, 3	+, I: 3 +, II: 3 −, III: 3	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	200, $130V_{dc}$,$110V_{ac}$ $500W$, $40kHz$ η_{max}:98.81% THD:4.28% RPC:×
[11]	3 S 6 D 3 L, 3 C	+: 2, 4 −: 2, 3	+: 4 −: 4	$\frac{\pm d}{1-d}$	180, $100V_{dc}$,$110V_{ac}$ $500W$, $20kHz$ η_{max}:97.5% THD:3% RPC:✓
[27] I	9 S 0 D 2 L, 2 C	+, I: 3, 4 +, II: 3, 3 + : 3, 4 − : 3, 4	+, I: 3 +, I: 4 +: 7 −: 3	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	NA RPC:✓
[27] III	8 S 0 D 2 L, 2 C	+, I: 4, 3 +, II: 4, 4 + : 4, 3 − : 3, 3	+, I: 2 +, I: 4 +: 6 −: 3	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	100, $400V_{dc}$,$230V_{ac}$ $2kW$, $25kHz$ η_{max}:97.5% THD:− RPC:✓
[27] IV	8 S 0 D 2 L, 2 C	+, I: 3, 3 +, II: 3, 3 +: 3, 3 −: 3, 3	+, I: 2 +, II: 4 +: 6 −: 4	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	NA RPC:✓
[35] III	2 S 0 D 2 L, 2 C	+: 1, 1 −: 1, 1	+: 2 −: 2	$\frac{1-2d}{1-d}$	$400V_{dc}$,$220V_{ac}$ $1kW$, $50kHz$ η_{max}:95.25% THD:− RPC:✓
[6]	4 S 2 D 3 L, 2 C	+: 1, 2 −: 2, 2	+: 1 −: 1	d $\frac{-d}{1-d}$	$180V_{dc}$,$110V_{ac}$ $350W$,$37kHz$ η_{max}:98.55% THD:2.53% RPC:×
[7]	5 S 3 D 3 L, 3 C	+, I: 2, 3 +, II: 2, 2 −, III: 2, 2	+, I: 3 +, II: 2 −, III: 2	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	$192V_{dc}$,$110V_{ac}$ $450W$,$75kHz$ η_{max}:97.22% THD:1.81% RPC:×
[37]	5 S 1 D 2 L, 2 C	+: 3, 3, 2 −: 3, 3, 2	+: 3 −: 3	$\frac{d}{1-d}$ $\frac{-d}{1-d}$	$75V_{dc}$,$110V_{ac}$ $1000W$,$10kHz$ η_{max}:96% THD:2.18% RPC:×
[36]‡	4 S 0 D 2 L, 2 C	+: 3, 3 −: 3, 3	+: 4 −: 4	$\frac{d_i - d_b}{1-d_b}$	$400V_{dc}$,$240V_{ac}$ 3 kVA,$75kHz$ η_{max}:< 97% THD:2.1% RPC:✓

† S: switch, D: diode, SD: series body diode, L: inductor, C: capacitor.
‡ d_i: inverter stage duty-cycle in [36] and d_b: boost stage duty-cycle in [36].

TABLE II
RMS VALUE OF TOTAL VOLTAGE AND CURRENT STRESS

Ref.	TVS_{RMS}/V_{PV} ± half cycle	TCS_{RMS}/i_g ± half cycle
Proposed	$(2d+1)$, $\frac{3-d}{1-d}$, $\frac{\lvert 2d+1\rvert}{1-d}$	$\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{d(4-2d)^2+9(1-d)}$, $\frac{1}{1-d}\sqrt{8d^3-23d^2+10d+9}$
[21]	$\frac{1+d}{1-d}$, $\frac{\lvert 4d-1\rvert}{1-d}$	$\frac{1}{1-d}\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[22]	$\frac{1}{1-d}\sqrt{d(1+\lvert 2d-1\rvert)^2+(1-d)(1+d)^2}$, $\frac{1}{1-d}\sqrt{d(1+\lvert 2d-1\rvert)^2+(1-d)(4d-1)^2}$	$\frac{1}{1-d}\sqrt{16-12d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[26]	$\frac{1}{1-d}\sqrt{d(1+\lvert 2d-1\rvert)^2+(1-d)(1+d)^2}$, $\frac{1}{1-d}\sqrt{d(1+\lvert 2d-1\rvert)^2+(1-d)(4d-1)^2}$	$\frac{1}{1-d}\sqrt{16-12d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[25]	$\sqrt{4d+(1-d)(2d+1)^2}$, $\frac{2}{1-d}$, $\frac{1}{1-d}\sqrt{d(1+\lvert 2d-1\rvert)^2+(1-d)(4d-1)^2}$	$\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{9-5d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[27] III	2, $\frac{1}{1-d}\sqrt{d(3-2d)^2+4(1-d)}$, $\frac{1}{1-d}\sqrt{d(2-d)^2+(1-d)(1+\lvert 2d-1\rvert)^2}$, $\frac{1}{1-d}\sqrt{d(2-2d+\lvert 2d-1\rvert)^2+(1-d)(1+\lvert 2d-1\rvert)^2}$	$\sqrt{9+7d}$, $\frac{4}{1-d}$, $\frac{1}{1-d}\sqrt{9+7d}$, $\frac{3}{1-d}$
[27] IV	2, $\frac{1}{1-d}\sqrt{d(3-2d)^2+4(1-d)}$, $\frac{1}{1-d}\sqrt{d(2-d)^2+(1-d)(1+\lvert 2d-1\rvert)^2}$, $\frac{1}{1-d}\sqrt{d(2-2d+\lvert 2d-1\rvert)^2+(1-d)(1+\lvert 2d-1\rvert)^2}$	3, $\frac{3}{1-d}$, $\frac{3}{1-d}$, $\frac{3}{1-d}$

diagram of the proposed control system during the PPR is shown in Fig. 8(c).

After determining $d(t)$ for all three modes and NPR, the PWM module generates the gate signals for the switches.

In the inner current control loop, a simple, fast, and effective digital dead-beat current control system is adopted to calculate the duty cycles for all modes [38], [39], [40], [41].

During the positive power mode, the controller regulates the ac-side current indirectly by controlling the current though the FI L. The reference for the FI current is established with (66) and the phase information provided by the PLL. The outputs of (66) become a reference for the inner current control loop. The optimal duty cycle, for the FI converter, can therefore be determined from the measured V_{PV} and v_{out} voltage, and the measured and reference current through the FI L. During the NPR the controller directly regulates the current through the output filter inductor L_g.

In the outer loop, the grid or reference voltage is fed to the PLL to determine the phase angle of the ac voltage, that is, ω. By using I_g^* and $\sin(\omega t + \phi^*)$, the reference value of instantaneous ac current can be obtained. The relationships necessary for calculating the duty cycles in the various modes

TABLE III
PROS AND CONS OF MAIN COMMON-GROUNDED INVERTERS

Ref.	Pros (✓) and Cons (×)
Proposed	✓ Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[21]	✓ Buck-boost operation × No reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[22], [26], [24], [25]	✓ Buck-boost operation × No reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter × High number of semiconductor devices
[35] type-4	× Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[35] type-1,2,3	× Buck-boost operation ✓ Reactive power capability × Flying capacitor inverter ✓ Single-stage power converter
[11]	✓ Buck-boost operation ✓ Reactive power capability ✓ ± output dc-dc converter ✓ Single-stage power converter × High number of semiconductor devices
[27]	✓ Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter × High number of semiconductor devices
[37]	✓ Buck-boost operation × Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter

are described in the following. During mode-I and in the positive half-cycle, when S_1 is ON, the voltage across the FI L can be determined as follows:

$$v_L = L\frac{di_L}{dt} = V_{\mathrm{PV}} - v_{\mathrm{out}}. \tag{38}$$

Therefore, the slope of L current during S_1 ON-state in mode-I ($\delta_{\mathrm{I,ON}}$) is

$$\delta_{\mathrm{I,ON}} = \frac{di_L(t)}{dt} = \frac{V_{\mathrm{PV}} - v_{\mathrm{out}}}{L}. \tag{39}$$

When S_1 is OFF and D is conducting, the inductor voltage is

$$v_L = L\frac{di_L}{dt} = -v_{\mathrm{out}} \tag{40}$$

and slope of i_L when S_1 is OFF ($\delta_{\mathrm{I,OFF}}$) can be expressed as follows:

$$\delta_{\mathrm{I,OFF}} = \frac{di_L(t)}{dt} = \frac{-v_{\mathrm{out}}}{L}. \tag{41}$$

Similarly, during mode-II in the positive half-cycle, when the switch S_2 is ON, the voltage across L can be expressed as follows:

$$v_L = L\frac{di_L}{dt} = V_{\mathrm{PV}} \tag{42}$$

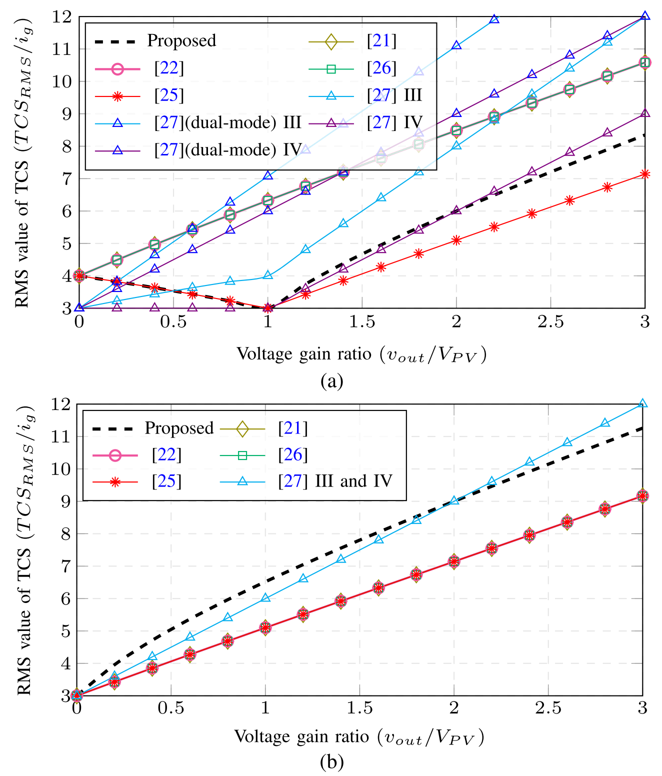


Fig. 7. Rms value of TCS during (a) positive and (b) negative half-cycles.

and when S_2 is OFF, the inductor voltage is

$$v_L = L\frac{di_L}{dt} = V_{\mathrm{PV}} - v_{\mathrm{out}}. \tag{43}$$

The slope of the L current during S_2 ON-state ($\delta_{\mathrm{II,ON}}$) and OFF-state ($\delta_{\mathrm{II,OFF}}$) can be expressed as follows:

$$\delta_{\mathrm{II,ON}} = \frac{di_L(t)}{dt} = \frac{V_{\mathrm{PV}}}{L} \tag{44}$$

$$\delta_{\mathrm{II,OFF}} = \frac{di_L(t)}{dt} = \frac{V_{\mathrm{PV}} - v_{\mathrm{out}}}{L}. \tag{45}$$

During mode-III in the negative half-cycle, when the switch S_1 is ON, the voltage across L can be expressed as follows:

$$v_L = L\frac{di_L}{dt} = V_{\mathrm{PV}} \tag{46}$$

and when S_1 is OFF, the inductor voltage is

$$v_L = L\frac{di_L}{dt} = v_{\mathrm{out}}. \tag{47}$$

The slope of the L current during S_1 ON-state ($\delta_{\mathrm{III,ON}}$) and OFF-state ($\delta_{\mathrm{III,OFF}}$) can be expressed as follows:

$$\delta_{\mathrm{III,ON}} = \frac{di_L(t)}{dt} = \frac{V_{\mathrm{PV}}}{L} \tag{48}$$

$$\delta_{\mathrm{III,OFF}} = \frac{di_L(t)}{dt} = \frac{v_{\mathrm{out}}}{L}. \tag{49}$$

In the NPR and during the time that the ac grid voltage is positive, the voltage across L_g and the current slope of L_g during S_6 ON-state ($\delta_{+\mathrm{NPR,ON}}$) and OFF-state ($\delta_{+\mathrm{NPR,OFF}}$) can be expressed as follows:

$$v_{Lg} = L_g\frac{di_{Lg}}{dt} = -v_g \tag{50}$$

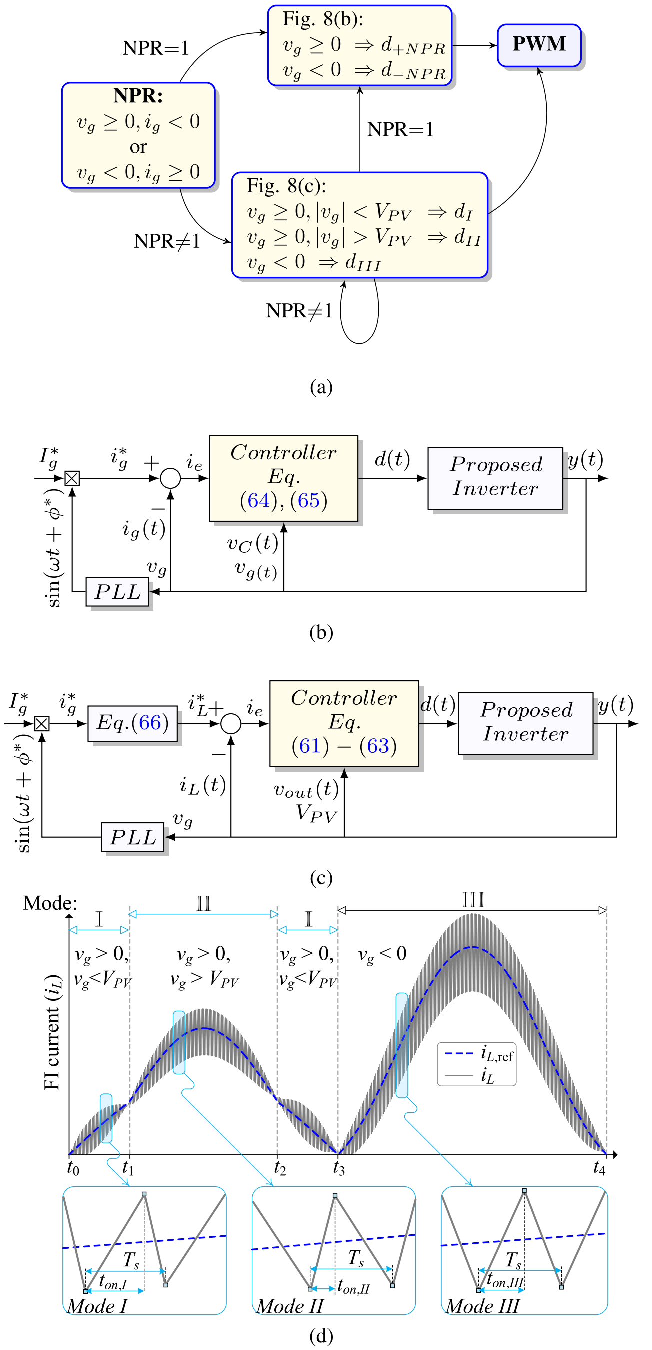


Fig. 8. (a) Proposed control system diagram. (b) Control system during negative. (c) PPR. (d) Variation of the FI current $i_L(t)$.

$$\delta_{+\mathrm{NPR,ON}} = \frac{di_{Lg}(t)}{dt} = \frac{-v_g}{L_g} \tag{51}$$

$$v_{Lg} = L_g \frac{di_{Lg}}{dt} = v_C - v_g \tag{52}$$

$$\delta_{+\mathrm{NPR,OFF}} = \frac{di_{Lg}(t)}{dt} = \frac{v_C - v_g}{L_g}. \tag{53}$$

Similarly, in the NPR and during the negative half-cycle of ac grid voltage, the voltage across L_g and the current slope of L_g during S_3 ON-state ($\delta_{-\mathrm{NPR,ON}}$) and OFF-state ($\delta_{-\mathrm{NPR,OFF}}$) can be expressed as follows:

$$v_{Lg} = L_g \frac{di_{Lg}}{dt} = -v_g \tag{54}$$

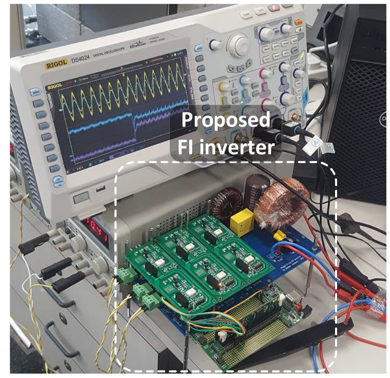


Fig. 9. Experimental prototype of the proposed TMCGFI inverter.

$$\delta_{-\mathrm{NPR,ON}} = \frac{di_{Lg}(t)}{dt} = \frac{-v_g}{L_g} \tag{55}$$

$$v_{Lg} = L_g \frac{di_{Lg}}{dt} = -v_C - v_g \tag{56}$$

$$\delta_{-\mathrm{NPR,OFF}} = \frac{di_{Lg}(t)}{dt} = \frac{-v_C - v_g}{L_g}. \tag{57}$$

As shown in Fig. 8(d), and based on predictive control theory, the FI current i_L at the next sampling time ($i_L[k+1]$) can be calculated from its current value ($i_L[k]$), using the ON-state and OFF-state slopes of mode-j ($j \in$ mode-I, II, III), that is,

$$i_L[k+1] = i_L[k] + \delta_{j,\mathrm{ON}} t_{\mathrm{ON}} + \delta_{j,\mathrm{OFF}}(1 - t_{\mathrm{ON}}) \tag{58}$$

where t_{ON} is the S_1 or S_2 ON-state dwell time.

The controller is intended to eliminate the error i_e between the reference FI current (i_L^*) and $i_L[k+1]$ [42], [43], [44], [45], which translates to

$$\begin{aligned} i_e = i_L^* - i_L[k+1] = 0 \Rightarrow i_L^* - i_L[k] \\ -\delta_{j,\mathrm{ON}}[d_j(t)]T_s - \delta_{j,\mathrm{OFF}}[1 - d_j(t)]T_s = 0. \end{aligned} \tag{59}$$

Then, t_{ON} and consequently, the optimal duty cycle can be obtained as follows:

$$d_j(t) = \frac{(i_L^* - i_L[k]) - \delta_{j,\mathrm{OFF}} T_s}{(\delta_{j,\mathrm{ON}} - \delta_{j,\mathrm{OFF}})T_s} \tag{60}$$

$$d_{\text{mode-I}}(t) = \frac{L(i_L^* - i_L[k]) + v_{\mathrm{out}} T_s}{V_{\mathrm{PV}} T_s} \tag{61}$$

$$d_{\text{mode-II}}(t) = \frac{L(i_L^* - i_L[k]) - (V_{\mathrm{PV}} - v_{\mathrm{out}})T_s}{v_{\mathrm{out}} T_s} \tag{62}$$

$$d_{\text{mode-III}}(t) = \frac{L(i_L^* - i_L[k]) - v_{\mathrm{out}} T_s}{(V_{\mathrm{PV}} - v_{\mathrm{out}})T_s}. \tag{63}$$

Similarly, in the NPR we have

$$d_{+\mathrm{NPR}}(t) = \frac{L_g(i_g^* - i_g[k]) - (v_C - v_g)T_s}{-v_C T_s} \tag{64}$$

$$d_{-\mathrm{NPR}}(t) = \frac{L_g(i_g^* - i_g[k]) + (v_C + v_g)T_s}{v_C T_s}. \tag{65}$$

Note that the average current through the inductor L in each mode is equal to the average current injected into the grid since the average current of C is zero in the steady state. Therefore,

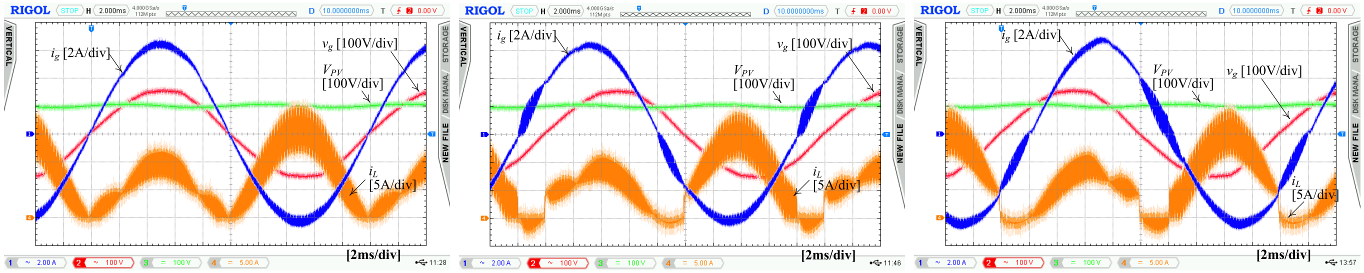


Fig. 10. Waveforms of $V_{\rm PV}$, v_g, i_g, and i_L for (a) $P_{\rm out} = 500$ W and $Q_{\rm out} = 0$ Var (PF = 1). (b) $P_{\rm out} = 400$ W and $Q_{\rm out} = 300$ Var (PF = 0.8 leading). (c) $P_{\rm out} = 400$ W, $Q_{\rm out} = 300$ Var (PF = 0.8 lagging).

TABLE IV
EXPERIMENTAL TEST CONDITIONS AND PARAMETERS

Parameters	Values
Rated power (P_{out}):	500 [W]
Switching frequency (f_s):	20 [kHz]
Grid side voltage (v_g):	110 [V] and 50 [Hz]
PV side voltage (V_{PV}):	100 [V] and 180 [V]
Inductors L and L_g:	1.0 [mH] and 0.4 [mH]
DC Capacitors C and C_{dc}:	2.2 [μF] and 1000 [μF]
MOSFET switches:	IPW60R017C7
Diode:	STTH30L06C
Microcontroller:	Piccolo TMS320F28035

one can readily conclude that

$$i_L^* = \begin{cases} |i_g^*|, & \text{Mode-I} \\ |i_g^*|\dfrac{|v_g|}{V_{\rm PV}}, & \text{Mode-II} \\ |i_g^*|\dfrac{V_{\rm PV} + |v_g|}{V_{\rm PV}}, & \text{Mode-III} \end{cases} \tag{66}$$

where i_g^* is the reference grid current.

VI. Experimental Verification

To confirm the proper operation of the proposed common-ground triple-mode FI PV inverter, a laboratory hardware prototype shown in Fig. 9 has been made. The specifications of the proposed converter and component parameters are presented in Table IV.

Fig. 10(a) illustrates the steady-state performance under unity power factor mode and with output power references of 500 W and 0 Var. It can be seen that the PV-side voltage is 100 V and the grid current is 4.54 A. Fig. 10(b) and (c) shows the steady-state operation under 0.8 leading and lagging power factor, respectively (or 400 W and ±300 Var). It is evident from Fig. 10 that the proposed TMCGFI inverter injects highly sinusoidal ac current with THD ≤5% even during the nonunity power factor operation and considering that the ac grid voltage is also slightly distorted.

The transient performance of the proposed FI converter and dead-beat control system from unity (500 W and 0 Var) to nonunity power factors (400 W and ±300 Var) has been investigated experimentally and the results are shown in Fig. 11. A fast and smooth transient response, from unity power factor to 0.8 lagging is confirmed in Fig. 11(a), and from unity power factor to 0.8 leading is shown in Fig. 11(b).

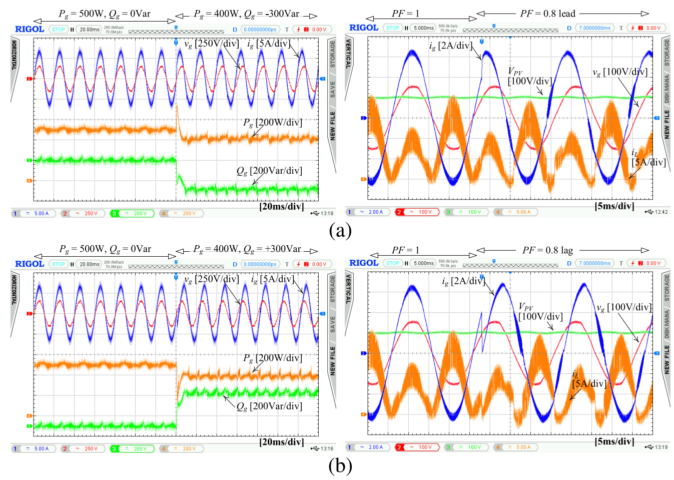


Fig. 11. Transient waveforms from unity to (a) 0.8 leading and (b) 0.8 lagging power factors.

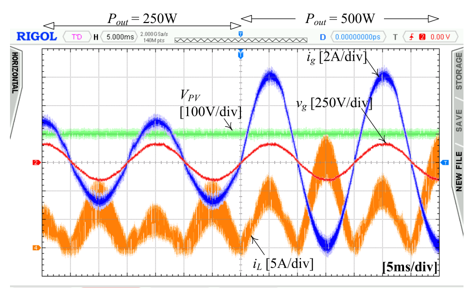


Fig. 12. Transient waveforms in response to power jump from 250 to 500 W grid-side power.

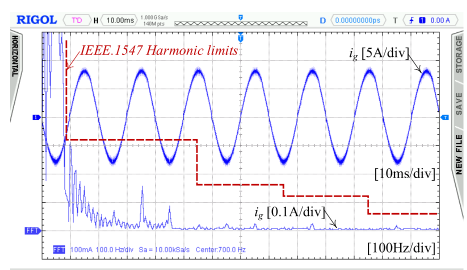


Fig. 13. Harmonic spectrum of the grid-side current at the rated power.

The transient response to a step change in the reference ac grid-side power is presented in Fig. 12. Clearly, a fast-dynamic current performance is achieved and this verifies that the IDBC, as already expected, offers a high dynamic performance in response to any changes.

The measured grid-side current harmonic spectrum under rated output power level is shown in Fig. 13. Clearly, the

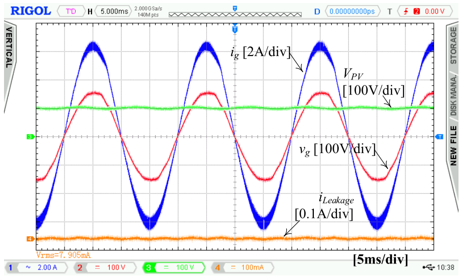
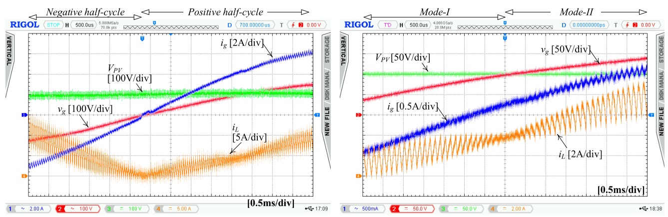


Fig. 14. Leakage current waveform.



(a) (b)

Fig. 15. Zoomed-in view of transient from (a) negative (mode-III) to positive (mode-I) half-cycle and (b) from mode-I to mode-II.

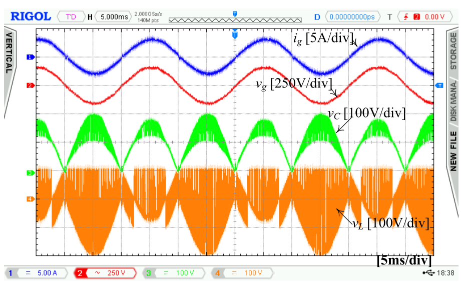


Fig. 16. Voltage waveforms of C and L.

grid current harmonic components are well below the IEEE 1547 limit.

Based on the approach used in [11] and [26], the measured leakage current waveform through the parasitic capacitors C_p and C_n of the PV side are shown in Fig. 14. As we expect, the leakage current of the proposed common-ground inverter is negligible (7 mA).

With a closer look at the ac-side current waveform, one can detect a very smooth mode transition from the negative to positive half-cycle or from mode-III to mode-I operation as shown in Fig. 15(a). Fig. 15(b) shows the zoomed-in view of the grid-side current and FI current following a transition from mode-I to mode-II. This ensures that the THD of the proposed converter current remains lower than 5% and, in fact, the THD of the injected grid-side current is 3.1%.

The voltage waveforms of capacitor C and the FI L have been depicted in Fig. 16. As already expected, the voltage across C is unipolar. Therefore, in this part of the circuit instead of an ac type, a dc-type capacitor can be used and hence, the physical volume and the cost of the proposed converter are further improved.

Fig. 17 illustrates the PV-side current under both unity and nonunity power factors.

The transient response to a step change in the grid voltage, transitioning from 110 to 220 V, under a constant current mode of 9.09 A, is depicted in Fig. 18. It is evident from the figure that the proposed converter demonstrates the capability

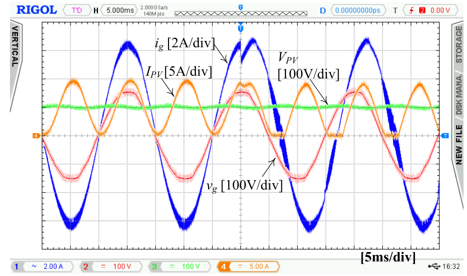


Fig. 17. Measured PV-side current ($I_{\rm PV}$) of the proposed converter.

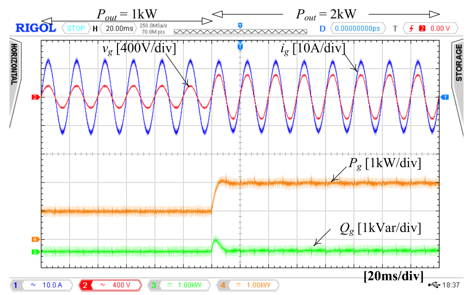


Fig. 18. Waveforms i_g, v_g, P_g, and Q_g for grid-side power ranging from 1 to 2 kW.

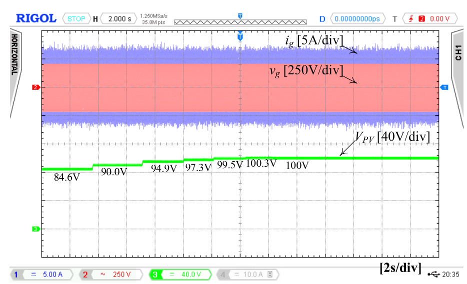


Fig. 19. Waveforms a real PV voltage, grid voltage, and injected current.

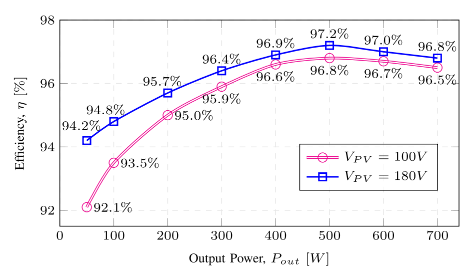


Fig. 20. Proposed FI converter efficiency curve versus output power levels.

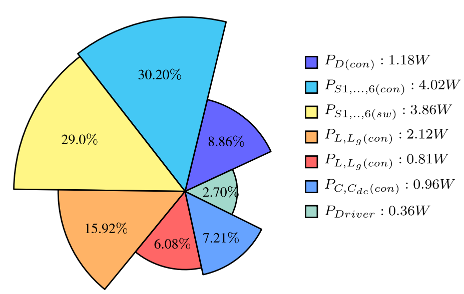


Fig. 21. Power loss break down of the proposed converter at $\eta_{\max}$.

to operate effectively under higher power levels, specifically at 1 and 2 kW. Furthermore, by adjusting the PV-side voltage from 84.6 to 100.3 V. Fig. 19 demonstrates the capability of the proposed inverter to function effectively with a real PV voltage profile.

TABLE V
EXPERIMENTAL TEST RESULTS

Test conditions:	THD:	$\Delta i_{g,max}$:	TVS:	TCS:
Unity PF, V_{PV}=100V	3.4%	0.33A	569.78V	34.41A
Unity PF, V_{PV}=180V	3.1%	0.33A	947.12V	28.17A
0.8 leading PF, V_{PV}=100V	4.62%	0.8A	582.02V	32.32A
0.8 leading PF, V_{PV}=180V	4.38%	0.8A	695.72V	27.95A
0.8 lagging PF, V_{PV}=100V	4.55%	0.7A	598.89V	32.79A
0.8 lagging PF, V_{PV}=180V	4.43%	0.7A	717.63V	27.66A

Measured peak efficiencies of 96.8% and 97.2% are achieved for the proposed converter when $V_{\text{PV}} = 100$ and 180 V, respectively, and these peak efficiencies occur at 500 W loading which can be seen from Fig. 20. The California Energy Commission (CEC) and European Union (EU) measured the efficiency of the proposed converter as 96.26% and 95.78%, respectively. The power loss breakdown of the proposed converter at the peak efficiency is presented in Fig. 21. As observed, the major portion of the power loss is attributed to the conduction loss of switches, indicating its significance in the overall power loss distribution.

A summary of the experimental results is presented in Table V. Under unity power factor conditions, the THD of i_g is measured at 3.4% and 3.1% for PV voltages of 100 and 180 V, respectively. For leading power factor conditions, the THD of the current with PV voltages of 100 and 180 V is illustrated, measuring at 4.62% and 4.38%, respectively. Similarly, under lagging power factor conditions, with PV voltages of 100 and 180 V, the THD values are recorded at 4.55% and 4.43%, respectively. Furthermore, Table V provides information on the maximum ripple of the grid current ($\Delta i_{g,\text{max}}$) during unity, leading, and lagging power factor conditions, measured at 0.33, 0.8, and 0.7 A, respectively. Table V shows the TVS and TCS ratings of the semiconductor devices used in the proposed converter. The maximum TVS and TCS ratings are recorded as 947.12 V and 34.41 A, respectively.

VII. CONCLUSION

In this article, the FI-based common-ground PV inverter with the capability of supporting reactive power provision to the ac grid is presented. This converter also has the benefits of using a low number of semiconductor devices with no ac type capacitor. The proposed converter does not require an ac capacitor and has a relatively small grid filter inductor, resulting in a relatively small volume. Switching losses are reduced by adopting the triple-mode time-sharing technique. The proposed converter has utilized the combination of both indirect and direct dead-beat current controllers during positive and NPR, respectively, which ensures accurate and fast control of the grid-side current. Active and reactive power regulation and different transient and steady-state responses have been successfully demonstrated using the developed prototype. The prototype converter has a maximum efficiency of 97.2% and 96.8% at $V_{\text{dc}} = 180$ and 100 V, $V_{\text{rms}} = 110$ V, $P_{\text{out}} = 500$ W, and $f_s = 20$ kHz. The measured waveforms from the prototype have validated the theoretical analysis and confirmed the superior operation of the proposed converter.

REFERENCES

[1] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces*, Standard 1547-2018, Inst. Electr. Electron. Engineers Standards, 2018, p. 2018.

[2] R. Mallwitz, "Circuit apparatus for transformerless conversion of an electric direct voltage into an alternating voltage," U.S. Patent 7 616 467 B2, Nov. 7, 2009.

[3] R. Ayyanar, "Circuits and methods for photovoltaic inverters," U.S. Patent 9 413 269 B2, Aug. 2, 2016.

[4] Y. Xia, J. Roy, and R. Ayyanar, "A single stage common ground three-level PV inverter with integrated power decoupling," *IEEE Open J. Power Electron.*, vol. 1, pp. 227–237, 2020.

[5] Z. Yao, Y. Zhang, and X. Hu, "Transformerless grid-connected PV inverter without common mode leakage current and shoot-through problems," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3257–3261, Dec. 2020.

[6] Z. Yao and Y. Zhang, "A doubly grounded transformerless PV grid-connected inverter without shoot-through problem," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6905–6916, Aug. 2021.

[7] Z. Yao and Z. Wang, "Single-stage doubly grounded transformerless PV grid-connected inverter with boost function," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2237–2249, Feb. 2022.

[8] A. Sarikhani, M. M. Takantape, and M. Hamzeh, "A transformerless common-ground three-switch single-phase inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8902–8909, Sep. 2020.

[9] A. Kumar and P. Sensarma, "New switching strategy for single-mode operation of a single-stage buck–boost inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5927–5936, Jul. 2018.

[10] J. Jiang, S. Pan, J. Gong, F. Liu, X. Zha, and Y. Zhuang, "A leakage current eliminated and power oscillation suppressed single-phase single-stage nonisolated photovoltaic grid-tied inverter and its improved control strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6738–6749, Jun. 2021, doi: 10.1109/TPEL.2020.3035033.

[11] H. Heydari-doostabad, M. Pourmahdi, M. Jafarian, A. Keane, and T. O'Donnell, "Three-switch common ground step-down and step-up single-stage grid-connected PV inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7577–7589, Jul. 2022.

[12] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403–5415, Jul. 2017.

[13] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018.

[14] X. Xu, M. Su, Y. Sun, B. Guo, H. Wang, and G. Xu, "Four-switch single-phase common-ground PV inverter with active power decoupling," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 3223–3228, Mar. 2022.

[15] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. Hoboken, NJ, USA: Wiley, 2011.

[16] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single-phase transformerless grid-connected inverter with boosting ability and common ground feature," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9313–9325, Nov. 2020.

[17] R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, Y. P. Siwakoti, and J. Pou, "Nine-level nine-switch common-ground switched-capacitor inverter suitable for high-frequency AC-microgrid applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6132–6143, May 2022.

[18] M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, S. S. Lee, D. D. Lu, and Y. P. Siwakoti, "A single-source single-stage switched-boost multilevel inverter: Operation, topological extensions, and experimental validation," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11258–11271, Sep. 2022.

[19] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, "Common-ground grid-connected five-level transformerless inverter with integrated dynamic voltage boosting feature," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6661–6672, Dec. 2022.

[20] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo, and F. Blaabjerg, "A novel Common-ground-type nine-level dynamic boost inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 4435–4442, Aug. 2022.

[21] D. Karschny, "Inverter," German Patent 1 964 522 C1, Apr. 5, 1998.

[22] H. Patel and V. Agarwal, “A single-stage single-phase transformer-less doubly grounded grid-connected PV interface,” *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.

[23] P. J. Grbovic, F. Gruson, N. Idir, and P. L. Moigne, “Turn-on performance of reverse blocking IGBT (RB IGBT) and optimization using advanced gate driver,” *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 970–980, Apr. 2010.

[24] M. Tofigh Azary, M. Sabahi, and E. Babaei, “Single-phase common mode transformer-less soft-switching grid-connected inverter with eliminated leakage current,” *Int. J. Circuit Theory Appl.*, vol. 47, no. 6, pp. 838–861, Jun. 2019.

[25] N. Gao et al., “MOSFET-switch-based transformerless single-phase grid-tied inverter for PV systems,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 3830–3839, Aug. 2022.

[26] M. T. Azary, M. Sabahi, E. Babaei, and F. A. A. Meinagh, “Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221–231, Jan. 2018.

[27] N. Vosoughi Kurdkandi, O. Husev, O. Matiushkin, D. Vinnikov, Y. P. Siwakoti, and S. S. Lee, “Novel family of flying inductor-based single-stage buck–boost inverters,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 6020–6032, Oct. 2022.

[28] H. Tian, W. Han, M. Chen, G. Liang, and Z. Tang, “Common-ground-type inverter with dynamic boosting and reactive compensation for grid,” *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6017–6027, May 2024.

[29] S. Kumari, N. Sandeep, A. Verma, U. R. Yaragatti, and H. Pota, “Design and implementation of transformer-less common-ground inverter with reduced components,” *IEEE Trans. Ind. Appl.*, early access, Apr. 7, 2022.

[30] A. Jakhar, N. Sandeep, and A. K. Verma, “Common-ground-type quadruple boosting nine-level inverter,” *IEEE J. Emerg. Sel. Topics Ind. Electron.*, early access, Feb. 27, 2024.

[31] D. Singh and N. Sandeep, “A novel common-ground multi-source inverter,” *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15142–15146, Dec. 2023.

[32] A. Srivastava and J. Seshadrinath, “A novel single phase three level triple boost CG switched-capacitor based grid-connected transformerless PV inverter,” *IEEE Trans. Ind. Appl.*, vol. 59, no. 2, pp. 2491–2501, Mar. 2023.

[33] L. Wang and M. Shan, “A novel single-stage common-ground zeta-based inverter with nonelectrolytic capacitor,” *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11319–11331, Sep. 2022.

[34] W. Chen, X. Yang, W. Zhang, and X. Song, “Leakage current calculation for PV inverter system based on a parasitic capacitor model,” *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8205–8217, Dec. 2016.

[35] G. d. O. Assunç ao and I. Barbi, “Method for deriving transformerless common-ground voltage source inverter topologies,” *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10821–10832, Sep. 2022.

[36] Y. Xia, J. Roy, and R. Ayyanar, “A capacitance-minimized, doubly grounded transformer less photovoltaic inverter with inherent active-power decoupling,” *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5188–5201, Jul. 2017.

[37] P. K. Chamarthi, M. S. E. Moursi, V. Khadkikar, K. H. A. Hosani, A. Al-Durra, and T. H. M. EL-Fouly, “A single stage doubly grounded transformerless inverter topology with buck-boost voltage capability for grid connected PV systems,” *IEEE Trans. Power Del.*, vol. 37, no. 6, pp. 5044–5058, Dec. 2022.

[38] H. Heydari-doostabad, S. H. Hosseini, R. Ghazi, and T. O’Donnell, “Pseudo DC-link EV home charger with a high semiconductor device utilization factor,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2459–2469, Mar. 2022.

[39] H. Heydari-doostabad and T. O’Donnell, “A wide-range high-voltage-gain bidirectional DC–DC converter for V2G and G2 V hybrid EV charger,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4718–4729, May 2022.

[40] H. Heydari-doostabad and M. Monfared, “An integrated interleaved dual-mode time-sharing inverter for single-phase grid-tied applications,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 286–296, Jan. 2019.

[41] S. H. Hosseini, R. Ghazi, and H. Heydari-doostabad, “An extendable quadratic bidirectional DC–DC converter for V2G and G2 V applications,” *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4859–4869, Jun. 2021.

[42] M. R. Aalami, M. Zarif, M. Alishahi, A. A. Shojaei, and H. H. Doostabad, “Flying-inductor-cell based inverters for single-phase transformerless PV applications,” *IET Power Electron.*, vol. 16, no. 1, pp. 75–91, Jan. 2023.

[43] M. Pourmahdi, H. Heydari-doostabad, R. Ghazi, and T. O’Donnell, “Buck–boost common ground bridgeless PFC (CGBPFC) rectifies with positive/negative output,” *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1272–1282, Feb. 2022.

[44] M. A. Abbaszadeh, M. Monfared, and H. Heydari-doostabad, “High buck in buck and high boost in boost dual-mode inverter (Hb2DMI),” *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4838–4847, Jun. 2021.

[45] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, “Single-phase dual-mode interleaved multilevel inverter for PV applications,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2905–2915, Apr. 2020.

Hamed Heydari-doostabad (Senior Member, IEEE) received the Ph.D. degree (Hons.) in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2018.

He is currently an Assistant Professor at the School of Electrical and Electronic Engineering, University College Dublin (UCD), Dublin, Ireland. His research interests include power electronics, especially power converters, renewable energy systems, and control systems.

Maryam Pourmahdi received the B.Sc. and M.Sc. (Hons.) degrees in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2018 and 2021, respectively. She is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, University College Dublin (UCD), Dublin, Ireland.

Her research interests include power electronics, especially PFC rectifiers, inverters, dc converters, control systems, and power quality.

Mohammad Monfared (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2004, and the M.Sc. and Ph.D. degrees (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2006 and 2010, respectively.

In 2022, he joined the Faculty of Science and Engineering, Swansea University, Swansea, U.K. His research interests include power electronics, renewable energy systems, and energy management.

Dr. Monfared is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS.

Terence O’Donnell (Senior Member, IEEE) received the B.E. and Ph.D. degrees in electrical engineering from University College Dublin (UCD), Dublin, Ireland, in 1990 and 1996, respectively.

He is currently an Associate Professor with the School of Electrical and Electronic Engineering, UCD. He is a Principal Investigator with UCD Energy Institute, Dublin, where his research interests are focused on the use of power electronics converters in power systems and, in particular, on the interfacing of power electronics to the grid. Specific interests include the grid applications of solid-state transformers, the control of converters for distributed energy resources, and the use of power hardware in the loop testing methods.