A New Hardware Architecture for SVPWM Technique Based on the Taylor Decomposition

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***Abstract*— A novel hardware digital architecture for the space vector pulsewidth modulation (SVPWM) technique is proposed and based on a novel algorithm for the evaluation of the dwell times. Indeed, the complexity of the calculation of trigonometric functions is solved by introducing a Taylor series decomposition and using a convenient definition of the space vector $\alpha - \beta$ plane. Our architecture can modify the dwell times as a function of the fundamental and switching frequencies, of the phase and of the modulation index. Compared to other techniques, it avoids the use of external reference voltages as well as of the precalculated dwell times, like for the LUT-based architectures. Although it can be implemented in several logic devices, an Altera Cyclone V field programmable gate array (FPGA) is used as a digital controller of a three-phase power inverters and its resources are 16% and 2%, respectively, of the look-up tables and of the flip flops. Several cases are studied in order to show the goodness of the output waveforms during the real-time variations of the inputs.**

***Index Terms*— Digital design, field programmable gate array (FPGA), space vector pulsewidth modulation (SVPWN), three-phase dc/ac power converter.**

I. Introduction

THE recent increase in air pollution is leading the international academic and industrial research studies to improve the power electronics systems in terms of energy efficiency and power density. Several fields of applications can find interest from transportation [1], [2] to distributed generation [3]. Although the new semiconductor technologies, like the wide bandgap semiconductor devices in Silicon Carbide [4], [5], [6] and in Gallium Nitride [7], [8], can help to achieve such goal, thanks to higher switching frequencies, power density, and efficiency than Silicon one, an increase of the complexity of the electronics power systems is also required. Indeed, in addition to the management of the energy conversion, the controllers of the modern power converters supervise the auxiliary and communication circuits or the activities of the single stages in the multistage converters [9]. This complexity can be taken on with digital controllers for their flexibility and computation capabilities [10], like digital signal processor (DSP), [11], micro controller [12], or field programmable gate array (FPGA), [13]. Lately, FPGA controllers are excellent candidates to implement digital controllers due to their possibility to compute real-time operation in less execution time [14], [15], [16].

In this scenario, the performance of the system is also related to the control strategy and, in particular, for three-phase dc/ac power converters of Fig. 1(a), the space vector pulsewidth modulation (SVPWM), technique has a lower harmonic content and a higher dc bus utilization than other control techniques [17], but has a higher computational cost. Indeed, the calculation of trigonometrical function makes impracticable its implementation with analog circuits [18]. However, there are several effort to implement SVPWM technique in FPGA controllers in order to simplify and to reduce the complexity of the algorithm, and there are solutions based on coordinate rotation digital computer (CORDIC), algorithms [19] or on Lookup table approaches [20], [21] and that can use DSPs [22] or external flash memory with an external signal reference [23]. However, there are some drawbacks: first, in the case of the external PCs or DSPs, one needs powerful hardware that limits the fields of applications, like stand-alone applications because SVPMW signal generator requires external reference signals; second, although hardware architectures based on LUT reduce the complexity and do not require external resources, the variations of the three-phase output waveform are only possible for multiple values of the reference value [20], [21], [24]. Moreover, FPGA manufacturers provide FPGA core Intellectual Property modules to implement SVPWM technique, but they cannot be modified in order to optimize the resource for specific applications as well as to improve the algorithm.

In this article, we propose a novel hardware architecture as well as a novel algorithm of the SVPWM technique. They are based on a linearization of the trigonometric functions through the Taylor series decomposition and on an optimized construction of the space vector in the $\alpha - \beta$ plane. The architecture has been implemented in an Altera Cyclone V and in an Xilinx Artix 7 FPGAs, where a fixed-point customized arithmetic logic unit (ALU), executes the calculations for the dwell times at each switching period with only multipliers, adders, and divisors and without DSP or external reference voltage. Indeed, we discretize the circumference of the space

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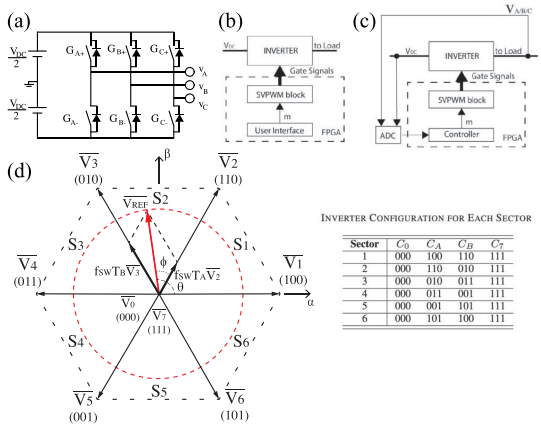

Fig. 1. (a) Three-phase power converter basic schematic. SVPWM block in (b) open-loop and (c) closed-loop configurations. (d) Polar plane and vector representation of the three-phase voltages based on the SVPWM technique, where the round brackets are the configurations of top transistor of (a).

vector so that its rotation can be described through an integer number, easily implemented with an internal counter. Furthermore, the values of the fundamental, f_C, and switching, f_{SW}, frequencies, of the modulation index, m_a, and of the phase can be changed without external reference signals and it is also possible to introduce a phase shift of the three-phase waveform as well as a variation of the rotation direction of the rotor, when the power converter drives an asynchronous motor. The possibility to change in real-time the three-phase output voltage parameters is useful both in an open-loop architecture, similar to Fig. 1(b), and in a closed-loop configuration, like in Fig. 1(c) where the controller evaluates m_a and sends it to the input of our SVPWM block to generate the gate driver signals. The article is organized as follows: in Section II the theory of the proposed algorithm is reported; in Section III its implementation in a hardware architecture based on an open-loop control scheme of Fig. 1(b); in Section IV the experimental results obtained from a three-phase power converter; finally, Section V the conclusions.

II. Theory of the Proposed SVPWM

SVPWM technique controls the configurations and the turn-on and -off timings of the transistors for a three-phase power converter dc/ac of Fig. 1(a). The aim is to generate a three-phase sinusoidal output voltage with f_C and amplitude, V_M, which is related to the input dc voltage, V_{dc}, through $m_a = 2V_M/V_{dc}$. f_{SW} depends on the power transistor characteristics as well as on the f_C. The three-phase output voltages referred to neutral potential are as follows:

$$\begin{cases} v_A = V_M \sin(2\pi f_C) \\ v_B = V_M \sin\left(2\pi f_C + \dfrac{2\pi}{3}\right) \\ v_C = V_M \sin\left(2\pi f_C - \dfrac{2\pi}{3}\right) \end{cases} \tag{1}$$

and can be represented on the polar plane of Fig. 1(d) in terms of the vectors $\overline{V_\alpha}$ and $\overline{V_\beta}$ through the following Clarke transformation [25]:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \dfrac{2}{3} & -\dfrac{1}{3} & -\dfrac{1}{3} \\ 0 & \dfrac{\sqrt{3}}{3} & -\dfrac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}. \tag{2}$$

The vector form of (2) is expressed in terms of the voltage reference vector, $\overline{V_{REF}}$, whose amplitude, V_{REF}, and angle referred to the α-axis, θ, are

$$\begin{cases} V_{REF} = \sqrt{V_\alpha^2 + V_\beta^2} \\ \theta = \arctan(V_\beta / V_\alpha). \end{cases} \tag{3}$$

The circle described by $\overline{V_{REF}}$ is descretized in step angles of $\Delta\theta = 2\pi f_C/f_{SW}$ and its rotation speed and radius are, respectively, related to f_C and V_M of (1).

The vector representation on the polar plane is useful for the evaluation of the inverter configurations and for the calculation of the dwell times, T_A, T_B, and T_0, when the power converter of Fig. 1(a) generates the three-phase output voltages of (1). Indeed, observing Fig. 1(d) the polar plane is divided into six sectors, S_i, by six active vectors, $\overline{V_i}$, which represent the eight different configurations of the inverter together with the two null vectors (i.e., $\overline{V_0}$ and $\overline{V_7}$). It is worth to note that the digits in the round bracket of Fig. 1(d) are the state condition of the top gate signals of Fig. 1(a), for example $\overline{V_6} = (101)$ means that G_{A+} and G_{C+} are high and G_{B+} is low, whereas the bottom gate signals are inverted, i.e., $(G_{A-}, G_{B-}, G_{C-}) \equiv (010)$. To describe the rotation of $\overline{V_{REF}}$ and, hence, to modulate the three-phase output voltage with the power converter, the $\overline{V_{REF}}$ is projected along the two vectors $\overline{V_i}$ and $\overline{V_{i+1}}$ when it is in S_i and the single switching period, T_{SW}, is lower than the fundamental period, T_C, i.e., $f_{SW} \gg f_C$, one obtains at jth time-step

$$V_{REF} = f_{SW}\left[\frac{T_0(j)}{2}V_0 + \frac{T_0(j)}{2}V_7 + T_A(j)V_i + \right. \\ \left. + T_B(j)V_{i+1}\right] \tag{4}$$

where the dwell-time T_0 is equally divided between $\overline{V_0}$ and $\overline{V_7}$. Assuming that for each switching interval, θ and V_{REF} are constant and that each S_i covers $\pi/3$ of the circle, the dwell times can be calculated using the trigonometric projections along $\overline{V_i}$ and $\overline{V_{i+1}}$, as follows [26]:

$$T_A(j) = \frac{m_a\sqrt{3}}{2f_{SW}} \sin\left[S_i\frac{\pi}{3} - \theta(j)\right] \tag{5a}$$

$$T_B(j) = \frac{m_a\sqrt{3}}{2f_{SW}} \sin\left[\theta(j)\text{-}(S_i - 1)\frac{\pi}{3}\right] \tag{5b}$$

$$T_0(j) = T_{SW} - T_A(j) - T_B(j) \tag{5c}$$

where S_i is the ith sector and its value is from 1 to 6.

A. Proposed SVPWM Algorithm

The dwell times of (5) can be rewritten applying the following assumptions.

1) A new angle is introduced ϕ, which is $[\theta - (S_i - 1)\pi/3]$ and has the same $\Delta\phi = \Delta\theta = 2\pi f_C/f_{SW}$. In this way, S_i is avoided in new (5).

TABLE I
COEFFICIENTS OF (7)

Coefficient	K	a_1	a_2	a_3	a_4
Value	$\frac{m_a f_{CLK}}{f_{SW}^2}$	$0.75 f_{SW}$	$2.72 f_C$	$\frac{14.8 f_C^2}{f_{SW}}$	$\frac{17.9 f_C^3}{f_{SW}^2}$

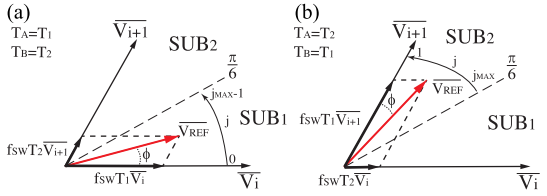

Fig. 2. Graphic representation of the proposed SVPWM algorithm for (a) $\overline{V_{REF}} \in \text{SUB}_1$ and (b) $\overline{V_{REF}} \in \text{SUB}_2$.

2) T_A and T_B values are symmetric respect to $\phi = \pi/6$ in each S_i. Resources are reduced being by reducing the number of bits of each variable.
3) The angle ϕ can be expressed as $\Delta\phi \cdot j$, where j is an integer from 0 to $j_{MAX} = f_{SW}/(12 f_C)$.
4) S_i defines the inverter configuration.
5) T_A, T_B, and T_0 are multiplied by f_{CLK} for the counting.

Hence, (5a) and (5b) can be discretized as follows:

$$T_1(j) = \frac{m_a\sqrt{3}}{2 f_{SW}} \sin\left(\frac{\pi}{3} - j\Delta\phi\right) f_{CLK} \tag{6a}$$

$$T_2(j) = \frac{m_a\sqrt{3}}{2 f_{SW}} \sin\left(j\Delta\phi\right) f_{CLK} \tag{6b}$$

and, applying the Taylor series up to the third order, we obtain

$$T_1(j) = K\left[(a_1 - a_3 j^2) - (a_2 - a_4 j^2) j\right] \tag{7a}$$

$$T_2(j) = K\left[2(a_2 - a_4 j^2) j\right] \tag{7b}$$

$$T_0(j) = f_{CLK} T_{SW} - T_1(j) - T_2(j) \tag{7c}$$

where the coefficients are reported in Table I. The expansion up to third order is due to the narrow domain of the variable $j \in [0; j_{MAX}]$, i.e., $\phi \in [0; \pi/6]$. From (7) the dwell times can be calculated by changing only the integer number j, which is implemented with a digital counter, and maintain their dependencies on f_{SW}, f_C, and m_a. Once (7) are calculated, T_1 and T_2 are related to the effective dwell-times T_A and T_B of Fig. 1(d), as follows.

1) $j = 0 \rightarrow j_{MAX} - 1$, i.e., $\overline{V_{REF}} \in \text{SUB}_1$, [see Fig. 2(a)]

$$\begin{cases} T_A(j) = T_1(j) \\ T_B(j) = T_2(j) \end{cases} \tag{8}$$

equivalently.
a) $\phi = 0 \rightarrow \pi/6 - \Delta\phi$.
b) $\theta = (S_i - 1)\pi/3 \rightarrow \pi/6 + (S_i - 1)\pi/3 - \Delta\theta$.

2) $j = j_{MAX} \rightarrow 1$, i.e., $\overline{V_{REF}} \in \text{SUB}_2$, [see Fig. 2(b)]

$$\begin{cases} T_A(j) = T_2(j) \\ T_B(j) = T_1(j) \end{cases} \tag{9}$$

equivalently.
a) $\phi = \pi/6 \rightarrow \Delta\phi$.
b) $\theta = \pi/6 + (S_i - 1)\pi/3 \rightarrow \pi/3 + (S_i - 1)\pi/3 - \Delta\theta$.

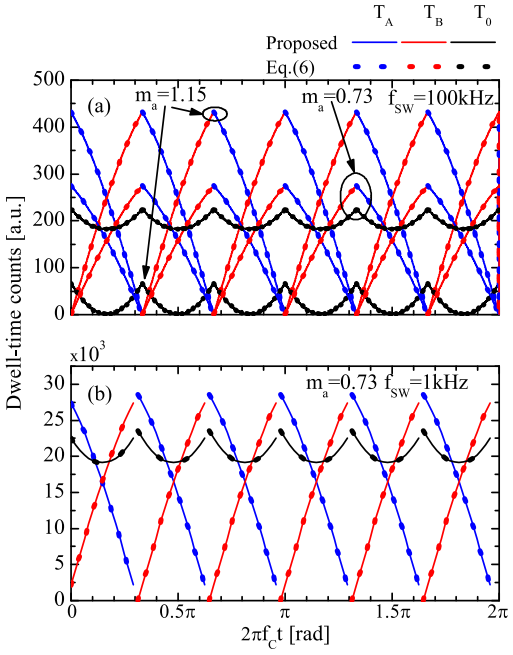

Fig. 3. Comparisons of the dwell-time counts for a $f_{CLK} = 50$ MHz calculated through (5) and the proposed algorithm. (a) $f_{SW} = 100$ kHz, $m_a = 0.73$ and 1.15 and (b) $f_{SW} = 1$ kHz, $m_a = 0.73$. Continuous lines are from the proposed model, dashed lines are from (6).

The SUB_1 of (8) is the subsector defined for $\phi \in [0; \pi/6)$ and the SUB_2 of (9) the subsector defined for $\phi \in [\pi/6; \pi/3)$. In Fig. 3 the comparisons between the effective dwell-times evaluated from (5) and the proposed algorithm are reported for different f_{SW} and m_a values and for a $f_{CLK} = 50$ MHz. In particular, Fig. 3(a) shows the effect of the m_a, when it changes from 0.73 to 1.15, whereas Fig. 3(b) shows the variation of f_{SW} from 100 to 1 kHz, whose clock counts is higher. In both cases, the theoretical and the proposed SVPWM dwell-time calculations give the same results.

III. HARDWARE ARCHITECTURE

In this section the proposed hardware architecture implements the SVPWM algorithm of Section II-A: it calculates the effective dwell-times through (7)–(9), manages the counters and the inverter configurations, and generates the six signals for the gate drivers of the power transistors. Our architecture is generic and can be implemented in any digital controller and, as an example, in Section IV we report an example of FPGA application. The block diagram of the proposed architecture is shown in Fig. 4(a) and is based by three macro blocks: COUNTING, TIME CALCULATOR and INVERTER CONFIGURATOR. The five inputs are f_C, f_{SW}, m_a, and θ^*, which are related to the three-phase output voltage and can be changed in real-time for each T_{SW}, and CNT_θ, which is the input signal for the phase function (see Section III-A). Its outputs are the six signals for the gate drivers. The description of the control signals and the main procedure is reported in the flux diagram of Fig. 5.

A. Phase Input Function

In several applications, for example in field-oriented-control technique, the controller needs to instantaneously change θ

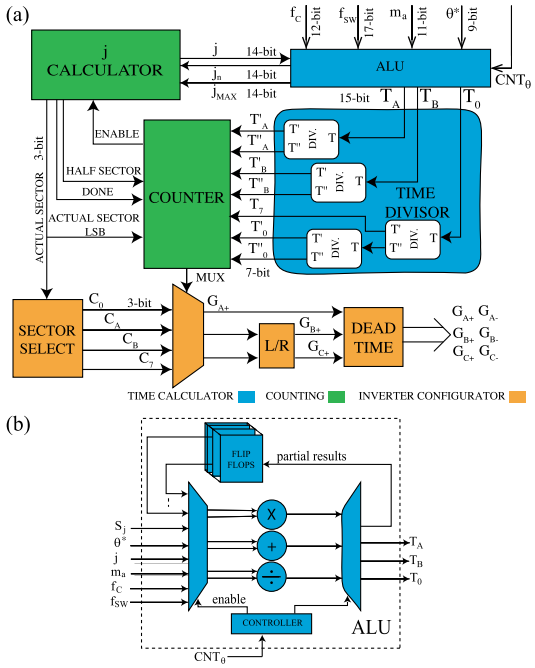

Fig. 4. Functional block diagram of (a) proposed architecture and (b) ALU.

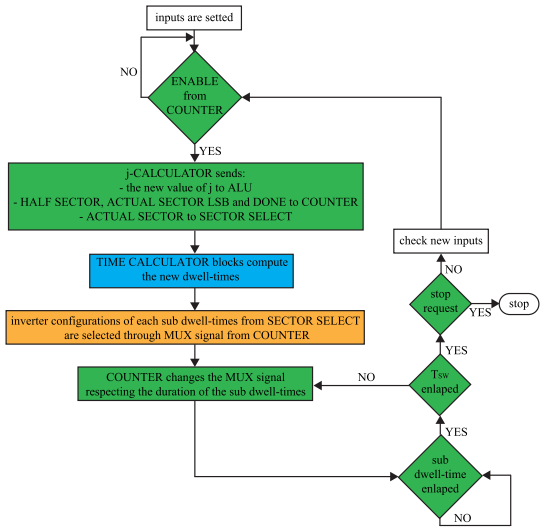

Fig. 5. Flux diagram of the main process steps of the proposed architecture. The colors are related to those of Fig. 4(a).

and, in our architecture, we can do it through the inputs θ^* and CNT_θ. The one-bit control signal, CNT_θ, defines if the value of θ^* refers to the position of the $\overline{V_{\mathrm{REF}}}$ in the $\alpha-\beta$ plane, i.e., position function and $\theta^* = \theta_{\mathrm{new}}$, or refers to the shift respect the actual angle, i.e., Shift function and $\theta^* = \theta_{\mathrm{delay}}$, which is delay respect to the actual phase. In terms of the HW architecture, the difference between the two phase variations is related to the updating of the counter j.

1) Position Function: When the angle changes, i.e., $\theta^* = \theta_{\mathrm{new}}$, we can calculate the related sector, S^*, and the related counter index, $j_{\theta*}$, as follows:

$$S^* = \mathrm{int}\left(\frac{\theta^*}{60}\right) + 1 \tag{10a}$$

$$j_{\theta*} = \mathrm{int}\left(\frac{\theta^*}{\Delta\theta}\right) - 2j_{\mathrm{MAX}}(S^* - 1). \tag{10b}$$

2) Shift Function: When a delay is desired, i.e., $\theta^* = \theta_{\mathrm{delay}}$, first, we evaluate the relative number of counts.

1) $\overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_1$

$$j^* = j + 2j_{\mathrm{MAX}}(S_j - 1) + \mathrm{int}(\theta^*/\Delta\theta). \tag{11}$$

2) $\overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_2$

$$\begin{aligned} j^* &= 2j_{\mathrm{MAX}} - j + 2j_{\mathrm{MAX}}(S_j - 1) + \mathrm{int}(\theta^*/\Delta\theta) \\ &= 2j_{\mathrm{MAX}}S_j - j + \mathrm{int}(\theta^*/\Delta\theta) \end{aligned} \tag{12}$$

and, then, S^* and $j_{\theta*}$ are as follows:

$$S^* = \mathrm{int}\left(\frac{j^*}{2j_{\mathrm{MAX}}}\right) + 1 \tag{13a}$$

$$j_{\theta*} = j^* - 2j_{\mathrm{MAX}}(S^* - 1). \tag{13b}$$

Once S^* is evaluated from (10a) or (13a), the new sector, S_θ, is calculated with the following relation:

$$S_\theta = \begin{cases} S^*, & S^* \le 6 \\ S^* - 6\ \mathrm{int}\left(\dfrac{S^*}{6}\right), & S^* > 6 \end{cases} \tag{14}$$

instead, starting from (10b) or (13b), we obtain the new counter index, j, as follows:

$$j_{\theta*} < j_{\mathrm{MAX}}: \begin{cases} j = j_{\theta*} \\ \overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_1 \\ \mathrm{COUNTER} = +1 \end{cases} \tag{15}$$

$$j_{\theta*} \ge j_{\mathrm{MAX}}: \begin{cases} j = 2j_{\mathrm{MAX}} - j_{\theta*} \\ \overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_2 \\ \mathrm{COUNTER} = -1. \end{cases} \tag{16}$$

B. COUNTING Macro-Block

The COUNTING macro-block synchronizes the entire system and is composed of two finite state machines, j-CALCULATOR and COUNTER, which communicate with ENABLE, DONE, HALF SECTOR signals and the least significative bit of the ACTUAL SECTOR signal.

1) j-CALCULATOR Block: As shown in Fig. 4(a), j-CALCULATOR block has three input signals and four output signals, and its task is the setting-up of the j variable. Indeed, when the COUNTER block sends the ENABLE signal, one of the following cases can occur.

1) $\phi \le (\pi/6)$: the value of j increases by 1 and HALF SECTOR is set to 0, i.e., $\overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_1$.
2) $(\pi/6) < \phi \le (\pi/3)$: the value of j decreases by 1 and HALF SECTOR is set to 1, i.e., $\overline{V_{\mathrm{REF}}} \in \mathrm{SUB}_2$.
3) $\phi = (\pi/3)$: ACTUAL SECTOR increases by 1 and, if ACTUAL SECTOR $= 6$, it carries to 0, i.e., a complete round of the $\alpha-\beta$ plane is done.
4) f_C or f_{SW} change: the values of j_{MAX} and j are updated through j_{MAX} and j_n signals from ALU block.

Once the new value of j is sent to ALU block, j-CALCULATOR sends the DONE signal.

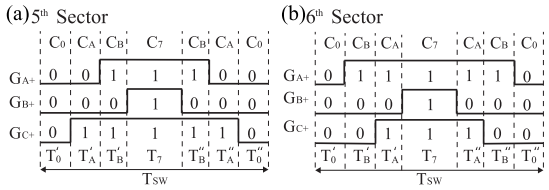

Fig. 6. Gate signals sequence for a single T_{SW} for (a) odd and (b) even sectors.

2) COUNTER Block: It has two output and ten input signals, whose seven are the sub dwell-times used in a single T_{SW}. These last are obtained from the TIME DIVISOR block, as explained in Section III-C. This block controls the multiplexer with the MUX signal: indeed, it selects the configuration of the top transistors for each sub-interval [21]. Fig. 6(a) and (b) report the temporal sequences of the gate signals for 5th and sixth sectors, respectively, for a single T_{SW} and there are also shown the sequences of the sub-interval times for odd and even S_i.

C. TIME CALCULATOR Macro-Block

The TIME CALCULATOR macro-block is composed by two blocks and its aim is the algebraic calculation of the dwell-times. The ALU block is a custom made fixed point 32-bit ALU and implements (7), whereas the TIME DIVISOR block performs the division of the dwell-times in the seven sub-intervals for the COUNTER block.

1) ALU Block: The internal structure of the ALU block is shown in Fig. 4(b), whose three output signals are the dwell-times evaluate from (7). A finite state machine CONTROLLER manages the sequence of operations by carrying out the multiplication, the division, and the addition through the multiplexer and by redirecting the relative results to the flip-flops and to the outputs. The aim of the flip-flops is to store the results of each 25 sequential steps, which are shown in Table II. Two different sequences are defined by the CONTROLLER through the signal CNT_θ and they are the sequence refers to position and that to shift of the Phase input functions (see Section III-A). It is worth to note that the new values j_θ and S_θ are calculated only when a new value of θ is given. Moreover, our architecture performs an update of the defined f_{SW} in order to have an integer number of the $\Delta\theta$, which, equivalently, means an integer value of j_{MAX}. This last is done between steps 1 and 4 of Table II, where the new switching frequency, f_{SWn}, is calculated as follows:

$$f_{SWn} = 12\ j_{MAX} f_C = 12\ \text{int}\left(\frac{f_{SW}}{12 f_C}\right) f_C. \tag{17}$$

Finally, when one or both of f_{SW} and of f_C change their values, a scaling of the j must be done (see steps 11–12 and 24–25 of Table II), otherwise a discontinuity of the waveform is shown. Indeed, the ALU keeps the proportionality between the new and the old values of j and of j_{MAX} as follows:

$$j_n = j \frac{f_{SWn}}{f_{SW,\text{old}}} \frac{f_{C,\text{old}}}{f_C} = j\, n_{SW} n_C. \tag{18}$$

It is worth to note that, since the sequences of Table II are in the last 25 clock periods, T_{CLK}, and the input signals vary in this interval time, the dwell-times variation has a maximum delay of $25T_{CLK} + T_{SW}$.

2) TIME DIVISOR Block: This block divides the three dwell-times in the seven subintervals of the COUNTER block (see Fig. 6) as follows [20]:

$$T' = \begin{cases} \dfrac{T}{2}, & \text{if } T \text{ is even} \\ \dfrac{T-1}{2}, & \text{otherwise} \end{cases} \tag{19a}$$

$$T'' = \begin{cases} \dfrac{T}{2}, & \text{if } T \text{ is even} \\ \dfrac{T+1}{2}, & \text{otherwise.} \end{cases} \tag{19b}$$

In Fig. 4(a) the DIV. sub-block, which performs (19), and the internal wiring of the TIME DIVISOR block are shown. It is worth noting that the division by 2 are carried out by a one bit right shift.

D. INVERTER CONFIGURATOR Macro-Block

The INVERTER CONFIGURATOR macroblock generates the six gate driver signals and it is composed by a SECTOR SELECT with a MULTIPLEXER and by the DEAD TIME and L/R blocks.

1) SECTOR SELECT and MULTIPLEXER Blocks: The SECTOR SELECT block is an LUT and contains the configurations of the inverter related to each sector, as reported in table of Fig. 1(d). Its input is the ACTUAL SECTOR signal from the j-CALCULATOR and selects the four configurations, C_i, of the desired single sector. The four 3-bits outputs go to the MULTIPLEXER, which routes one of them to the output through MUX signal from COUNTER block.

2) DEAD TIME and L/R Blocks: The DEAD TIME block has three inputs, which are related to the top transistor gate signals, and generates the three couple of the gate outputs. In particular, each signal has a delay when a rising edge appears and it is configurable (in Section IV it is 500 ns). Before sending the three signals to the DEAD TIME block, the signals of the B and C legs of the inverter can be switched in order to impose either a clockwise or a counterclockwise direction of rotation for $\overline{V_{REF}}$ [21].

IV. Experimental Results

The proposed architecture has been implemented in an Altera Cyclone V 5CEBA4F17C17 FPGA [27] used to drive a three-phase power inverter composed by STMicroelectronics IGBT STGW40M120DF3, whose maximum f_{SW} is 10 kHz, and with a dc-input voltage of $V_{dc} = 100$ V and a 100 Ω resistor load for each phase output. The architecture is designed to have $f_C \in [1, 512]$ Hz with an incremental step of 0.125 Hz, $f_{SW} \in [1, 100]$ kHz with an incremental step of 1 Hz, $\Delta\phi = 2\pi 10^{-5} = 3.6 \cdot 10^{-3}$, $\theta \in [0°, 360°]$ with a step of 1°, $m_a \in [0, 1.06]$ with a step of 0.01, and $f_{CLK} = 50$ MHz.

In Fig. 7 the phase and line output voltages of the power inverter are shown for a $f_C = 50$ Hz and a $m_a = 0.5$ and the typical SVPWM third-harmonics injection in the phase

TABLE II
ALU SEQUENCE OF OPERATIONS FOR THE CALCULATION OF THE DWELL-TIMES

Clock Iteration	Multiplication Shift	Multiplication Position	Subtraction Shift	Subtraction Position	Division Shift	Division Position
1	$f_C \times f_C$				$j'_{MAX} = f_{SW}/(f_C \; sll \; 2)$	
2	$a_2 = 2.72 \times f_C$				$j_{MAX} = int(j'_{MAX}/3)$	
3	$f'_{SWn} = f_C \times j_{MAX}$				$D_2 = \theta/11.25$	
4	$f_{SWn} = (f'_{SWn} \; sll \; 2) \times 3$					$S_\theta = \theta/59.88$
5	$G_1 = (S_j \; sll \; 1) \times j_{MAX}$	$G_1 = (S_\theta \; sll \; 1) \times j_{MAX}$			$D_1 = (f_C \; sll \; 5)/f_{SWn}$	
6	$f_C^2 \times f_C$		$G_2 = j - (\overline{G_1} + 1)$		$P = D_2/D_1$	
7	$K'' = m_a \times f_{CLK}$		$j'_\theta = G_2 - (\overline{P} + 1)$	$j_\theta = P - G_1$	$T_{SW} = 1/f_{SWn}$	
8	$a'_3 = 14.8 \times f_C^2$				$S'_\theta = j'_\theta/(j_{MAX} \; sll \; 1)$	
9	$G_3 = (S'_\theta \; sll \; 1) \times j_{MAX}$				$G_4 = S'_\theta/6$	
10	$a''_4 = 17.9 \times f_C^3$		$j_\theta = j'_\theta - G_3$		$G_5 = G_4/0.167$	
11	$j \times j$		$S_\theta = S'_\theta - G_5$		$n_{SW} = f_{SWn}/f_{SW,old}$	
12	$a_1 = 0.75 \times f_{SWn}$				$n_C = f_{C,old}/f_C$	
13	$a'_4 = a''_4 \times T_{SW}$					
14	$a_3 = a'_3 \times T_{SW}$					
15	$a_4 = a'_4 \times T_{SW}$					
16	$K' = K'' \times T_{SW}$					
17	$K = K' \times T_{SW}$					
18	$T_{SW} \times f_{CLK}$					
19	$j^2 \times a_4$					
20	$j^2 \times a_3$		$H'_2 = a_2 - a_4 \times j^2$			
21	$H_2 = H'_2 \times j$		$H_1 = a_1 - a_3 \times j^2$			
22	$T_2 = (K \; sll \; 1) \times H_2$		$H = H_1 - H_2$			
23	$T_1 = K \times H$		$T'_0 = T_{SW} \times f_{CLK} - T_2$			
24	$n = n_C \times n_{SW}$		$T_0 = T'_0 - T_1$			
25	$j_n = j \times n$					

$(X \; sll \; y)$ is a logical left shift of the variable X by y bits, i.e. $2^y \cot X$. $(\overline{X} + 1)$ is the adding of 1 *bit* to the logical NOT of the variable X, i.e. $-X$.

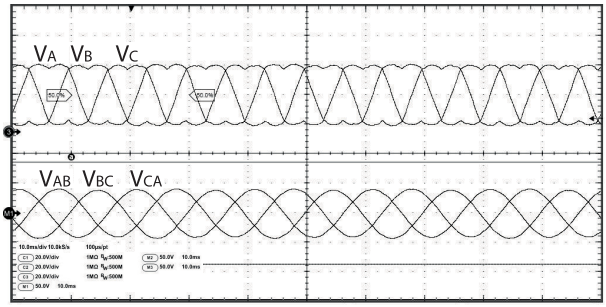

Fig. 7. Phase and line output voltages for $f_C = 50$ Hz, $f_{SW} = 10$ kHz, $m_a = 0.5$.

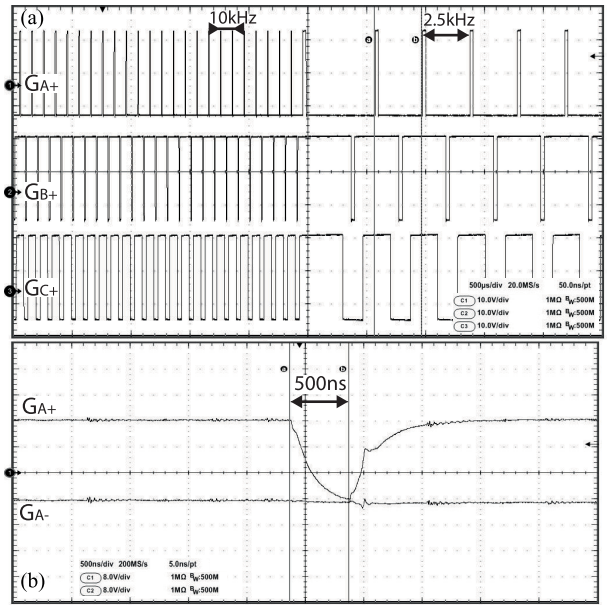

Fig. 8. (a) Experimental waveforms of the gate driver signal for the top transistors for a variation of f_{SW} from 100 to 25 kHz. (b) Experimental waveforms of G_{A+} and G_{A-} show a dead-time of 500 ns. $m_a = 1$, $f_{CLK} = 50$ MHz.

voltages is evident. The gate driver signals are reported in Fig. 8(a) and f_{SW} changes from 10 to 2.5 kHz in order to test the instantaneous variation of the f_{SW}; moreover, Fig. 8(b) reports the dead-time interval of 500 ns between G_{A+} and G_{A-}. In Fig. 9 the capability of the proposed architecture to change f_C and m_a in real-time is reported and distortions of the waveform are avoided thanks to the j update performed at steps 11–12 and 24–25 of Table II. In particular, in Fig. 9(a) the line voltages show an instantaneous variation of f_C from 50 to 1 Hz and 10 Hz and in Fig. 9(b) we apply a variation of the amplitude and f_C with the relation $m_a = 0.02 \cdot f_C$, where f_C varies from 1 to 50 Hz in 4 s. In this last case, the real-time changing of the values of m_a and f_C can be used for the V/f control of asynchronous three-phase motors, for example. Moreover, in Fig. 9(c) the three-phase output voltages and the current of the leg-A are reported for discontinuous load variations between 50 and 100 Ω. Then, in Fig. 10 the line output voltages have an instantaneous phase variation: Fig. 10(a) reports the position function of Section III-A, where $\theta^* = \theta_{new}$ of (10), and Fig. 10(b) reports the Shift function of Section III-A, where $\theta^* = \theta_{delay}$ of (11)–(12). In Table III the hardware resources are reported for our implementation both in Altera Cyclon V

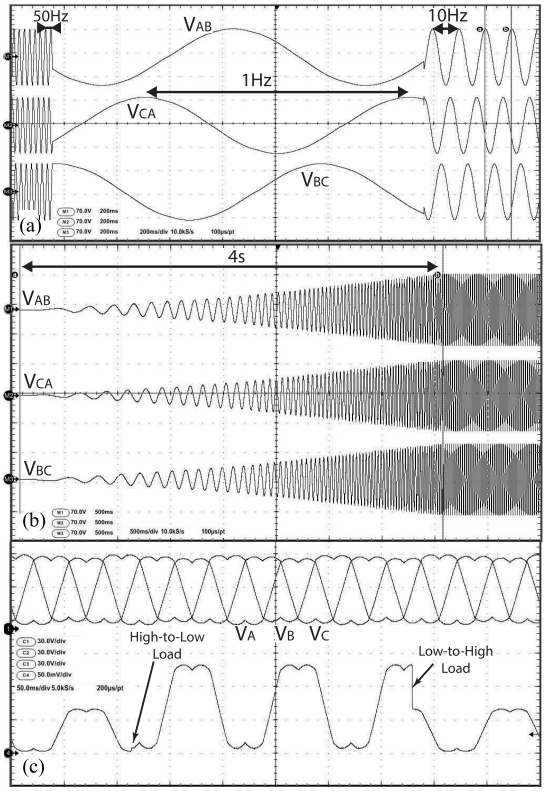

Fig. 9. Experimental line voltage waveforms with (a) instantaneous variation of $f_C = [50, 1, 10]$ Hz and (b) continuous variation of f_C from 1 to 50 Hz and a proportional $m_a = 0.02 \cdot f_C$ in an interval time of 4 s. Set-up is $f_{SW} = 10$ kHz, $f_{CLK} = 50$ MHz, $V_{dc} = 100$ V. (c) Phase voltages and current of the phase-A during load variations between 50 and 100 Ω with $f_C = 10$ Hz, $f_{SW} = 10$ kHz, $f_{CLK} = 50$ MHz, and $V_{dc} = 70$ V.

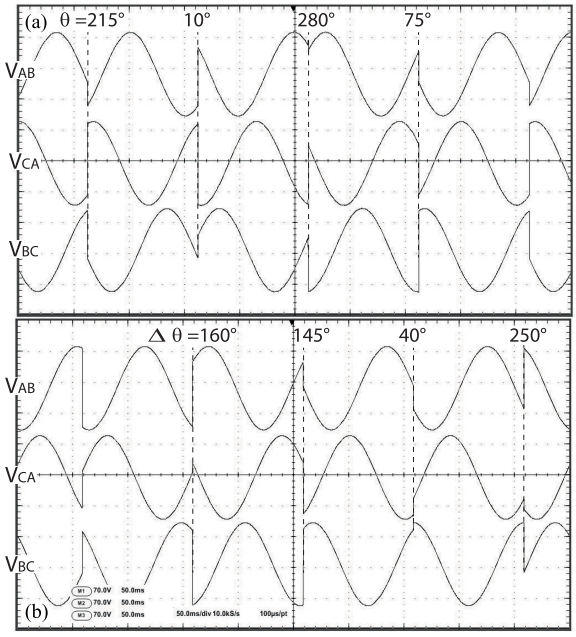

Fig. 10. Experimental line voltage waveforms with an instantaneous variation of θ using (a) position function ($\theta^* = \theta_{new}$) and (b) shift function ($\theta^* = \theta_{delay}$). Set-up is $f_C = 10$ Hz, $f_{SW} = 10$ kHz, $f_{CLK} = 50$ MHz, $V_{dc} = 100$ V.

[27] and in Xilinx Artix 7 [28], which has less resource. In both cases, DSPs are avoided and a 16% and 2% of the overall LUT and FF are, respectively, used for Cyclon V [27], whereas

TABLE III
COMPARISONS OF THE SYNTHESIS WITH THE STATE-OF-ART

		LUT	BRAM	FF	DSP	Dyn.Pow. $[mW]$	Config. Contr.
This work	CycloneV [27]	2878	0	1441	0	4.66*	int.
	Artix7 [28]	4798	0	1488	0	1.69**	int.
LUT [21]	CycloneV [27]	4986 (+73%)	0	382 (-73%)	0	18.19* (+290%)	int.
	Artix7 [28]	9121 (+90%)	0	878 (-41%)	0	7.91** (+368%)	int.
CORDIC Cascade	CycloneV [27]	4007 (+39%)	0	853 (-40%)	0	3.84*(-17%)	int.
	Artix7 [28]	5929 (+24%)	0	847 (-43%)	0	0.97** (-42%)	int.
CORDIC Iterative	CycloneV [27]	3271 (+13%)	0	880 (-39%)	0	3.81*(-18%)	int.
	Artix7 [28]	4591 (-4%)	0	872 (-41%)	0	0.96** (-43%)	int.
Cyclone II	[29]	780	-	88	-	28*	ext.
Spartan III	[22]	161	-	77	11	-	ext.
Spartan III	[30]	810	3	188	0	-	ext.
Cyclone IV	[31]	903	-	18	0	-	ext.

Configuration for Dynamic Power evaluation: $f_C = 150Hz$, $f_{SW} = 10kHz$, $m_a = 1$, and $f_{CLK} = 50MHz$ for *-case or $f_{CLK} = 12MHz$ for **-case.

a 23% and 3.58% for Artix 7 [28]. Moreover, Cyclon V [27] shows a dynamic power consumption of 4.7 mW, evaluated by PowerPlay Power Analyzer Tool from Altera, whereas Artix 7 [28] of 1.69 mW, evaluated with Xilinx Power Estimator. In Table III we report an equivalent comparison among different implementations of the ALU block using LUT-base architecture [21] and CORDIC-algorithms on the same FPGAs and with the same configurations. The architecture of [21], which is based on LUT-memory, has around twice that of LUT and less than half of FF, thanks to a lower number of operations compared to our proposal, but has a less resolution of f_C, i.e., 1 Hz, and of f_{SW}, because only integer multiple of f_C and 2^{-n} multiple of f_{SW} can be selected. The CORDIC is designed with a 14-bits for the decimal part of the angle (see $\Delta\phi = 2\pi\, 10^{-5} = 0.0036$), and two architectures are proposed: the CORDIC Cascade has 15 evaluation layers and calculates the dwell-times in 13 clock periods; instead, the CORDIC Iterative one has a single evaluation layer invoked for 16 clock interval times and in 29 clock periods the dwell-times are obtained. For Cyclon V [27], among all cases our proposal needs less number of LUTs, whereas a high number of FFs needs due to the partial results of our ALU, as reported in Fig. 4(b), which also justifies the few increasing of the dynamic power. Finally, in Table III we also reported comparisons from the state-of-art: if on one hand they need lower LUT and FF, on the other hand, [29] shows a higher dynamic power dissipation, [22] needs 11 DSPs, [30] require three BRAM (for a total of 54 kbit) and [31] outputs an overmodulated SVPWM. Although such differences can also depend on the implementation of the HW in the particular FPGA, they need an external controller, i.e., PC or microcontroller, that generates external three-phase reference signals to define f_C, m_a, and θ, limiting their applications in stand-alone systems.

V. CONCLUSION

In this article, we show a novel hardware architecture for the generation of the gate drive signals of three-phase inverters through SVPWM technique and is based on the Taylor series decomposition of the dwell-times. The variation of inputs is useful in real-time digital controls, for example in closed-loop system for the asynchronous motor. Moreover, the proposed architecture can be also implemented in micro-controllers as well as in integrated circuits, making it attractive for

System-On-Chip products. Limitations are the maximum $f_{SW,max} \leq f_{CLK}/25$ and the minimum required resources, that depend on the resolution of the dwell-times and on the minimum number of bits of a_4, due to $f_{C,min}$ and $f_{SW,max}$.

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