Nonlinearities of Multisampled Phase-Shifted PWM in Unbalanced Multicell Converters

Ruzica Cvetanovic, *Graduate Student Member, IEEE*, Ivan Z. Petric, *Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Simone Buso, *Member, IEEE*

***Abstract*— This article reveals, analyzes, and proposes the method to mitigate nonlinear effects of multisampled multiupdate (MSMU) digital pulsewidth modulation (PS-DPWM) that appear in unbalanced multicell voltage-source converters (MC-VSCs). For balanced MC-VSCs, the harmonic cancellation of PS-DPWM allows for an increase in the sampling frequency, ensuring that the average current is acquired at the peaks, valleys, and intersections of all the triangular carriers. For unbalanced operation, which is typically encountered in practice, e.g., due to cell voltage mismatch in multilevel MC-VSCs and inductance mismatch in interleaved MC-VSCs, harmonic cancellation of PS-DPWM is compromised and, thus, the increased sampling frequency brings switching ripple in the feedback signal. Since in MSMU control the modulating signal is also updated at peaks, valleys, and intersections of all the carriers, this may cause vertical intersections between the modulating signal and the carriers, resulting in specific nonlinear effects. The nonlinearities are shown to introduce limit-cycle oscillations (LCOs) and output waveform distortion. A method to prevent such detrimental impact of MSMU-PS-PWM is also proposed. A simple analytical procedure is proposed to quantify the analyzed nonlinear effects, revealing that they are more emphasized for higher levels of imbalance and control bandwidth. Moreover, the modulator nonlinearity is shown to decrease as the number of cells increases. The analyses are verified in simulations and experiments, using laboratory prototypes of three- and four-level MC-VSCs.**

***Index Terms*— Interleaved, limit-cycle oscillations (LCOs), multicell converters, multisampled multiupdate (MSMU) control, multilevel, phase-shifted pulsewidth modulation.**

I. Introduction

NOWADAYS, multicell voltage source converters (MC-VSCs) are widely used not only to overcome the voltage and current constraints of single power switches but also to achieve ultrahigh efficiency, power density, and dynamic performance [1], [2], [3], [4], [5], [6], [7]. Cells within MC-VSCs can be stacked in series or in parallel, resulting in multilevel [2], [3], [4], [5], [6] or interleaved MC-VSCs [7], [8], [9].

A widely used modulation strategy for MC-VSCs is the digital pulsewidth modulation (PS-DPWM) [2], [3], [4], [5], [7], where the carriers of the subsequent cells are phase-shifted with respect to each other, so that harmonic cancellation is achieved at the output [10], [11]. Under balanced conditions, this yields an increased frequency of the output current ripple, i.e., frequency multiplication [12], enabling output filter reduction [7], [12] and control loop bandwidth improvement [6], [13], [14], [15], [16], [17].

For regulating the output current of PS-DPWM MC-VSCs, multisampled multiupdate (MSMU) control is a widely adopted strategy, due to improved dynamic performance and robustness, offered by a significant reduction in the modulation delay [13], [14], [15], [16], [18], [19], [20], [21]. In MSMU-PS-DPWM, the sampling of the output current and update of the modulating signal are performed at peaks, valleys, and intersections of all the triangular carriers. Due to frequency multiplication of PS-DPWM, MSMU control in balanced MC-VSCs without any nonidealities does not feature any switching ripple component of the modulating signal. Therefore, MSMU in MC-VSCs is often claimed to be a natural linear extension of the double-sampled double-update control used in two-level VSCs [13], [14], [16], [21], completely neglecting thereby its behavior in unbalanced scenarios, which are the most often encountered in practice [1], [9], [22], [23], [24], [25].

Since in MSMU the modulating signal is updated at the peaks, valleys, and intersections of all the carriers, vertical intersections between the modulating signal and the carriers may occur around certain operating points [19], [26], [27]. In MSMU two-level VSCs, vertical intersections occur even in steady-state conditions as the switching ripple is always introduced into the feedback loop. On the other hand, in balanced MSMU MC-VSCs, vertical intersections are not possible in steady-state conditions. Nevertheless, ideally balanced operation is rarely achieved in practice due to tolerances of passive components, timing mismatches in gate-driving circuits, transients, different nature of the sources/loads connected to each cell's dc link, etc. [1], [5], [9], [22], [23], [24], [25], [28], [29], [30], [31], [32]. Imbalance deteriorates frequency multiplication and causes the switching ripple to appear in the

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Ruzica Cvetanovic and Simone Buso are with the Department of Information Engineering, University of Padua, 35131 Padua, Italy (e-mail: ruzica.cvetanovic@phd.unipd.it; simone.buso@dei.unipd.it).

Ivan Z. Petric is with Hanwha Q CELLS America Inc., Santa Clara, CA 95054 USA (e-mail: ivan.petric@phd.unipd.it).

Paolo Mattavelli is with the Department of Management and Engineering, University of Padua, 36100 Vicenza, Italy (e-mail: paolo.mattavelli@unipd.it).

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feedback. This may also happen under balanced conditions, if center-pulse (synchronous) sampling [33] is impaired, e.g., due to delays in driver circuits, deadtimes, and delays in sensing circuits. As a consequence, in its sampled variant, the modulating signal features jump discontinuities [27], which pose a risk for vertical intersections. Though their impact on two-level VSCs with MSMU-DPWM is well-investigated [27], the behavior of MSMU-PS-DPWM in unbalanced MC-VSCs has not been addressed in the literature so far.

To fill in the gaps of previous research, this article analyses the discontinuity-related nonlinear effects of MSMU-PS-DPWM that appear in unbalanced MC-VSCs. For accurate modeling of PS-DPWM behavior, a static transcharacteristic is defined for each phase-shifted carrier separately. Then, it is shown that similar to MSMU two-level VSCs, depending on the sign of the modulating signal discontinuity, vertical intersections cause reduced-gain, zero-gain, and infinite-gain (jitter) zones in the transcharacteristics [26], [27], [34]. In contrast to MSMU two-level VSCs, it is demonstrated that vertical intersections in MSMU MC-VSCs always cause limit-cycle oscillations (LCOs). For MC-VSCs with a dc operating point, this prevents steady-state operation to be achieved, whereas in case of ac operating point, the output current is strongly distorted. Thus, in industrial applications where a certain degree of imbalance is most often encountered, a widely used MSMU-PS-DPWM may bring a detrimental impact, which is for the first time analyzed in this article and demonstrated using laboratory prototypes of three- and four-level MC-VSCs. The extent of discontinuity-related nonlinear effects in unbalanced MC-VSCs with MSMU-PS-DPWM is shown to be proportional to the relative imbalance magnitude and relative crossover frequency of the current control loop. As the number of cells increases, the modulating waveform discontinuities are reduced, causing therefore nonlinearity of MSMU-PS-DPWM to diminish. Still, to prevent the detrimental impact of modulator nonlinearity that is pronounced in unbalanced multilevel and interleaved converters with lower number of cells, some provision has to be taken in practical applications. As one such a method, this article proposes digital feedback filtering which removes the switching ripple from the sampled current without impairing control loop's small-signal dynamic performance. Although reported before for two-level VSCs with MSMU-DPWM [35], [36], the use of RRRs in MC-VSCs with MSMU-PS-DPWM has not been considered before, as ripple-induced nonlinearities were neglected.

This article is organized as follows. In Section II, MSMU-PS-DPWM control of MC-VSCs is introduced, and the basic types of intersections between the modulating signal and the carriers are outlined, along with an explanation of the jittering mechanism. The impact of mismatched dc link voltages in multilevel MC-VSCs and mismatched inductances in interleaved MC-VSCs on the appearance of the switching ripple component in the modulating signal is illustrated in Section III. The resulting nonlinear effects are quantitatively analyzed in Section IV and their adverse effect on converter's input and output waveforms is illustrated. In Section V, the experimental measurements of modulator transcharacteristics are shown to be in excellent agreement with the simulations and analytics.

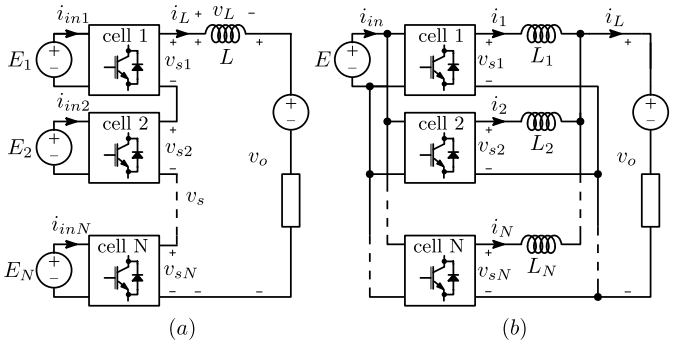

Fig. 1. Single-phase MC-VSC (a) multilevel and (b) interleaved topology. Each cell can be realized as a half- or full-bridge.

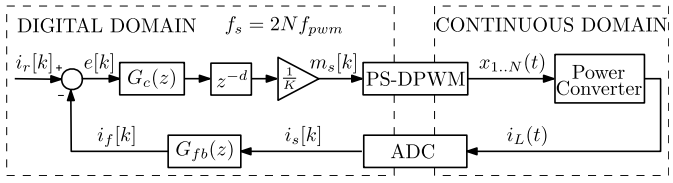

Fig. 2. System block diagram of digital, current-controlled, single-phase, MC-VSC with symmetric MSMU-PS-DPWM.

The detrimental impact of LCOs on the performance of dc–dc and dc–ac MC-VSCs is also experimentally verified as illustrated in Section V in the time domain. Section VI concludes the article. As an addendum, suppression of the reported nonlinear effects of MSMU-PS-DPWM is addressed in Appendix.

II. MSMU Control of Multicell Converters

A. System Description

In this article, digital current-controlled MC-VSCs with MSMU-PS-DPWM are considered. As examples of multilevel and interleaved MC-VSCs, single-phase converters consisting of N series- and parallel-stacked half-bridge or full-bridge cells, shown in Fig. 1, are used. Nevertheless, the presented methodology can be applied to other single- or multiphase multicell topologies with MSMU-PS-DPWM.

In Fig. 1(a), each cell is supplied from a separate dc source, E_i. The output voltages of all the cells, $v_{s1}, \ldots, v_{sN}$, are summed to form the output voltage of the MC-VSC, v_s. The difference between v_s and load voltage v_o is applied to an inductive filter, L. In Fig. 1(b), all the cells are supplied from the same dc source, E. The output voltage of each cell, v_{si}, is applied to an inductor, L_i, and the currents of all the inductors, $i_1, \ldots, i_N$, are summed to form the output current, i_L, of the MC-VSC.

A block diagram of the considered current-controlled system is shown in Fig. 2. An analog-to-digital converter (ADC) performs the transition from continuous to digital domain. The sampling of i_L is performed at the center of the applied voltage pulses, ensuring the center-pulse (synchronous) sampling [33], with the rate f_s equal to the total number of edges that can be modulated. Under balanced conditions, this ensures removal of the switching ripple from i_L. Assuming half-bridge cells and

PS-DPWM with $(360°/N)$ phase shift[1] between the adjacent triangular[2] carriers [10], this yields $f_s = 2Nf_{\text{pwm}} = N_{\text{ms}} f_{\text{pwm}}$, where f_{pwm} is the switching (carrier) frequency and N_{ms} is the multisampling factor. In the case of full-bridge cells with bipolar PS-DPWM, nothing changes compared with half-bridge cells. The analysis is also easily extendable to unipolar PS-DPWM.

If the application of interest requires digital feedback filtering, the sampled current i_s can be processed by $G_{fb}(z)$, resulting in i_f.[3] By subtracting i_f from the reference i_r, the error signal e is obtained and used as the input to the current controller G_c. The controller output update is delayed by d sampling periods $T_s = (1/f_s)$, due to the finite execution time [33]. The voltage reference generated by the current controller is scaled by K to the range $[0, 1]$, resulting in the digital modulating signal m_s. For half-bridge cells $K = E_\Sigma$, where $E_\Sigma = NE_n$ for multilevel and $E_\Sigma = E_n$ for interleaved converters, and E_n is the cell's nominal input dc voltage. For full-bridge cells $K = 2E_\Sigma$, and an additional offset has to be added, which is not shown in Fig. 2 as it does not affect the proposed analysis. The entire digital system runs at the rate determined by the sampling frequency f_s.

The PS-DPWM serves as an interface between digital and continuous domains. This article considers symmetric PS-DPWM, where the same signal m_s is used to modulate each cell. Its inherent ZOH function transforms m_s to m and compares it with the carrier w_i, belonging to DPWM$_i$. In this way, the switching signal x_i is obtained, which is a square waveform with duty cycle D_i.[4] It is used to control the power switches within the ith cell of the MC-VSC.

B. Intersections Between Modulating Signal and Carriers

In multisampled single- and double-update PS-DPWM, the modulating signal for each cell is updated at the peaks and/or valleys of the carrier corresponding to that cell [16], [18]. This results in only horizontal intersections between the modulating signal and the carrier. In MSMU-PS-DPWM, the modulating signal, which is the same for all cells, is updated at every sampling instant, i.e., at the peaks, valleys, and intersections of all the carriers, which is more than twice per carrier period, $T_{\text{pwm}} = (1/f_{\text{pwm}})$. Thus, due to the discontinuity of m, vertical intersections between m and w_i are now possible [19], [20], [27].

[1]As a starting point, this article considers PS-DPWM with a fixed phase shift value [equal to $(360°/N)$], leaving the consideration of PS-DPWM with variable phase shift [23], [28], [29], [30], [31], [32] for future studies.

[2]PS-DPWM with triangular carriers simplifies the choice of sampling instants that coincide with the average current values [5]. Moreover, it allows dual-edge modulation [37], which improves the transient response capabilities; hence, triangular carriers are typically chosen over the sawtooth ones. For this reason, the following analysis considers the triangular carriers.

[3]Motivation for digital feedback filtering can be various, e.g., to enhance noise suppression capabilities [17], [38], [39] or to avoid introducing switching ripple in feedback under unbalanced operation, as discussed in Appendix. Other than the analyses in Appendix, the MSMU-PS-DPWM control system without digital feedback filtering ($G_{fb} = 1$) is considered in this article, to provide a generic analysis of the underlying phenomena.

[4]In the steady-state without any nonidealities ($m_s = D = \text{const.}$), due to symmetric PS-DPWM, $D_1 = D_2 = \cdots = D_N = D$ and $V_o = DE_\Sigma$, where V_o is the (dc) steady-state value of the load voltage v_o.

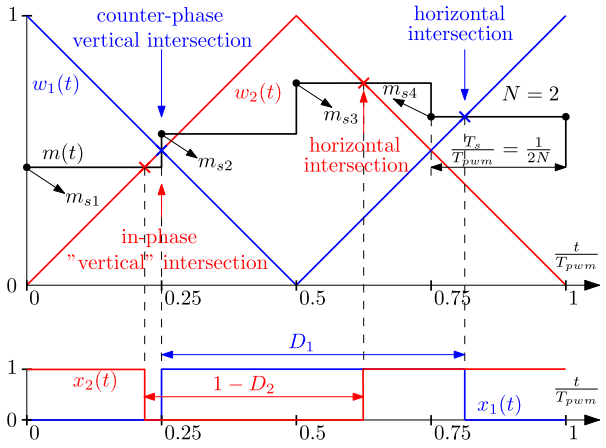

Fig. 3. Different intersections between m and w_i for MSMU-PS-DPWM with $N = 2$. For DPWM$_1$, corresponding to w_1, a counter-phase vertical and a horizontal intersection occur during negative and positive slopes of w_1, respectively. For DPWM$_2$, corresponding to w_2, an in-phase "vertical" and a horizontal intersection occur during positive and negative slopes of w_2, respectively. To prevent multiple commutations, the switching action of DPWM$_i$ is defined by the first intersection between m and w_i, which turns in-phase "vertical" into horizontal intersections.

Due to the imposed synchronization between the update of m and the carriers, vertical intersections may occur only around certain operating points, which are determined by N_{ms} [27]. These operating points are defined as the *critical* duty cycles

$$D_c = \frac{2k}{N_{\text{ms}}} = \frac{k}{N} \tag{1}$$

where $1 \leq k < N$ and k is an integer.

To analyze the modulator nonlinearities induced by vertical intersections, it is important to differentiate between in-phase and counter-phase operation, determined by the relationship between the slope of m and the slope of w_i [27]. When, at the update instant closest to the intersection with w_i, the slope of m has the same sign as the slope of w_i, the intersection and the operation of DPWM$_i$ are referred to as *in-phase* [27]. On the other hand, when the slopes have opposite signs, the intersection and the operation of DPWM$_i$ are referred to as *counter-phase* [27]. An interesting property of MSMU-PS-DPWM is that an in-phase operation for one carrier is a counter-phase operation for another carrier, which is illustrated in Fig. 3 for MSMU-PS-DPWM with $N = 2$ (to make the illustration clear, but the same holds also for higher N). This is because the modulating signal is updated at instants when exactly two carriers intersect. As shown in Sections IV and V, this has a detrimental impact on the nonlinear phenomena that appear in MC-VSCs.

C. Jitter Amplification Phenomenon

In [27] and [34], it is shown that for two-level converters in-phase operation and the modulating signal discontinuity result in jitter amplification phenomenon. Since in case of MC-VSCs, as previously explained, at least one of the phase-shifted carriers always features in-phase operation, vertical intersections always result in jitter amplification phenomenon, which is for the first time analyzed in this article. The mechanism

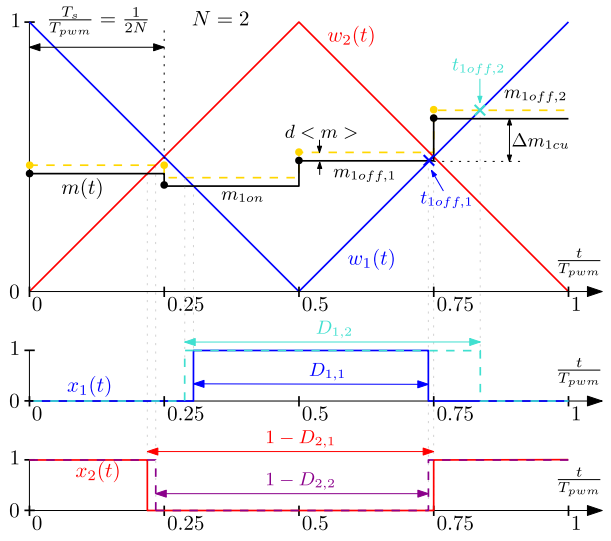

Fig. 4. Example of an operating regime that may cause jitter amplification for MSMU-PS-DPWM with $N = 2$. In-phase operation that is present for w_1, together with the modulating signal discontinuity, poses a risk for limit cycling (duty cycle jittering).

behind it is illustrated in Fig. 4 and briefly explained below, using MSMU-PS-DPWM with $N = 2$ as an example, but the conclusions remain the same also for other values of N.[5]

In the example shown in Fig. 4, an in-phase operation is present for w_1. Consider an initial operating point, where the falling edge of x_1 is determined by the intersection between w_1 and the modulating segment $m_{1\text{off},1}$, resulting in the duty cycle $D_{1,1}$. In case the closed-loop control yields a small change in the controller's output, such that a higher duty cycle is required, the modulating signal is incremented by a certain amount $d\langle m\rangle$. As illustrated in Fig. 4, a very small positive $d\langle m\rangle$ causes the falling edge of x_1 to be determined by the following segment $m_{1\text{off},2}$, which changes the duty cycle from $D_{1,1}$ to $D_{1,2}$. As the applied duty cycle is higher than the required one, the controller will respond by decreasing the value of m, which, in the subsequent switching period, may again cause the segment $m_{1\text{off},1}$ to intersect with w_1. Thus, x_1 is determined by the modulating signal discontinuity Δm_{1cu}, rather than $d\langle m\rangle$. This results in limit cycling (duty cycle jittering) that has detrimental impact on system performance, as illustrated by the time-domain waveforms from simulations and experiments for MC-VSCs with dc and ac operating point. The incapability of MSMU-PS-DPWM to achieve desired duty cycle is manifested as "increased-gain" regions in the modulator static transcharacteristics corresponding to the carriers that feature an in-phase operation, as explained in Section IV-A.

D. Enabling Mechanism Behind Vertical Intersections

For vertical intersections to occur, some disturbance is required when the operating point is close to D_c. For example, a change in m can be caused by reacting to transient variations or, under steady-state conditions, by the switching ripple component. In this article, the effects due to the latter are addressed.

For balanced MC-VSCs with MSMU-PS-DPWM, the ripple frequency is increased to Nf_{pwm}, which allows for sampling the average current with the rate $f_s = 2Nf_{\text{pwm}}$. Therefore, considering the ideal choice of sampling instants, switching ripple of i_L is not introduced in the feedback signal and m does not contain any switching ripple component. However, with imbalance, the frequency multiplication is lost and the switching ripple appears in m.

Mismatched values of the cells' dc link voltages, in case of multilevel MC-VSCs, and of the inductances, in case of interleaved MC-VSCs, are used in this article as illustrative examples of the imbalance. To analyze the nonlinearity of MSMU-PS-DPWM with such an imbalance, it is of interest to gain insight into the shape of the switching ripple waveform at D_c, as addressed in Section III.

III. Switching Ripple Around Critical Operating Points in Unbalanced Multicell Converters

A. Output Current Ripple in Multilevel MC-VSCs With Mismatched DC Links

The current ripple waveform in unbalanced multilevel MC-VSCs depends, in a general case, on the dc link voltages of all the cells. Thus, general statements about its shape require complicated spectral analyses [10], [40], which lack a clear insight, especially for higher N. To illustrate core principles without using complex mathematical procedures, for the subsequent analyses, we introduce some assumptions regarding the distribution of imbalance among the cells. Nevertheless, it is important to emphasize that as verified in the simulations and experiments, the resulting nonlinear effects only quantitatively change in the most general case with an arbitrary imbalance distribution.

At first, it is assumed that $\sum_{i=1}^{N} E_i = NE_n$. For $N = 2$, this yields two possible imbalance distributions: $E_1 = E_n + \Delta E$, $E_2 = E_n - \Delta E$, and $E_1 = E_n - \Delta E$, $E_2 = E_n + \Delta E$, where $\Delta E > 0$ is referred to as the magnitude of the voltage imbalance. As an example, waveforms of interest at $D_c = (1/2)$ are shown in Fig. 5(a), for a multilevel MC-VSC with two half-bridge cells, $E_1 = E_n + \Delta E$ and $E_2 = E_n - \Delta E$. As seen, the output current ripple at $D_c = (1/2)$ is triangular with the fundamental frequency component at f_{pwm} and the peak–peak value

$$\Delta I = \frac{k_{D_c}\Delta E}{f_{\text{pwm}}L} = \frac{\Delta E_{D_c}}{f_{\text{pwm}}L} \tag{2}$$

where $k_{D_c} = (N/(N-1))D_c(1-D_c)$. There are cases, also for $N > 2$, where the output current ripple at D_c is a triangular waveform with the fundamental frequency component at f_{pwm} and the peak–peak value defined by (2). One such example is the following distribution of imbalance:

$$E_1 = E_n + \Delta E,\ E_2 = \cdots = E_N = E_n - \frac{\Delta E}{N-1}. \tag{3}$$

Relevant waveforms with such imbalance for a multilevel MC-VSC with three half-bridge cells are shown in Fig. 5(b),

[5]For high enough N, i.e., N_{ms}, discontinuity of the modulating signal is almost completely removed, eliminating thereby nonlinear effects caused by it and making the MSMU-PS-DPWM feature analog-like performance.

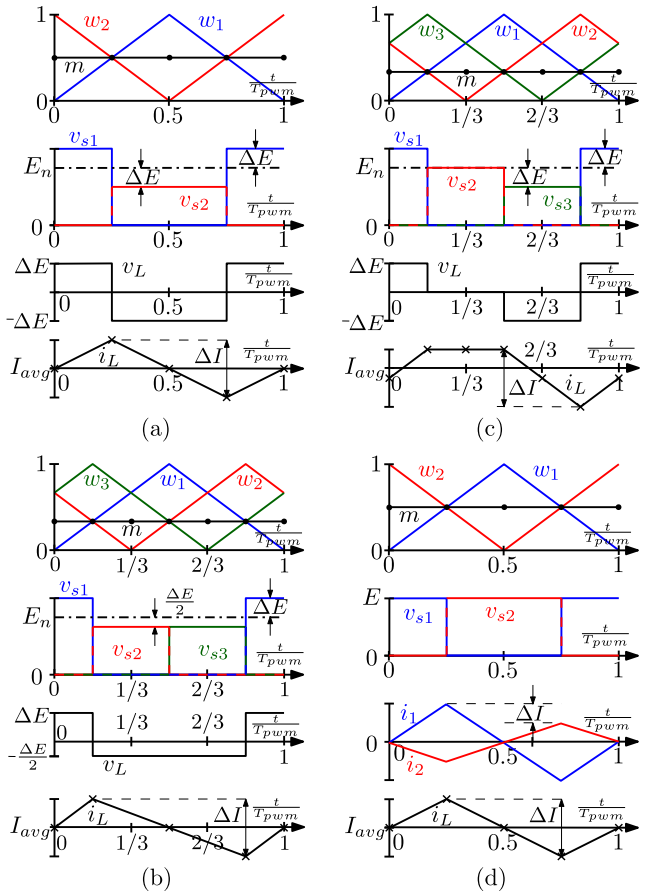

Fig. 5. Switching ripple at $D_c = (1/N)$ in multilevel MC-VSC with (a) $N = 2$, imbalance (3), (b) $N = 3$, imbalance (3), (c) $N = 3$, imbalance (4), and (d) unbalanced interleaved MC-VSC with $N = 2$ and $L_1 < L_2$.

at $D_c = (1/3)$. It is easy to show that for some imbalance distributions, the ripple is not triangular. For example, in Fig. 5(c) an illustration is given for

$$E_1 = E_n + \Delta E,\ E_2 = E_n,\ E_3 = E_n - \Delta E. \tag{4}$$

Nonetheless, it can be shown that for an arbitrary imbalance distribution, the peak–peak value of the current ripple at D_c and ΔI, is proportional to the joined imbalance magnitude, ΔE_{D_c}, determined at each D_c as described below. Namely, due to PS-DPWM, the voltage across the inductor, $v_L(t)$, is a piecewise constant waveform, which, in a general case, at D_c features N different values V_{Lh} within one T_{pwm}, where $h = (1, \ldots, N)$ denotes the index of the segment, starting from $w_1 = 0$, during which $v_L(t) = V_{Lh}$. Each V_{Lh} causes i_L to change for ΔI_h within the time period (T_{pwm}/N), i.e., $\Delta I_h = (V_{Lh}/Nf_{\text{pwm}}L)$. By finding the array of subsequent voltages applied to the inductor that features the highest sum Σ, the peak–peak value of the inductor current ripple at D_c, in case of an arbitrary imbalance distribution, is determined

$$\Delta I = \frac{\Sigma}{Nf_{\text{pwm}}L} = \frac{\Delta E_{D_c}}{f_{\text{pwm}}L}. \tag{5}$$

Note that for balanced operation where $\Delta E_{D_c} = 0$, at D_c $\Delta I = 0$, which is a known property of PS-DPWM. Due to this property, the operating points defined by (1) are sometimes called nominal conversion ratios [5].

B. Output Current Ripple in Interleaved MC-VSCs With Mismatched Inductances

To illustrate the influence of mismatched inductances on the shape of the output current ripple at D_c in interleaved MC-VSCs, the waveforms of interest are shown in Fig. 5(d) for an interleaved MC-VSC with two half-bridge cells, $L_1 = L_n - \Delta L$ and $L_2 = L_n + \Delta L$, where L_n is the nominal inductance and $\Delta L > 0$ is the magnitude of the inductance imbalance. As seen from Fig. 5(d), the current ripple exhibits the same waveform as the one in Fig. 5(a), with the peak–peak value given by

$$\Delta I = \frac{D_c E}{f_{\text{pwm}}}\left(\frac{1}{L_n - \Delta L} - \frac{1}{L_n + \Delta L}\right). \tag{6}$$

It can be shown that also in interleaved MC-VSCs with $N > 2$, the influence of the imbalance on the shape of the output current ripple at D_c is similar to the one in multilevel MC-VSCs. Thus, without loss of generality, the subsequent analyses are performed for multilevel MC-VSCs, but the conclusions are easily applied also to interleaved MC-VSCs. This was verified by running simulations also for interleaved MC-VSCs converters, but the results are not included due to space limitations.

C. Modulating Signal Ripple

For regulating the output current of the MC-VSCs, proportional–integral or proportional–resonant controllers are widely used [1], [2], [13], [14]. They are designed so that the impact of the integral or the resonant action is bandlimited well below the crossover frequency f_c. Consequently, at high frequencies, their frequency response converges to the one determined by the proportional gain. Thus, for these, high-frequency proportional-dominant controllers, the peak–peak value of the switching ripple component of the modulating signal, Δm_{pp}, can be very closely approximated as proportional to the relative crossover frequency f_{cr} of the current loop [26]. Moreover, since at D_c, $\Delta I \propto \Delta E$, Δm_{pp} at D_c is proportional to the relative imbalance magnitude, ΔE_r

$$\Delta m_{pp} \approx \frac{k_p \Delta I}{K} \propto \frac{f_c}{Nf_{\text{pwm}}}\frac{\Delta E}{E_n} = f_{cr}\Delta E_r \tag{7}$$

where $k_p = 2\pi f_c L$ is the proportional gain of the current controller. Thus, the nonlinear effects of MSMU-PS-DPWM in unbalanced MC-VSCs, caused by the ripple in m, can be analyzed in a relative manner, by changing only ΔE_r and f_{cr}. Note that in addition to ΔE_r and f_{cr}, the time delay present in the propagation path of switching and feedback signals also impacts the modulator nonlinearities. Namely, by shifting the position of the modulating signal ripple with respect to the carriers, delay affects the types of intersections between m and w_i [27].

IV. Analysis of MSMU-PS-DPWM Nonlinearities in Unbalanced Multicell Converters

A. Modulator Transcharacterization

One way to describe the behavior of the modulator is a static transcharacteristic [27], which, in case of PS-DPWM, has to be

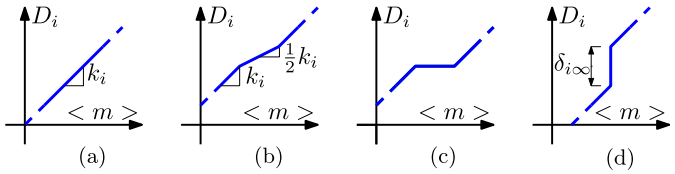

Fig. 6. Types of zones that may appear in transcharacteristic of DPWM$_i$ (a) linear behavior obtained with double horizontal intersections, (b) reduced-gain zone obtained with a single counter-phase vertical intersection, (c) zero-gain (dead-band) zone obtained with double counter-phase vertical intersections, and (d) infinite-gain (jitter) zone obtained with in-phase "vertical" intersection.

defined for each carrier separately. The transcharacteristic of DPWM$_i$ provides the value of D_i, as a function of the average value of the modulating signal over one switching period, $\langle m \rangle$, calculated as an average of N_{ms} values of m_s within one T_{pwm}. In Fig. 3, this corresponds to $((m_{s1} + m_{s2} + m_{s3} + m_{s4})/4)$.

The transcharacteristic of DPWM$_i$ is a piecewise linear function, with different gains $k_i = (dD_i/(d\langle m \rangle))$ of each linear segment, determined by different types of intersections between m and w_i. In this article, k_i is referred to as the gain of DPWM$_i$. In case of horizontal intersections between m and w_i, D_i is determined by a unique modulating signal and both the edges of x_i are equally modulated by applying a small perturbation of the modulating signal, $d\langle m \rangle$. Thus, linear behavior of DPWM$_i$ is achieved and $k_i \approx 1$, as shown in Fig. 6(a). Note that in the presence of an imbalance, k_i is not exactly equal to 1 due to the ripple modulation effect [26]. Vertical intersections between m and w_i cause the gain of DPWM$_i$ to deviate from $k_i \approx 1$ [27]. Counter-phase vertical intersections can occur for one or both the slopes of w_i, preventing thereby the modulation of one or both the edges of x_i. This results in reduced- or zero-gain (dead-band) zones [26] in the transcharacteristic of DPWM$_i$, which, as shown in Fig. 6(b) and (c), feature $k_i \approx (1/2)$ and $k_i = 0$. The logic that prevents multiple commutations turns the in-phase "vertical" intersections into horizontal ones, which brings another nonlinear phenomenon. Namely, as explained in Section II-C, a small perturbation $d\langle m \rangle$ causes the response of one or both the edges of x_i to be determined by the modulating signal discontinuity, instead of $d\langle m \rangle$, resulting in increased gain of DPWM$_i$. The in-phase "vertical" intersections can appear for both the slopes of w_i, or in combination with a horizontal or counter-phase vertical intersection. With in-phase operation, there is a range of duty cycles for which the steady-state cannot be achieved, and thus, the transcharacteristics are not defined [34]. However, to indicate their impact, the corresponding nonlinearity zones are represented by vertical lines ($k_i \to \infty$), as shown in Fig. 6(d). These zones are referred to as infinite-gain (jitter) zones [27], because they result in LCOs, which have an adverse effect in MC-VSCs with either dc or ac operating point, as demonstrated in simulations and experiments.

B. Discontinuities of Critical Modulating Segments

Since the vertical intersections occur to an extent determined by the discontinuity of m [27], to quantify the actuator (modulator) nonlinearity induced by them, it is of interest to define the critical modulating segments and their discontinuities.

Similar to the definitions in [27] and [34], the critical modulating segments of DPWM$_i$ are defined as the two subsequent segments of m before and after the update instant closest to the intersection between m and w_i. For each DPWM$_i$, two pairs of critical modulating segments exist, each corresponding to one of the slopes of w_i.

The discontinuities of DPWM$_i$'s critical modulating segments for positive (Δm_{icu}) and negative (Δm_{icd}) slopes of w_i are then defined as in [27]

$$\begin{aligned} \Delta m_{icu} &= m(T_{icu} + \epsilon) - m(T_{icu} - \epsilon) \\ \Delta m_{icd} &= m(T_{icd} - \epsilon) - m(T_{icd} + \epsilon) \end{aligned} \tag{8}$$

where ϵ is an infinitely small positive number, and T_{icu} and T_{icd} are the modulating signal update instants closest to the intersection with w_i. Equation (8) is defined such that positive values of $\Delta m_{icu,d}$ correspond to in-phase operation.

The size of $\Delta m_{icu,d}$ is correlated with the extension of nonlinear zones that appear in DPWM$_i$'s transcharacteristics around D_c. The in-phase discontinuities of each slope of w_i contribute to its respective jitter zone heights as $\delta_{i\infty u,d} = (\Delta m_{icu,d}/2)$ [27]. As verified in Sections IV-D and IV-E, when the in-phase operation occurs for both the slopes of w_i, the joined height of the jitter zones can be estimated as

$$\Delta D_{i\infty} = \frac{\Delta m_{icu}}{2} + \frac{\Delta m_{icd}}{2}. \tag{9}$$

Thus, it is of interest to provide a simple analytical procedure which would, for each DPWM$_i$, predict whether an in-phase or counter-phase operation occurs, as well as the size of $\Delta m_{icu,d}$ around D_c.

C. Analytical Calculation of the Discontinuities

To calculate $\Delta m_{icu,d}$, it is necessary to find $m(t)$. The exact analytical calculation of $m(t)$ requires an iterative procedure, whose steps for two-level VSCs are described in [26] and [27]. Since its extension to MC-VSCs brings additional complexity, in this article, an approximate procedure is used, which is based on the naturally sampled equivalent of the modulating signal, $m_{ns}(t)$ [27]. As shown in [27], the use of the approximate procedure is justified for predicting $\Delta m_{icu,d}$, since, for the high-frequency proportional-dominant controllers, its results negligibly deviate from those of the exact procedure. To obtain $m_{ns}(t)$, the analog equivalent of the modulating signal ripple, $m_{rd}(t)$, has to be found. The procedure relies on an assumption that all the control blocks can be represented in the s-domain.

For the assumed imbalance distribution (3) and the operating point (1), the converter circuit is solved for all the topological states, considering only the average value of the modulating signal (as in Fig. 5). The resulting triangular ripple of the inductor current $i_{\text{rip}}(t)$ is then found. Next, $i_{\text{rip}}(t)$ is used to solve a set of controller-related equations, which, after scaling by K, yields $m_r(t)$. Finally, an arbitrary amount of time delay

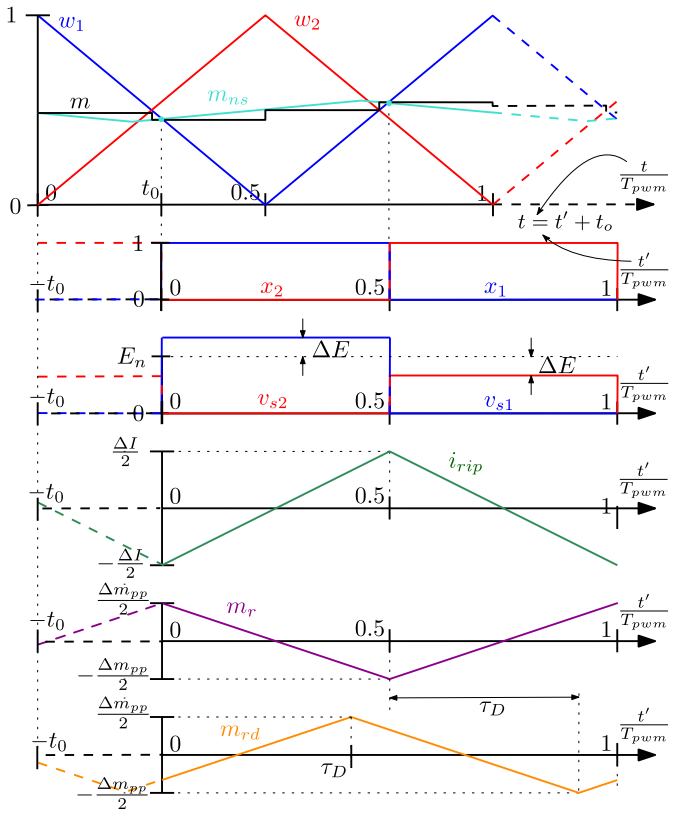

Fig. 7. Illustration of the procedure used to obtain modulating signal ripple component, $m_{rd}(t)$, naturally sampled equivalent of the modulating signal $m_{ns}(t)$ and its resampled variant. Illustration is given at $D_c = (1/2)$, for an MC-VSC with $N = 2$ and the imbalance from (3). A purely proportional current controller is assumed and the relative delay is equal to τ_D.

$\Delta t = \tau_D T_{\text{pwm}}$ is added to obtain $m_{rd}(t)$. This time delay[6] can be due to the algorithm execution time, feedback filters, delays in the sensing and driver circuits, etc.

Based on $m_{rd}(t)$ and the operating point considered, the naturally sampled modulating signal $m_{ns}(t)$ is calculated relative to the first carrier [26]. This waveform is then used to find an approximate version of $m(t)$, obtained by resampling $m_{ns}(t)$ at assumed sampling instants. This approximation only slightly shifts the switching instants with respect to the exact calculation. The procedure described above is illustrated in Fig. 7 for an MC-VSC with $N = 2$, the imbalance from (3), and the purely proportional current controller. The resampled version of $m_{ns}(t)$ is used to calculate $\Delta m_{icu,d}$, as in (8). More details about the analytical calculation of the modulating signal discontinuities can be found in [26], [27], [41], and [35], and in the MATLAB script `discont_calculation.m` that is submitted with this article, as supplementary material.

D. Discontinuity Graphs

This section presents discontinuity graphs that provide the value of $\Delta m_{icu,d}$ as a function of τ_D. Note that with the above-described procedure for analytical calculation of the modulating signal discontinuities, it is sufficient to obtain the discontinuity graph only for the first carrier. Namely, by simply shifting it for the value equal to the phase shift of the considered carrier, the discontinuity graphs for all the other carriers can be obtained. The MATLAB script `discont_graphs.m` used to obtain the discontinuity graphs is uploaded as active content with the article, to provide more insight.

The discontinuity graphs are given for $\tau_D \in [0,1]$, which is sufficient due to the periodicity of the switching ripple. The impact of ΔE_r on $\Delta m_{icu,d}$ is also illustrated. As predicted by (7), the influence of f_{cr} is verified to be the same as that of ΔE_r. For the presentation conciseness, the results below are obtained for fixed $f_{cr} = 0.1$.

Although vertical intersections also appear in the vicinity of D_c, the discontinuity graphs are plotted only at D_c, since, as shown below, this is sufficient to predict properties of MSMU-PS-DPWM transcharacteristics around D_c. Note that with the imbalance distribution from (3), the discontinuity graphs at D_c for the positive slope of w_i are the same as the graphs at $1 - D_c$ for the negative slope of w_i.

In Fig. 8, the discontinuity graphs for $N = 2$ and $D_c = (1/2)$ are shown for various imbalances. Since for $D_c = (1/2)$ and $D_c = 1 - D_c$, the discontinuity graphs for the positive and negative slopes of w_i are the same. The presented discontinuity graphs are proportional to ΔE_r, as implied by (7). Under balanced conditions, i.e., for $\Delta E_r = 0$, the calculated discontinuities are zero, and thus, the vertical intersections are not possible in the steady-state. In addition, it is seen from Fig. 8 that the borders between the in-phase and counter-phase regimes are almost independent of ΔE_r. The same is verified for f_{cr}. Based on this, it can be inferred that for the fixed imbalance distribution, τ_D defines whether the in-phase or counter-phase regime occurs, whereas the extent of the discontinuities is determined by ΔE_r and f_{cr}. Moreover, for the value of τ_D corresponding to the above-mentioned border, almost linear behavior of the modulator is achieved, regardless of ΔE_r and f_{cr}. Another important remark from Fig. 8 is that the discontinuity graphs of DPWM_1 are equal to the inverted graphs of DPWM_2. This is due to PS-DPWM, which causes the discontinuity graphs of adjacent carriers to feature the same shape, with the τ_D-axis shifted by the imposed phase shift, i.e., $(1/N)$.

In Fig. 9, the discontinuity graphs for $N = 3$ and $D_c = (1/3)$ and the imbalance distribution from (3) are shown. For the sake of presentation, only the results for $\Delta E_r = 0.2$ are plotted, but it is verified that as for $N = 2$, the values of the discontinuities are proportional to ΔE_r and f_{cr}, while the boundaries between the in-phase and counter-phase regimes remain located at nearly constant values of τ_D. From Fig. 9, it can be seen that the sum of maximum discontinuities for the positive and negative slopes of w_i is the same for all the DPWMs and reduced, compared with $N = 2$. This is an important remark, which underlines that as N increases, the discontinuity-related nonlinear effects of MSMU-PS-DPWM in unbalanced MC-VSCs are reduced. Note that this was also verified for $N > 3$, but the results are not included due to space limitations. In addition, given that the discontinuity related modulator nonlinearity is more pronounced for lower values of

[6]In addition to time delay, the intersections between the modulating waveform and the carriers can also be influenced by feedback filters, as shown in [34]. However, the time delay was found to be of more general value, not having to consider a specific filter design.

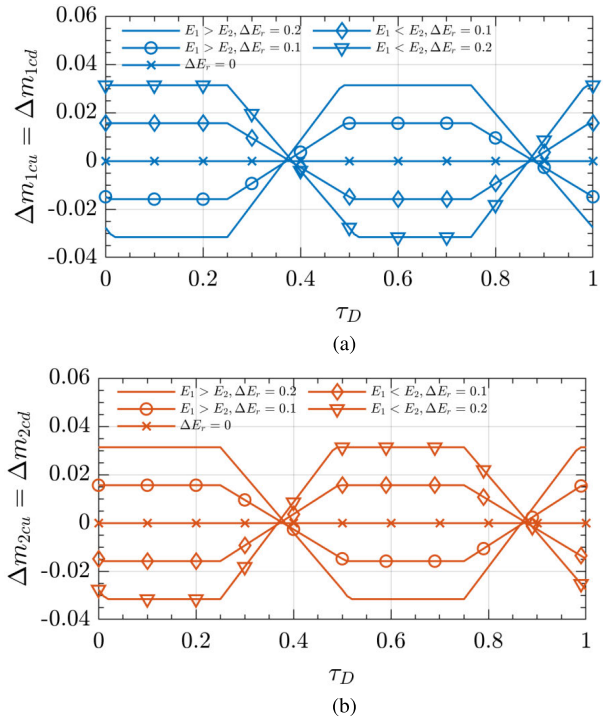

Fig. 8. Discontinuity graphs at $D_c = (1/2)$ for an MC-VSC with $N = 2$, $f_{cr} = 0.1$ and various imbalances (a) DPWM_1 and (b) DPWM_2.

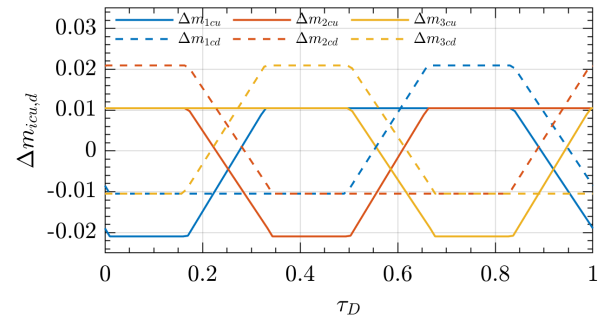

Fig. 9. Discontinuity graphs at $D_c = (1/3)$ for an MC-VSC with $N = 3$, $f_{cr} = 0.1$, imbalance distribution from (3), and $\Delta E_r = 0.2$. The blue, red, and yellow colors correspond to $\text{DPWM}_{1,2,3}$, respectively.

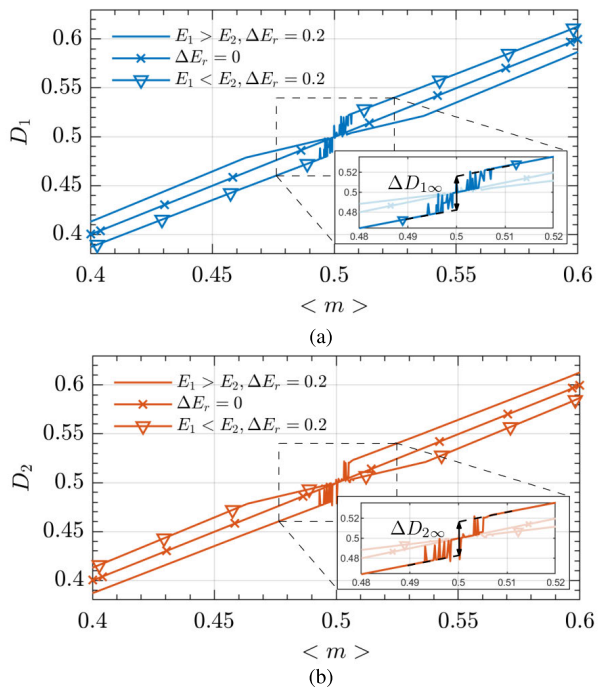

Fig. 10. Simulated transcharacteristics around $D_c = (1/2)$ for and MC-VSC with $N = 2$, $f_{cr} = 0.1$, $\tau_D = 0$, and various imbalances (a) DPWM_1 and (b) DPWM_2.

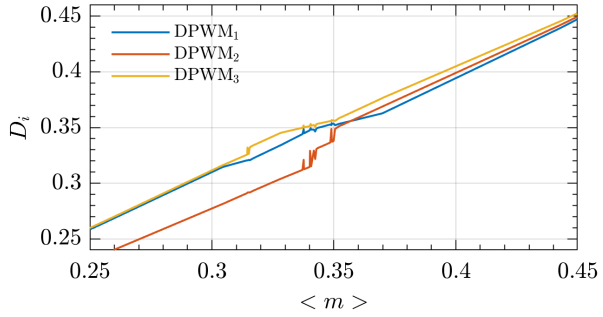

Fig. 11. Simulated transcharacteristics around $D_c = (1/3)$ for an MC-VSC with $N = 3$, $f_{cr} = 0.1$, $\tau_D = 0$, imbalance distribution from (3), and $\Delta E_r = 0.2$. The blue, red, and yellow colors correspond to $\text{DPWM}_{1,2,3}$, respectively.

N, the results in this article are presented for such values of N. For a very high number of cells, i.e., multisampling factors, the discontinuities and, consequently, the nonlinear effects caused by them, are almost completely suppressed, as the sampled feedback closely resembles the continuous analog signal [27].

E. Simulated Transcharacteristics

To verify the predictions of the discontinuity graphs, simulations are performed to obtain the transcharacteristics of MSMU-PS-DPWM around D_c. For this purpose, MC-VSCs with the parameters from Table I are implemented in MATLAB/Simulink. The transcharacteristics are obtained by imposing a slow current reference sweep while saving the values of the modulating signal m_s and the detected duty cycles $D_{1,\ldots,N}$. The Simulink model `sim_trch.slx` and the postprocessing script `plot_trch.m` used to obtain simulated transcharacteristics are submitted with this article, as active content.

In Fig. 10, the simulated transcharacteristics around $D_c = (1/2)$ are shown for $N = 2$, $\tau_D = 0$, and $f_{cr} = 0.1$, considering $E_1 > E_2$ and $E_1 < E_2$, both with $\Delta E_r = 0.2$. The results for $\Delta E_r = 0$ are also included to verify that MSMU-PS-DPWM is linear under balanced conditions. As predicted by the discontinuity graphs in Fig. 8, for $E_1 > E_2$, the transcharacteristics of DPWM_1 and DPWM_2 exhibit reduced-gain and jitter zones, respectively, while vice versa is observed for $E_1 < E_2$. Under unbalanced conditions, jittering of the detected duty cycle, caused by the LCOs, is clearly observable. In addition, the transcharacteristics of DPWM_1 and DPWM_2, obtained for $E_1 < E_2$, are, respectively, equal to those of DPWM_2 and DPWM_1, obtained for $E_1 > E_2$. Furthermore, the heights of the joined jitter zones in Fig. 10, $\Delta D_{1\infty} = \Delta D_{2\infty} = 0.032$, are the same as those calculated from (9), by substituting $\Delta m_{icu,d}$ predicted by the graphs in Fig. 8.

In Fig. 11, the simulated transcharacteristics around $D_c = (1/3)$ are shown for $N = 3$, $\tau_D = 0$, $f_{cr} = 0.1$, imbalance

TABLE I
HARDWARE AND CONTROL PARAMETERS OF THE TESTED MC-VSCS

MC-VSC	label	value	unit
Number of cascaded cells	N	$\{2, 3\}$	/
Nominal dc link voltage	E_n	$\{120, 50\}$	V
Filter inductance	L	1.5	mH
Output capacitance	C	470	μF
Output resistance	R	24	Ω
Switching frequency	f_{pwm}	$10/N$	kHz
Dead-time	t_{dt}	0.8	μs
Control loop	**label**	**value**	**unit**
Sampling frequency	f_s	20	kHz
Crossover frequency	f_c	$\{1, 0.5\}$	kHz
Proportional gain	k_p	$\{9.6, 4.7\}$	Ω
Integral / resonant gain	k_i	$\{5.9, 1.5\}$	kΩ/s

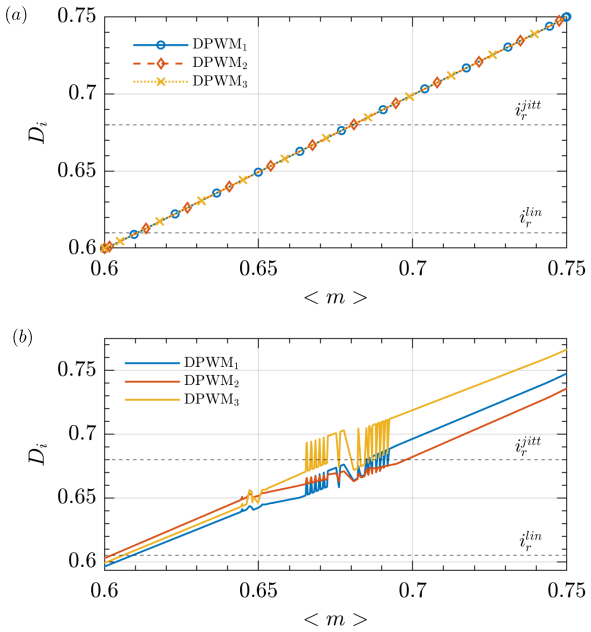

Fig. 12. Simulated transcharacteristics around $D_c = (2/3)$ for an MC-VSC with $N = 3$, $\tau_D = (1/N)$, $f_{cr} = 0.1$ and (a) balanced dc links $E_1 = E_2 = E_3 = E_n$ and (b) arbitrarily chosen imbalance distribution: $E_1 = 1.23E_n$, $E_2 = 0.86E_n$, and $E_3 = 0.91E_n$. The blue, red, and yellow colors correspond to DPWM$_{1,2,3}$, respectively.

distribution from (3), and $\Delta E_r = 0.2$. As predicted by the discontinuity graphs in Fig. 9, the transcharacteristics of DPWM$_1$ and DPWM$_2$ exhibit reduced-gain and jitter zones, respectively, whereas for DPWM$_3$ both the reduced-gain and jitter zones are present. Note that in addition to the LCOs observed around the jitter zones in the transcharacteristic of the DPWM$_i$ that features an in-phase operation, some smaller amplitude LCOs are also visible in the transcharacteristics of all other DPWMs. This is because LCOs, caused by the in-phase operation of DPWM$_i$, are present in the system and thus also impact the operation of other DPWMs. This is an important remark that demonstrates that the in-phase operation for one carrier is sufficient to cause jittering in the overall system. Moreover, since, as mentioned in Section II-B, a counter-phase operation for one carrier is at the same time an in-phase operation for another carrier, vertical intersections in unbalanced MC-VSCs with MSMU-PS-DPWM always cause jittering. This conclusion is valid regardless of the imbalance distribution, and, as shown in Section V, the jittering effect is more pronounced for higher τ_D and f_{cr}.

To further elaborate on this, in Fig. 12 the simulated transcharacteristics around $D_c = (2/3)$ are shown for $N = 3$, $\tau_D = (1/N)$, $f_{cr} = 0.1$, and (a) balanced dc links: $E_1 = E_2 = E_3 = E_n$ and (b) an arbitrarily chosen imbalance distribution: $E_1 = 1.23E_n$, $E_2 = 0.86E_n$, and $E_3 = 0.91E_n$. As expected, under balanced conditions, linear behavior of MSMU-PS-DPWM is achieved. However, in the presence of an arbitrarily chosen imbalance, the nonlinear effects are clearly visible, which shows that the nonlinearity of MSMU-PS-DPWM is present regardless of the imbalance distribution. To illustrate its detrimental impact on the performance of the MC-VSC, the reference step change is imposed, which in the presence of imbalance moves the operating point from the linear to jitter zone (as marked in Fig. 12). The time-domain input and output converter waveforms in response to this reference change are shown in Fig. 13 under balanced ($E_1 = E_2 = E_3 = E_n$) and in Fig. 14 under unbalanced conditions ($E_1 = 1.23E_n$, $E_2 = 0.86E_n$, $E_3 = 0.91E_n$). In addition to the raw waveforms [shown in gray color in Figs. 13(b)–(f) and 14(b)–(f)], the waveforms obtained after removing the switching ripple (using a moving average filter over T_{pwm}) are also shown, for a better visualization. After the step reference change, under balanced conditions (Fig. 13), the steady-state is achieved and the responses are as expected. However, in the presence of imbalance (Fig. 14), the steady-state cannot be achieved and the LCOs, caused by the nonlinearity of MSMU-PS-DPWM, are clearly visible in the converter waveforms, which is in accordance with the corresponding transcharacteristics from Fig. 12(b).

V. EXPERIMENTAL VALIDATION

This section provides experimental validation of the previously discussed nonlinear phenomena observed in unbalanced MC-VSCs with MSMU-PS-DPWM and illustrates their influence in typical application scenarios. For dc–dc converters, the impact on the transient response and the occurrence of LCOs is examined. For dc–ac converters, the impact on the output waveform distortion is analyzed.

A. Test Setup

For the experimental measurements, a single-phase current-controlled laboratory prototype of the MC-VSC from Fig. 2 is realized, with the hardware and control loop parameters from Table I. The block diagram and the picture of the test setup are shown in Figs. 15 and 16. The setup consists of three main parts, denoted by three different colors in Fig. 15. Red part represents the tested MC-VSC, realized using the SiC half-bridge modules from Imperix. An inductive filter is used and a resistive load is connected in parallel with the output capacitor. Inductor current is sensed by an external sensor from Imperix, which is based on LAH 50-P from LEM.

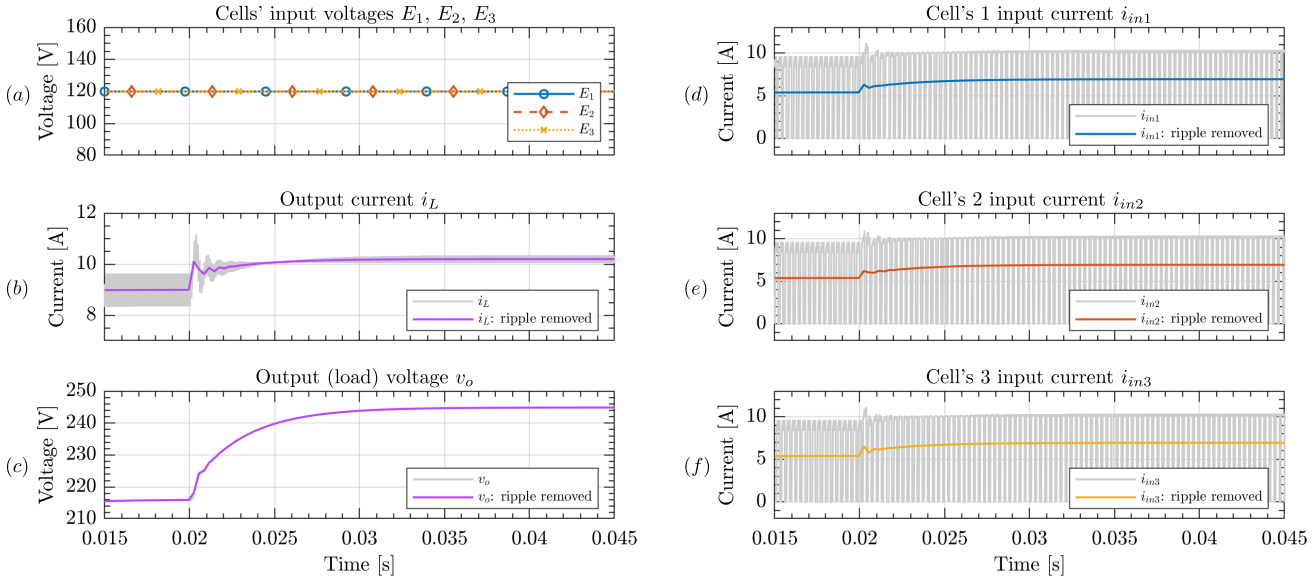

Fig. 13. Simulation results for an MC-VSC with $N = 3$, $\tau_D = (1/N)$, $f_{cr} = 0.1$, and balanced dc links: $E_1 = E_2 = E_3 = E_n$. Input and output converter waveforms in response to the reference step change from i_r^{lin} to i_r^{jitt} (marked in Fig. 12), which in the presence of imbalance moves the operating point from the linear to jitter zone (a) cell's input voltages (b) output current (c) output (load) voltage, and (d)–(f) cell's input currents. For a better visualization, in addition to the raw waveforms [shown in gray color in (b)–(d)], the waveforms after removing switching ripple are also shown.

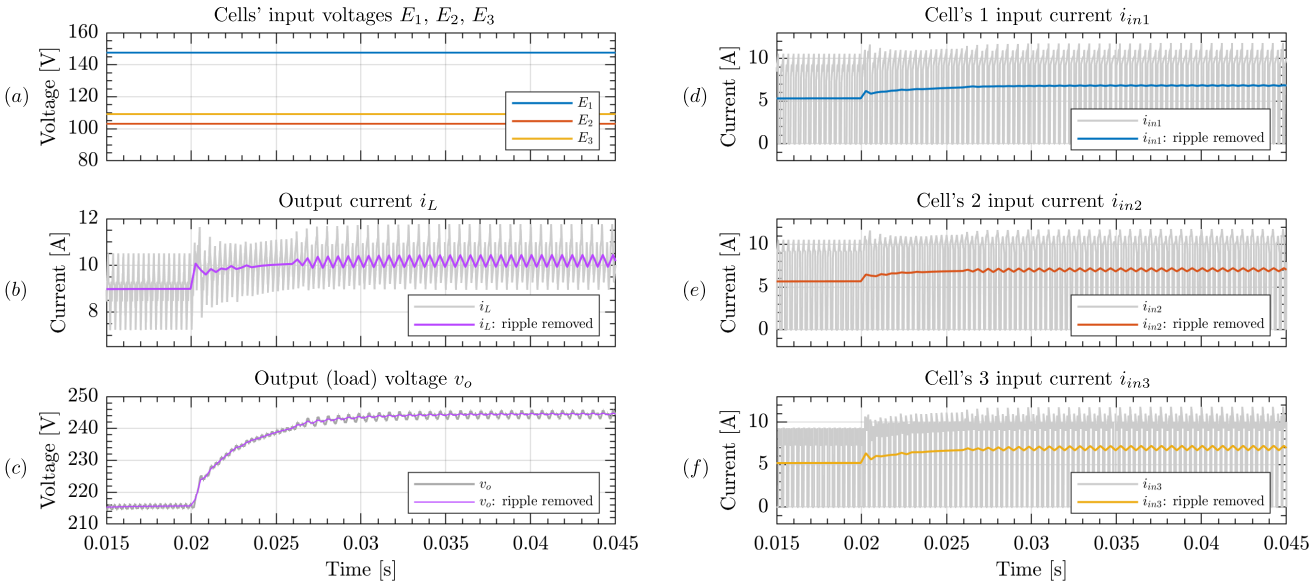

Fig. 14. Simulation results for an MC-VSC with $N = 3$, $\tau_D = (1/N)$, $f_{cr} = 0.1$, and an arbitrarily chosen imbalance distribution: $E_1 = 1.23E_n$, $E_2 = 0.86E_n$, and $E_3 = 0.91E_n$. Input and output converter waveforms in response to the reference step change from i_r^{lin} to i_r^{jitt}, which moves the operating point from the linear to jitter zone, as marked in Fig. 12(a) (a) cell's input voltages, (b) output current, (c) output (load) voltage, and (d)–(f) cell's input currents. For a better visualization, in addition to the raw waveforms [shown in gray color in (b)–(d)], the waveforms after removing switching ripple are also shown.

The control system, denoted by blue color in Fig. 15, is implemented on Imperix B-Box Embedded Control Module, using both the DSP and FPGA that are available on the board. The ADC and the current control are implemented on DSP. Due to the algorithm computation time, the modulating signal update is delayed by one sampling period, T_s. An additional delay is added in some tests, to examine the impact of delay on the modulator nonlinearities, as analyzed in Section IV. The digital modulating signal, m_s, is forwarded to the FPGA via Imperix sandbox, which serves as an interface between DSP and FPGA and ensures a proper synchronization. The MSMU-PS-DPWM is coded in VHDL and implemented on the FPGA, with the DPWM clock that runs at $f_{\text{clk}} = 125$ MHz. The switching signals, $x_{1,\ldots,N}$, are sent back to DSP where deadtime is realized. To obtain modulator transcharacteristics, the duty cycles $D_{1,\ldots,N}$ are detected on the FPGA, forwarded to DSP, and exported together with m_s, using Imperix Cockpit. Postprocessing, denoted by yellow color in Fig. 15, is performed in MATLAB. For examining transient response and waveform distortion, the inductor current is acquired with

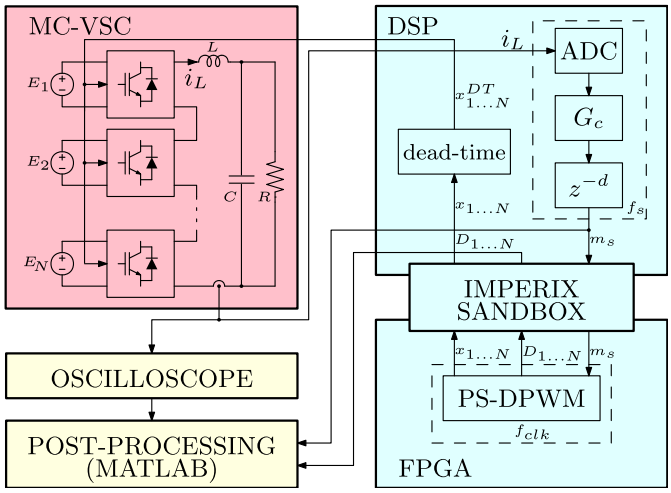

Fig. 15. Block diagram of the test setup used to experimentally validate nonlinear effects of MSMU-PS-DPWM in unbalanced MC-VSCs.

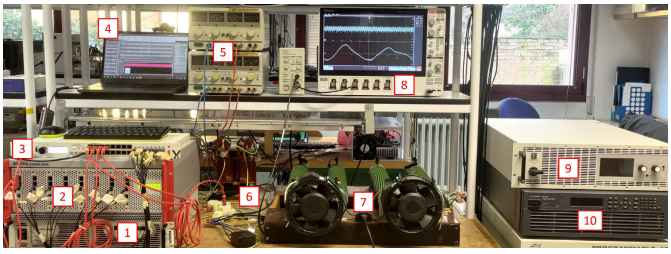

Fig. 16. Test setup used for experimental validation. 1) Power supply TDK/Lambda GEN300-17 used for the dc–dc tests, 2) SiC half-bridge modules from Imperix, 3) boom box controller, 4) laptop, 5) power supplies GW GPC-3030 used for the dc–ac tests, 6) filter inductor, output capacitor, and sensing circuits, 7) resistive load, 8) oscilloscope; power supplies, 9) EA-PSI 9750-20TDK, and 10) Keysight RP7962A used for the dc–dc tests.

12.5 MS/s rate, using the Tektronix TCP202 current probe and MS056 oscilloscope.

B. Impact of Nonlinearities in DC–DC Converters

As examples of dc–dc converters, multilevel MC-VSCs with two and three half-bridge cells are formed. The dc link of each cell is realized using one of the following power supplies: Keysight RP7962A, TDK/Lambda GEN300-17, and EA-PSI 9750-20. The nominal dc link voltage is set to $E_n = 120$ V. The proportional–integral current controller is used

$$G_c(z) = k_p + k_i T_s \frac{z}{z-1} \tag{10}$$

where k_p and k_i are the proportional and integral gain, respectively.

In Fig. 17, the transcharacteristics, obtained by imposing current reference sweep in experiments and simulations, are shown around $D_c = (1/2)$, for the MC-VSC with $N = 2$, imbalance distribution from (3) and different τ_D, f_{cr}, and ΔE_r. According to the presented results, an excellent match between the simulations and experiments is achieved. Moreover, the types of zones and the joined jitter zone heights that appear in Fig. 17(a), (b), and (d) correspond to those predicted by the discontinuity graphs in Fig. 8. Compared with Fig. 17(a), the extensions of the nonlinear zones in Fig. 17(c) and (d) are halved, which is in agreement with (7).

In the presented simulated and experimentally measured transcharacteristics, the impact of LCOs on system inability to achieve steady-state operation is seen, around the operating points where nonlinearity zones exist. This causes a stochastic jittering of the duty cycle. The degree of this jittering depends on the LCOs' magnitude and frequency and should not be misinterpreted with the height of the jitter zone, which quantifies the extent of the actuator (modulator) nonlinearity. Note that it is also experimentally verified that under balanced conditions, i.e., for $\Delta E_r = 0$, linear transcharacteristics are obtained, but the results are not included due to space limitations.

In Figs. 18 and 19, the experimental results are shown for the MC-VSC with $N = 3$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance distribution from (4), and different ΔE_r. Comparison between the simulated and experimentally measured transcharacteristics around $D_c = (1/3)$ is shown in Fig. 18(a) and (b) for $\Delta E_r = 0.2$ and $\Delta E_r = 0.1$, respectively. An excellent match between the simulations and experiments is achieved. Moreover, the extent of the observed nonlinear effects is again scaled with ΔE_r. In Fig. 19, the effect of jittering and LCOs is illustrated in the time domain. A step reference change is imposed, so that, for $\Delta E_r \neq 0$, the operating point changes from the linear to jitter zone, as marked in Fig. 18(a) and (b). The tracking errors, relative to the maximum peak–peak current ripple present under balanced conditions, are shown in Fig. 19(a) for $\Delta E_r \in \{0, 0.1, 0.2\}$. For a better visualization, switching ripple is removed from the plotted data using a moving average filter over T_{pwm}. As expected, with unbalanced dc links, the steady-state cannot be achieved after the step reference change and the LCOs, caused by the modulator nonlinearity, are clearly visible in the presented waveforms. On the contrary, balanced dc links yield a linear operation. This is further illustrated in Fig. 19(b)–(d) where the inductor current in response to the same reference step change is shown for $\Delta E_r \in \{0, 0.1, 0.2\}$. In addition to the raw, unprocessed, data that are acquired by the oscilloscope and shown in gray color in Fig. 19(b)–(d), the waveforms obtained after removing the switching ripple are also shown, for a better visualization.

C. Impact of Nonlinearities in DC–AC Converters

As an example of dc–ac converter, a multilevel MC-VSC with two full-bridge cells is formed. The linear power supplies GW GPC-3030 are used as the cells' dc inputs, to avoid stability problems of the switched power supplies that were noted under unbalanced dc links and ac operation. The nominal dc link voltage is set to $E_n = 50$ V, which was the maximum possible due to hardware limitations of the power supplies.

To investigate the impact of the previously discussed phenomena on the output waveform distortion, a sinusoidal ac reference is imposed and the proportional–resonant current controller is used

$$G_c(z) = k_p + k_i T_s \frac{1 - \cos(2\pi f_1 T_s) z^{-1}}{1 - 2\cos(2\pi f_1 T_s) z^{-1} + z^{-2}} \tag{11}$$

where $f_1 = 50$ Hz is the fundamental frequency. Due to RLC load, at f_1, the output voltage lags the inductor current for 21°. Note that the simulations were performed with an

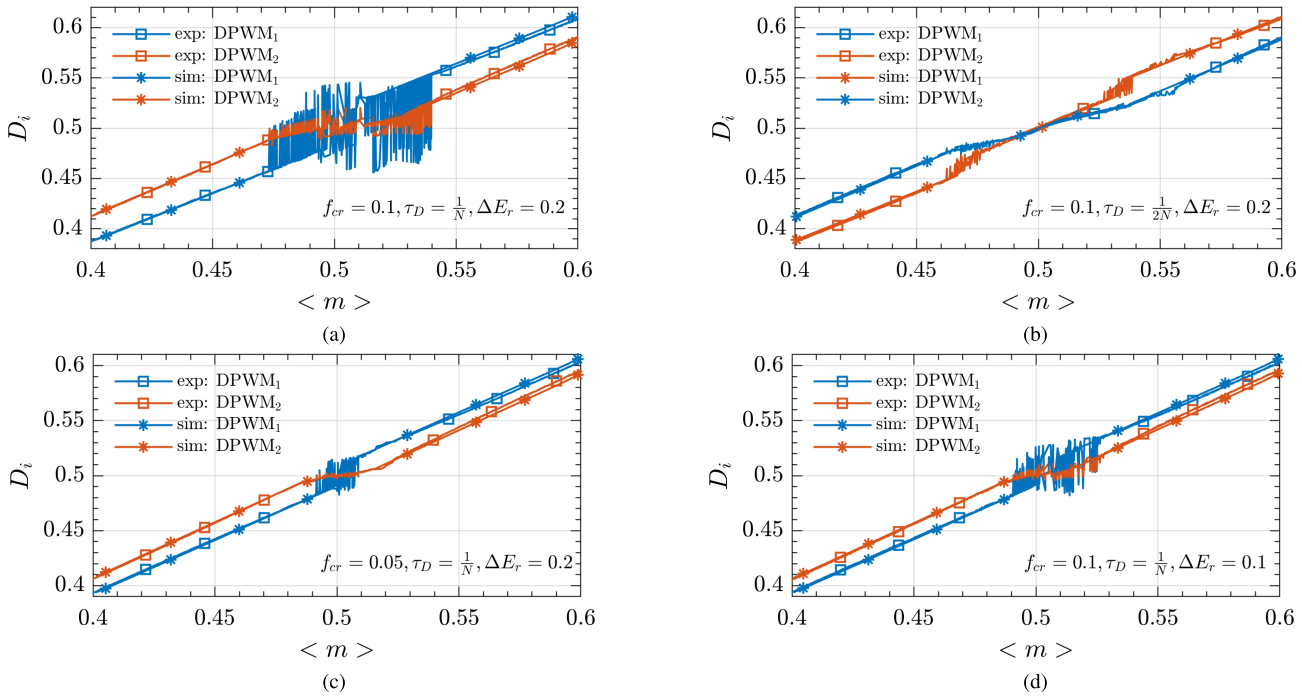

Fig. 17. Comparison between the experimentally measured and simulated transcharacteristics around $D_c = (1/2)$ for the MC-VSC with $N = 2$, imbalance distribution from (3), and different τ_D, f_{cr} and ΔE_r (a) $f_{cr} = 0.1$, $\tau_D = (1/N)$, and $\Delta E_r = 0.2$, (b) $f_{cr} = 0.1$, $\tau_D = (1/2N)$, and $\Delta E_r = 0.2$, (c) $f_{cr} = 0.05$, $\tau_D = (1/N)$, and $\Delta E_r = 0.2$, and (d) $f_{cr} = 0.1$, $\tau_D = (1/N)$, and $\Delta E_r = 0.1$.

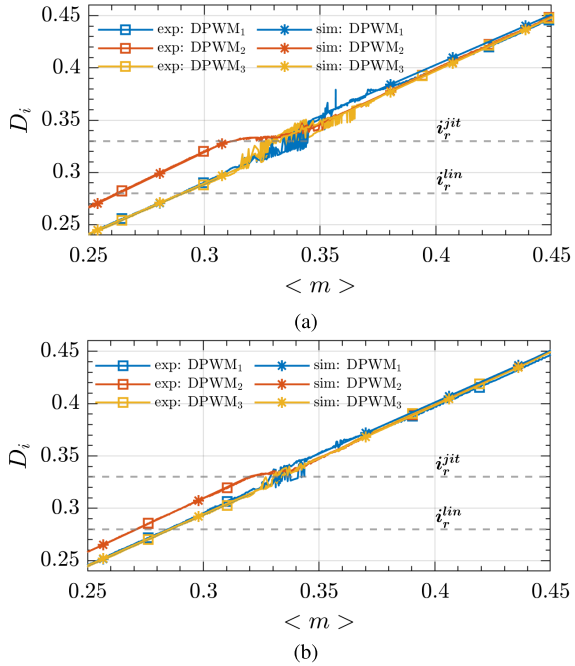

Fig. 18. Experimental results for the MC-VSC with $N = 3$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance distribution from (4), and $\Delta E_r \in \{0, 0.1, 0.2\}$. Comparison between the simulated and experimentally measured transcharacteristics for (a) $\Delta E_r = 0.2$ and (b) $\Delta E_r = 0.1$.

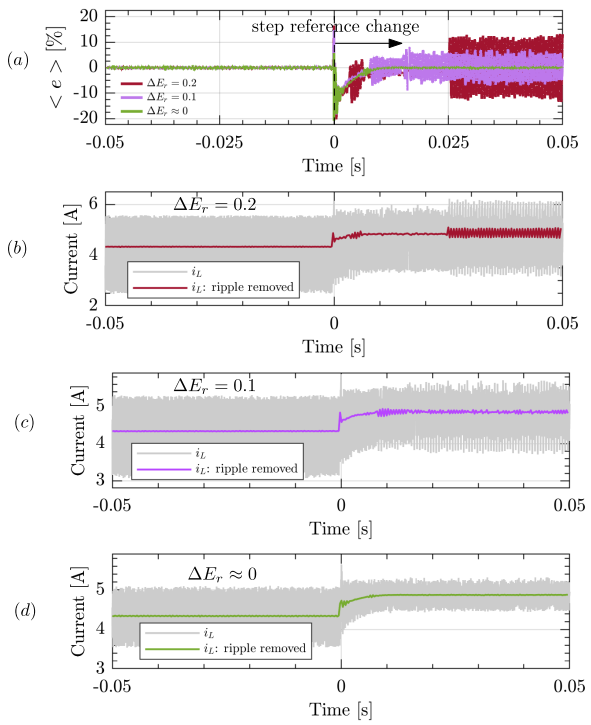

Fig. 19. Experimental results for the MC-VSC with $N = 3$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance distribution from (4), and $\Delta E_r \in \{0, 0.1, 0.2\}$. (a) Relative tracking errors of the reference step change from i_r^{lin} to i_r^{jit}, which for $\Delta E_r \neq 0$ moves the operating point from the linear to jitter zone, as marked in Fig. 18(a) and (b). The switching ripple is filtered out for a better visualization. The tracking errors are given relative to the maximum peak–peak current ripple present under balanced conditions. (b)–(d) Inductor current in response to the same reference step change.

inductive filter directly connected to an ac voltage source, and the conclusions remain the same as below.

At first, the transcharacteristics are measured around $D_c = (1/2)$ for $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance distribution from (3), and $\Delta E_r \in \{0, 0.2\}$. The results are confirmed to be similar to the ones of the previously tested MC-VSC with half-bridge cells. For $\Delta E_r = 0.2$, the jittering occurs, same

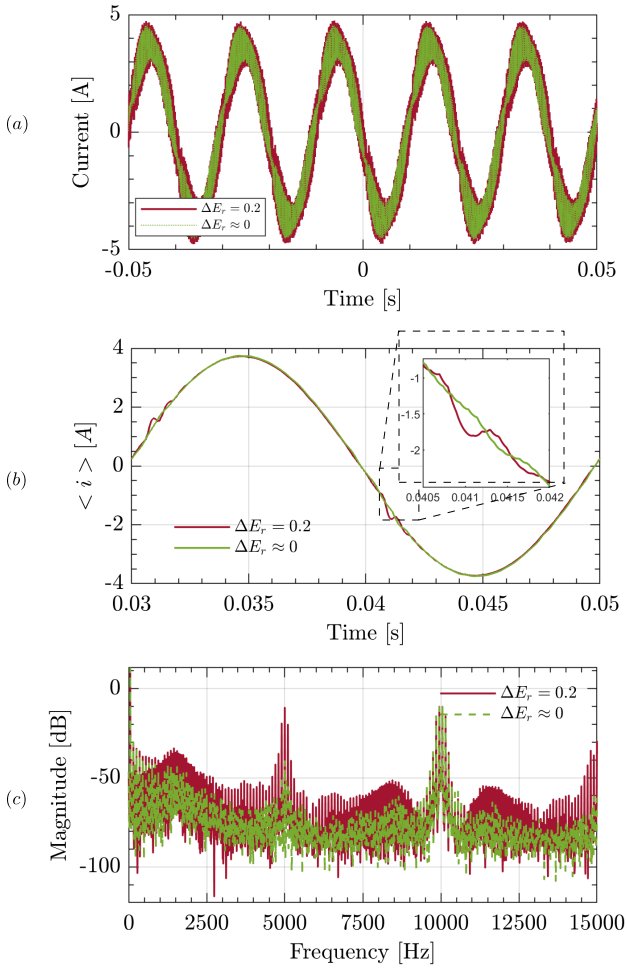

Fig. 20. Experimental results for the MC-VSC with $N = 2$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance from (3), and $\Delta E_r \in \{0, 0.2\}$, operated in the sinusoidal ac regime: time-domain waveforms of the inductor current (a) with and (b) without the switching ripple, and (c) spectra of the inductor current.

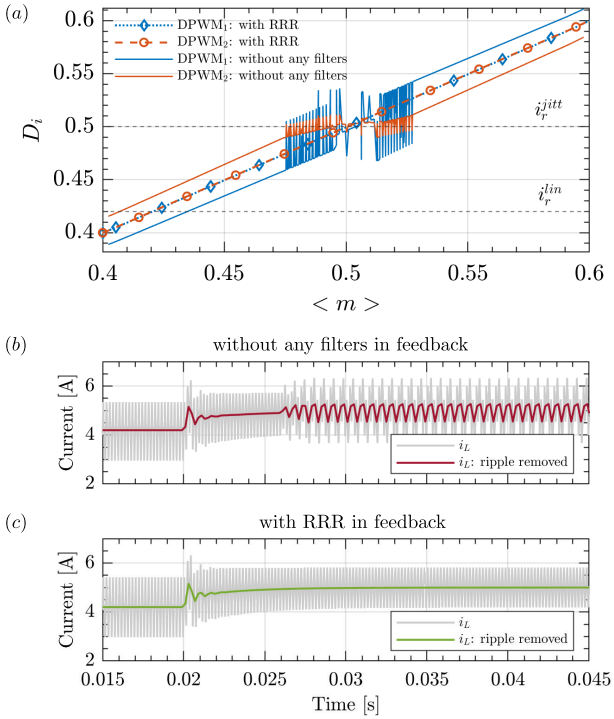

Fig. 21. Comparison of the simulation results for MC-VSC with $N = 2$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance from (3), and $\Delta E_r = 0.2$, in case without any filters in feedback and with RRR (a) modulator transcharacteristics around $D_c = (1/2)$ and (b) inductor current in response to the reference step change for the case (b) without any filters in feedback and (c) with RRR in feedback. In case without any filters, the imposed reference step change moves the operating point from linear to jitter zone, as indicated in (a).

as in Fig. 17(a), which is expected to cause distortion in ac operation. On the other hand, since MSMU-PS-DPWM yields linear operation under balanced conditions, the deadtime is expected to be the only source of distortion in ac operation with $\Delta E_r = 0$. To verify this, the time-domain waveforms of the inductor current and their spectra are compared in Fig. 20 for $\Delta E_r = 0.2$ and $\Delta E_r = 0$. For a better visualization, in Fig. 20(b) the switching ripple is removed from plotted data using an MAF over T_{pwm}. As expected, a considerable distortion around the voltage zero crossings occurs for $\Delta E_r = 0.2$, which is not present for $\Delta E_r = 0$. Note that the similar effects were observed in simulations with zero deadtime, which verifies that the origin of the distortion for $\Delta E_r = 0.2$ is the modulator nonlinearity.

VI. Conclusion

In this article, the discontinuity-related nonlinear effects of MSMU-PS-DPWM that arise in unbalanced MC-VSCs are analyzed. A simple analytical procedure is proposed to predict the nonlinear zones that appear in the transcharacteristic of each carrier. Their extension is verified to be proportional to the relative value of imbalance magnitude and crossover frequency, and inversely proportional to the number of cells. It is shown that due to PS-DPWM, vertical intersections in MSMU unbalanced MC-VSCs always cause LCOs. This phenomenon, which is more pronounced for higher control loop delays and bandwidths, deteriorates the performance of dc–dc and dc–ac MC-VSCs. Experimental measurements, performed on single-phase laboratory prototypes of the three- and four-level MC-VSCs, are in excellent agreement with the simulations and analytical predictions.

Appendix

To avoid detrimental impact of discontinuity-related nonlinear effects of MSMU-PS-DPWM that appear in unbalanced MC-VSCs, some provision has to be taken in practical applications. Since the modulator nonlinearity arises due to the switching ripple that gets sampled in presence of an imbalance between the cells, digital feedback filtering aimed at removing the ripple from the acquired feedback signal seems like a promising candidate. Though moving average filter over T_{pwm} is known to be effective in removing the switching ripple in multisampled applications, it compromises dynamic performance improvements that increased sampling frequency offers [17], [35], [41]. As an alternative, this article proposes repetitive ripple removal filter (RRR) from [36]. Its z-domain transfer function is

$$G_{\text{RRR}}(z) = \frac{(1+R)\left(1-\left(z^{-N_{\text{ms}}} - \frac{1}{N_{\text{ms}}}\sum_{q=1}^{N_{\text{ms}}} z^{-q}\right)\right)}{1-\left(z^{-N_{\text{ms}}} - \frac{1}{N_{\text{ms}}}\sum_{q=1}^{N_{\text{ms}}} z^{-q}\right)+R} \quad (12)$$

where R defines the settling time and the phase lag of the RRR [36]. In this article, $R = 0.125$ is used, such that

RRR's settling time is approximately $10T_{\text{pwm}}$ and that its impact on control loop's small-signal dynamics of interest is negligible [36].

To demonstrate the effectiveness of RRR in mitigating the nonlinear effects discussed in this article, simulations were run for MC-VSC with $N = 2$, $f_{cr} = 0.1$, $\tau_D = (1/N)$, imbalance from (3), and $\Delta E_r = 0.2$. Simulations were organized in the same way and with the same parameters as outlined at the beginning of Section IV-E. In Fig. 21(a), modulator transcharacteristics are compared for the case without any filters in feedback ($G_{fb}(z) = 1$) and with RRR ($G_{fb}(z) = G_{\text{RRR}}(z)$). As seen, RRR successfully eliminates nonlinear zones that are present when no filters are used, resulting in a completely linear behavior of MSMU-PS-DPWM, even in the presence of an imbalance. To further elaborate on this, a step reference change is imposed, so that, in the case without any filters, the operating point moves from the linear to jitter zone, as marked in Fig. 21(a). Inductor current waveforms in response to this reference change are shown in Fig. 21(b) and (c), in the case without any filters and with RRR in feedback. LCOs that are clearly observable in Fig. 21(b) are successfully eliminated by RRR, as seen in Fig. 21(c). This illustrates the effectiveness of RRR in mitigating the discontinuity-related nonlinear effects of MSMU-PS-DPWM and, consequently, in preventing their detrimental impact on the performance of unbalanced MC-VSCs.

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Ruzica Cvetanovic (Graduate Student Member, IEEE) was born in Belgrade, Serbia, in 1996. She received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, in 2019 and 2020, respectively. She is currently pursuing the Ph.D. degree with the Power Electronics Group, Department of Information Engineering, University of Padua, Padua, Italy.

From 2020 to 2021, she was with the Power Converters and Systems Group, School of Electrical Engineering, University of Belgrade. In 2021, she joined the Power Electronics Group, Department of Information Engineering, University of Padua, as a Visiting Researcher. Her current research interests include modeling and digital control of grid-tied power electronics converters.

Ivan Z. Petric (Member, IEEE) was born in Belgrade, Serbia, in 1994. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Belgrade, Belgrade, in 2017 and 2018, respectively, and the Ph.D. degree in electrical engineering from the University of Padua, Italy, in 2023.

From 2018 to 2019, he was a Researcher with the Power Electronics, Machines and Control Group, the University of Nottingham, Nottingham, U.K. In 2022, he was a Visiting Researcher with the Electrical Engineering and Computer Sciences Department, University of California, Berkeley, CA, USA. His current research interests include modeling and control of power converters, advanced modulation strategies, and grid-connected converters for renewable energy sources and smart microgrids.

Paolo Mattavelli (Fellow, IEEE) received the M.S. degree (Hons.) and the Ph.D. degree in electrical engineering from the University of Padua, Padua, Italy, in 1992 and 1995, respectively.

From 1995 to 2001, he was a Researcher at the University of Padua. From 2001 to 2005, he was an Associate Professor at the University of Udine, Udine, Italy, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padua, Vicenza, Italy, with the same duties. From 2010 to 2012, he was with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA. He is currently a Professor at the University of Padua. His current Google scholar h-index is 81. His major field of interests include analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and micro-grids, and high-temperature and high-power density power electronics. In these research fields, he has been leading several industrial and government projects.

Dr. Mattavelli served as an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2003 to 2012. From 2005 to 2010, he was the Industrial Power Converter Committee (IPCC) Technical Review Chair for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. From 2003 to 2009 and 2013 to 2015, he has been a Member-at-Large of IEEE Power Electronics Society's Administrative Committee. He also received the Prize Paper Award in IEEE TRANSACTIONS ON POWER ELECTRONICS in 2005, 2006, 2011, and 2012 and the 2nd Prize Paper Award at the IEEE Industry Application Annual Meeting, in 2007. He is an IEEE Fellow and the Co-Editor in Chief for IEEE TRANSACTIONS ON POWER ELECTRONICS.

Simone Buso (Member, IEEE) received the M.Sc. degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padua, Padua, Italy, in 1992 and 1997, respectively.

He is currently an Associate Professor of electronics with the Department of Information Engineering (DEI), University of Padua. His main research interests are in the industrial and power electronics fields and are related specifically to switching converter topologies, digital control of power converters, and renewable energy sources and smart micro-grids.

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