Modeling of Switching Power Losses in Cascaded H-Bridges With Unipolar PWM

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***Abstract*— This article studies the extraction of an equivalent resistance for calculation of the switching power losses in cascaded H-bridge (CHB) multilevel inverters with unipolar pulsewidth modulation. The concept of local and global root mean square (rms) currents and switching power losses is introduced in each H-bridge (HB) considering different frequencies of the inverter output and the switching network, i.e., transistor and diode. Energy conservation law has been used to show that the equivalent averaged local and global resistances for switching power losses are functions of load power factor angle, load rms current, and modulation index. This dependency is then reduced to only load rms current when the equivalent resistances are transformed to the inverter output branch based on the reflection rule. Consequently, a resistive model of switching power losses of the inverter is deduced, which depends neither on the knowledge of the physics of the switch nor on complicated nonlinear equations of the semiconductor devices and loop inductances. Double-pulse tests (DPTs) are conducted to acquire reliable data on the switching characteristics of the devices for different operating points.**

***Index Terms*— Energy efficiency, insulated-gate bipolar transistor (IGBT), inverters, metal-oxide-semiconductor field-effect transistor (MOSFET), pulsewidth modulation, switching loss.**

I. Introduction

SWITCHING and conduction losses of semiconductor devices account for a significant amount of losses in power electronics converters. Based on the converter topology, e.g., in voltage-source inverters (VSIs), dead-time voltage drop adds to the above-mentioned losses. The conduction voltage drop of each semiconductor device arises from its ON-state resistance and threshold voltage. On the other hand, switching and dead-time voltage drops are due to the devices' turn-on and turn-off delay times. These losses form a significant portion of the converter nonlinear effects, specifically at low voltages and, if not properly compensated, may deteriorate the converter performance [1], [2], [3]. In many applications, the inverter voltage drops are modeled as an equivalent resistance, and the difference between the real output voltage and the reference waveform is compensated by adding a relevant value to the reference in phase with the output current [1], [2], [4]. Furthermore, this equivalent resistance can be included in the averaged small-signal model of the converter for a more accurate understanding of the converter dynamics [5].

Thus, modeling of these losses is necessary for the purpose of optimum operation and control, thermal management, and efficiency estimation of converters. So far, various approaches were presented in the literature for the sake of estimation and compensation of semiconductor losses in power electronics converters, for example, [4], [6], [7], [8], [9], [10] to name a few. In some of these references, the integrated effect of conduction, switching, and dead time is estimated in the form of converter (mostly inverters) nonlinear characteristics through different tests such as the dc current test [1], [2], [4], [6], [7]. In other publications, for instance in [9], [10], and [11], the individual effect of dead time, parasitic capacitances, and conduction losses is estimated, respectively. The above-mentioned losses are functions of the modulation and switching scheme [11], [12], [13].

In [14], [15], [16], and [17], theoretical approaches were presented for the estimation of the switching power losses in conventional two-level inverters. In [18], numerous measurements were carried out to find the effective parameters in the switching loss model of two-level inverters and, then, the mathematical model of switching losses was extracted via curve-fitting. In multilevel converters, the individual model of each device of a neutral point clamped (NPC) multilevel inverter was obtained according to its datasheet [19], and then, the analysis of switching losses was performed based on the extracted model and extensive simulations under various modulation indices and power factor angles. However, the switching characteristics of the device from its datasheet are for specific working points and it cannot be applied "as is" to various permutations of contributing factors. A similar procedure was followed in [13], where massive calculations were conducted to compute the switching losses in an NPC multilevel inverter under different working conditions.

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In [20], conduction and switching losses of series- or parallel-connected H-bridges (HBs) were compared for the purpose of selecting appropriate multilevel cascaded HB (CHB) configuration. These losses were estimated under the condition of constant load voltage and varying current. However, the measurement or calculation procedure for losses was not addressed explicitly.

In this article, the equivalent resistance for switching losses of a generic multilevel CHB inverter is estimated, when a phase-shifted unipolar pulsewidth modulation (PS-UPWM) is used. According to the above explanations, in addition to the switching characteristics such as switching delay times, the switching losses of each individual device in inverters depend on the instantaneous current to be commutated, and hence, modulation algorithm, load power factor angle, and modulation index are the contributing factors to the switching losses of the power.

In this regard, in Section II, the linearized equations for the voltage and current waveforms of transistors and diodes during commutation transients are extracted based on unipolar PWM switching intervals. Contrary to dc–dc converters, the frequency of the switching network (i.e., low-side transistor and high-side freewheeling diode or vice versa in an inverter leg) and the inverter output frequency are different. Thus, to be able to extract the equivalent resistance of the inverter switching losses, this article proposes to use the concept of local and global root mean square (rms) and average currents. The local and global rms currents of the switches are derived in Section III to extract the equivalent averaged resistance of local and global switching power losses based on the energy conservation law. The materials described in this section are also beneficial to estimate the averaged equivalent resistance for the conduction power losses of the devices. In Section IV, an output resistance is derived for the CHB inverter using the reflection rule. In Section V, the double-pulse tests (DPTs) are conducted on the experimental rig to have an authentic perception of the device switching characteristics for different working conditions. Also, experimental studies are performed on a multilevel CHB to verify the correctness of the inverter's estimated output equivalent resistance. The discrepancies between the experiments and theoretical modeling approach are discussed in Section VI. The article is concluded by drawing some conclusions in Section VII.

II. Turn-On and Turn-Off Transients in the Switches of HB Inverter

The PS-UPWM is commonly used for switching the CHB multilevel converters. A single-phase CHB (SP-CHB) converter with n series-connected HBs requires n carrier signals, each one time-shifted $T_{\rm cr}/2n$ with respect to the adjacent one, with $T_{\rm cr}$ being the carrier period, resulting in uniform power distribution among HBs and their switches [21]. Assuming that all the four transistors in each series-connected HBs carry the same rms current and dissipate the same switching and conduction power losses, only one of the HBs can be considered for the succeeding investigations, as shown in Fig. 1.

Fig. 1(b) illustrates the mechanism of unipolar PWM in generating switching pulses for HB shown in Fig. 1(a).

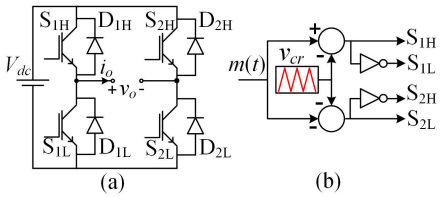

Fig. 1. Generic HB and its switching. (a) Circuit and (b) unipolar PWM.

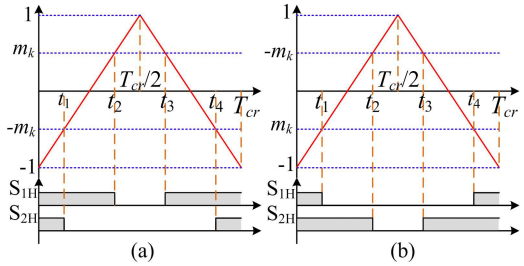

Fig. 2. Switching pulses in a period of carrier waveform for (a) $m > 0$ and (b) $m < 0$.

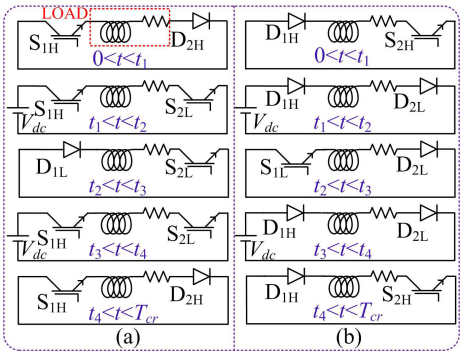

Fig. 3. HB equivalent circuit in the case of $m > 0$. (a) $i_o > 0$ and (b) $i_o < 0$.

The reference signal is sampled every half cycle or every cycle of the carrier in double-update-mode or single-update-mode modulators, respectively [21]. As shown in Fig. 2, the switching pulses for the transistors S_{1H} and S_{1L} are generated via comparison of the reference signal $m(t)$ with its corresponding carrier signal and those of switches S_{2H} and S_{2L} are produced through comparing the carrier with $-m(t)$, being $m(t) = M\sin(\theta = \omega_0 t)$, where ω_0 is the electrical pulsations of the output voltage and $M \in [0, 1]$ is the modulation index. The reference has been considered as constant within a period of the carrier in Fig. 2, being the reference frequency almost negligible compared with that of the carrier. The equivalent circuits for the HB are shown in Fig. 3 for the cases of $m > 0$, $i_o > 0$ [Fig. 3(a)] and $m > 0$, $i_o < 0$ [Fig. 3(b)]. In the following, the switching losses are computed for both the cases, where the same analysis can be extended to the two other cases, i.e., ($m < 0$, $i_o > 0$) and ($m < 0$, $i_o < 0$).

A. Case $m > 0$, $i_o > 0$

As it is obvious from Figs. 2(a) and 3(a), by commanding transistor S_{2L} at $t = t_1$, it turns on and the diode D_{2H} turns off. Assuming constant load current during the commutation process, i.e., $i_o = I_{\rm ok}$, one can draw the equivalent circuit of Fig. 4 for the HB. In Fig. 5(a) and (b), the approximate (linear) voltage and current waveforms of the transistor are shown

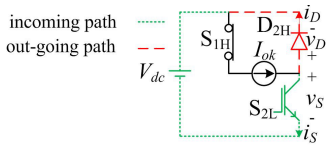

Fig. 4. HB equivalent circuit during the commutation between S_{2L} and D_{2H} ($t = t_1$).

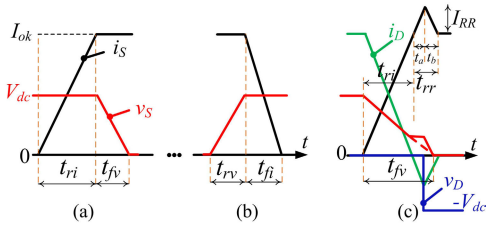

Fig. 5. Approximate (linear) voltage and current waveforms of switches in HB during (a) transistor turn-on, (b) transistor turn-off, and (c) transistor turn-on considering the diode reverse recovery.

for the turn-on and turn-off transients, respectively. Note that despite differences such as tail current in the turn-off transient of insulated-gate bipolar transistor (IGBT), the concepts of switching transients are the same for the IGBTs and metal-oxide-semiconductor field-effect transistors (MOSFETs) [22]. This will be explained in more detail in Section II-C.

Based on Fig. 5(a), during the turn-on transient, the switch current rises linearly to the load current in a period of $t_{\rm ri}$. Then, the voltage across the switch starts to reduce linearly during $t_{\rm fv}$. The total delay time, which contributes to the switching losses of the transistor, is $t_{d,\rm on} = t_{\rm ri} + t_{\rm fv}$. However, the switch turn-on transient is altered in practice due to the diode reverse recovery phenomenon and the displacement current of the gate-emitter (gate–source in MOSFET) and gate-collector (gate–drain in MOSFET) capacitances [23]. The practical waveform of a switch at turn-on is shown in Fig. 5(c). In a real case, when the gate-emitter voltage (or gate–source in MOSFET) exceeds the threshold voltage, the switch current rises and its voltage decreases. The rising interval of the transistor current to increase from 0 to $I_{\rm ok}$ lasts for $t_{\rm ri}$ during which the diode current falls from $I_{\rm ok}$ to 0. Within this period, due to the interaction between switch parasitic capacitances and the equivalent inductance seen from the device output capacitance (also called the loop inductance), the switch voltage plateaus at a fraction of dc-link voltage until the reverse recovery of the diode is finished [24]. On the other hand, as the diode current reaches zero, the reverse recovery current, $I_{\rm RR}$, flows through the diode for an interval of t_a. This current is added to the transistor current. Hereinafter, the diode is turned off and the voltage across the transistor reduces to nearly zero (saturation region). Note that in Fig. 5(c) usually $t_{\rm ri} + t_a < t_{d,\rm on} = t_{\rm fv} < t_{\rm ri} + t_{\rm rr}$.

Thus, according to Fig. 5(c), the currents of S_{2L} and D_{2H}, i.e., i_S and i_D, can be expressed by the following equations for the above-mentioned transient:

$$i_S = \begin{cases} \dfrac{I_{\rm ok} + I_{\rm RR}}{t_{\rm ri} + t_a} t, & 0 \le t \le t_{\rm ri} + t_a \\ \dfrac{-I_{\rm RR}}{t_b}(t - (t_{\rm ri} + t_{\rm rr})) + I_{\rm ok}, & t_{\rm ri} + t_a \le t \le t_{\rm ri} + t_{\rm rr} \\ I_{\rm ok}, & t \ge t_{\rm ri} + t_{\rm rr} \end{cases}$$

$$i_D = \begin{cases} -\dfrac{I_{\rm ok} + I_{\rm RR}}{t_{\rm ri} + t_a} t + I_{\rm ok}, & 0 \le t \le t_{\rm ri} + t_a \\ \dfrac{I_{\rm RR}}{t_b}(t - t_{\rm ri} - t_a) - I_{\rm RR}, & t_{\rm ri} + t_a \le t \le t_{\rm ri} + t_{\rm rr}. \end{cases} \tag{1}$$

In addition, the transistor and diode voltages, v_S and v_D, are

$$v_S = \frac{-V_{\rm dc}}{t_{\rm fv}}(t - t_{\rm fv}), \quad 0 \le t \le t_{d,\rm on} = t_{\rm fv}$$
$$v_D = \begin{cases} 0, & 0 \le t \le t_{\rm ri} + t_a \\ -V_{\rm dc}, & t_{\rm ri} + t_a \le t \le t_{\rm ri} + t_{\rm rr} \end{cases} \tag{2}$$

in which the switch voltage is approximated by the dashed line in Fig. 5(c).

Consequently, the instantaneous switching losses of the transistor turn-on, $p_{{\rm sw},S,\rm on}$, and the diode turn-off, $p_{{\rm sw},D,\rm off}$, can be calculated as the product of their voltage and current during the switching transient. Thus,

$$p_{{\rm sw},S,\rm on} = v_S i_S, \quad 0 \le t \le t_{\rm fv}$$
$$p_{{\rm sw},D,\rm off} = v_D i_D, \quad t_{\rm ri} + t_a \le t \le t_{\rm ri} + t_{\rm rr}. \tag{3}$$

At $t = t_2$ in Fig. 2(a), transistor S_{1H} turns off, and based on the load current polarity, diode D_{1L} turns on. In this regard, diagrams of Fig. 5(b) are drawn for the turn-off transient of S_{1H}. By removing the command pulse from the transistor, v_S increases to $V_{\rm dc}$ during $t_{\rm rv}$. Then, the current of S_{1H} commutates to D_{1L} during $t_{\rm fi}$. The transistor voltage and current equations during the turn-off transient are

$$i_S = \begin{cases} I_{\rm ok}, & 0 \le t \le t_{\rm rv} \\ \frac{-I_{\rm ok}}{t_{\rm fi}}(t - t_{\rm rv}) + I_{\rm ok}, & t_{\rm rv} \le t \le t_{\rm rv} + t_{\rm fi} \end{cases}$$
$$v_S = \begin{cases} \frac{V_{\rm dc}}{t_{\rm rv}} t, & 0 \le t \le t_{\rm rv} \\ V_{\rm dc}, & t_{\rm rv} \le t \le t_{\rm rv} + t_{\rm fi}. \end{cases} \tag{4}$$

Note that the voltage spike across the transistor is disregarded in (4) for the sake of simplicity. This will be discussed in detail in Sections II-C and VI. Similar to (3), the instantaneous switching loss of the transistor during turn-off interval is $p_{{\rm sw},S,\rm off} = v_S i_S$ for $0 \le t \le t_{\rm rv} + t_{\rm fi}$.

According to Figs. 2(a) and 3(a), at $t = t_3$, the switch S_{1H} turns on and D_{1L} turns off and, consequently, a transient period occurs similar to the one explained for $t = t_1$. Also, at $t = t_4$, S_{2L} turns off and D_{2H} turns on and the transient period is similar to the one started at $t = t_2$. Generally, for calculating the switching power loss for $m > 0$ and $i_o > 0$, one should note that switches S_{1H} and S_{2L} turn-on and turn-off once and diodes D_{1L} and D_{2H} turn-off once within a period of carrier waveform, i.e., two switching losses associated with the transistors and diodes in each carrier cycle. This will be later used in Fig. 9 for calculating the output equivalent resistance.

B. Case $m > 0$, $i_o < 0$

Similar to previous explanations in Section II-A, Figs. 2(b) and 3(b) indicate that switch S_{2H} turns on at $t = t_1$ and off at $t = t_4$. Also, S_{1L} turns on at $t = t_2$ and off

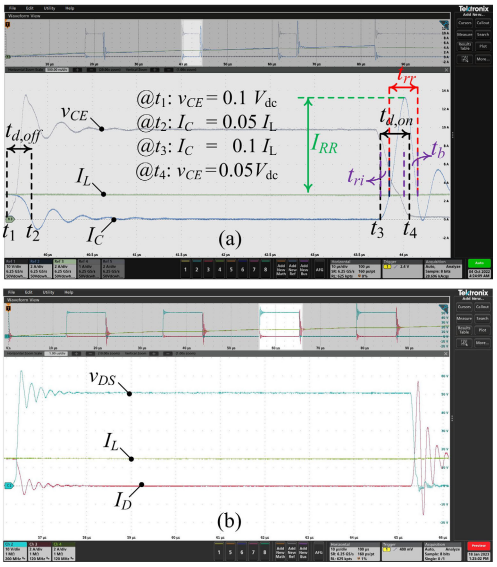

Fig. 6. Turn-off and turn-on transients for (a) IGBT (V_{CE}: collector–emitter voltage, I_C: collector current, I_L: inductive load current) and (b) MOSFET (V_{DS}: drain–source voltage, I_D: drain current, I_L: inductive load current).

at $t = t_3$. Regarding the diodes, D_{1H} and D_{2L} are turned off at $t = t_2$ and $t = t_4$, respectively.

It should be mentioned that the above explanations are completely the same when m is negative ($m < 0$). In fact, only the sequence of conducting switches differs while, in general, two transistors are turned on and off once and two diodes are turned off once during a switching period just as in the case of $m > 0$.

C. Experimental Waveforms of the Switching Transients for IGBT and MOSFET

To study the differences between the switching characteristics, two HBs with the same printed circuit board (PCB) layout—one with IGBT [25] and the other with MOSFET [26]—were tested. The basic design of the layouts is the same and some minor adjustments were made to optimize the driver circuit. Fig. 6 shows the switching transients for both the designs. Based on Fig. 6, the switching behavior during these intervals is the same for IGBT and MOSFET and corresponds to the theories presented in Section II-A. Both have voltage oscillations (ringing) across the switch, caused by the interaction between the switch capacitances and the loop inductances [24]. The amplitude of the voltage spike and the frequency of oscillations are different for IGBT and MOSFET because of the different rate of change in the switch current and the switch parasitic capacitances. At turn-off, the IGBT current falls rapidly first and then with a lower rate during the tailing interval and depends on component's technology [22]. Typically, in low-current applications (e.g., below 50 A), it contributes to a few percent of the turn-off loss. The experimental waveforms in Fig. 7 show that the tail current is not very relevant and decays to zero almost linearly. For high-current applications, the tail current is responsible for 15%–20% increase in the turn-off losses [27]. In such cases,

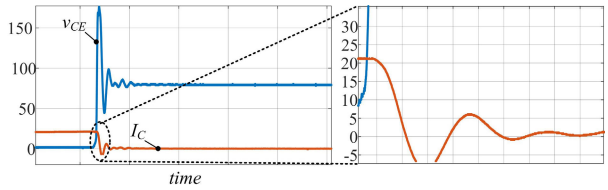

Fig. 7. Investigating the tail current at turn-off for the IGBT under test (no tail current is evident when the device is switched off close to its rated current).

TABLE I
CONDUCTING INTERVALS OF SWITCHES

	$m > 0$		$m < 0$	
	$i > 0$	$i < 0$	$i > 0$	$i < 0$
$0 < t < t_1$	S_{1H}, D_{2H}	D_{1H}, S_{2H}	S_{1H}, D_{2H}	D_{1H}, S_{2H}
$t_1 < t < t_2$	S_{1H}, S_{2L}	D_{1H}, D_{2L}	D_{1L}, D_{2H}	S_{1L}, S_{2H}
$t_2 < t < t_3$	D_{1L}, S_{2L}	S_{1L}, D_{2L}	D_{1L}, S_{2L}	S_{1L}, D_{2L}
$t_3 < t < t_4$	S_{1H}, S_{2L}	D_{1H}, D_{2L}	D_{1L}, D_{2H}	S_{1L}, S_{2H}
$t_4 < t < T_{cr}$	S_{1H}, D_{2H}	D_{1H}, S_{2H}	S_{1H}, D_{2H}	D_{1H}, S_{2H}

a piecewise linear approximation of the current can account for the tail current losses.

III. EXTRACTING THE EQUIVALENT SWITCHING RESISTANCE BASED ON ENERGY CONSERVATION LAW

There are some works dedicated to the identification of an equivalent resistance for the device switching and conduction losses in dc–dc converters based on the energy conservation law, such as [5], [28], [29]. In fact, they account for the losses during each switching period in the averaged small-signal model of the converter. The switching frequency in dc–dc converters is the same as the frequency of the switching network output, while these two frequencies are different in an HB. Consequently, to obtain an equivalent resistance representing the device switching and conduction losses in every output period, the concepts of local and global rms values of devices' currents are introduced in this section.

A. Local and Global RMS Currents of the Devices

The "local" (calculated for a period of carrier signal) rms values of the devices' currents can be calculated based on the conduction intervals of switches listed in Table I. Then, the "global" (calculated for a period of output voltage) rms values can be obtained based on the local ones.

Let us consider the output current as $i_o = I_o \sin(\omega_o t - \varphi)$, with I_o and φ being the amplitude and the power factor angle of load current, respectively. S_{1H}, D_{2H}, S_{2L}, and D_{1L} can conduct when the current is positive, i.e., $\varphi < \theta < \varphi + \pi$ (in this interval S_{1L}, D_{2L}, S_{2H}, and D_{1H} are constantly off). For $\varphi < \theta < \pi$, m and i_o are positive and the local rms current of the above-mentioned switches can be computed based on Fig. 2(a) and Table I. As in (5), t_1 and t_2 in Fig. 2(a) are obtained by intersecting the equations of both the carrier and reference waveforms in the interval of $0 < t < T_{cr}/2$

$$t_1 = \frac{T_{cr}}{4}(1 - m_k); \quad t_2 = \frac{T_{cr}}{4}(1 + m_k). \tag{5}$$

Accordingly, the local rms values of the currents in S_{1H}, D_{2H}, S_{2L}, and D_{1L} are calculated as in (6) for $m, i_o > 0$

$$I_{S_{1H},\text{rms},k} = \sqrt{\frac{2}{T_{\text{cr}}}\left(\int_0^{T_{\text{cr}}(1+m_k)/4} I_{\text{ok}}^2 dt\right)} = I_{\text{ok}}\sqrt{(1+m_k)/2}$$

$$I_{S_{2L},\text{rms},k} = \sqrt{\frac{2}{T_{\text{cr}}}\left(\int_{T_{\text{cr}}(1-m_k)/4}^{T_{\text{cr}}/2} I_{\text{ok}}^2 dt\right)} = I_{\text{ok}}\sqrt{(1+m_k)/2}$$

$$I_{D_{1L},\text{rms},k} = \sqrt{\frac{2}{T_{\text{cr}}}\left(\int_{T_{\text{cr}}(1+m_k)/4}^{T_{\text{cr}}/2} I_{\text{ok}}^2 dt\right)} = I_{\text{ok}}\sqrt{(1-m_k)/2}$$

$$I_{D_{2H},\text{rms},k} = \sqrt{\frac{2}{T_{\text{cr}}}\left(\int_0^{T_{\text{cr}}(1-m_k)/4} I_{\text{ok}}^2 dt\right)} = I_{\text{ok}}\sqrt{(1-m_k)/2}. \quad (6)$$

For $\pi < \theta < \pi + \varphi$, m is negative, i_o is positive and the local rms current of S_{1H}, D_{2H}, S_{2L}, and D_{1L} can be computed based on Fig. 2(b) and Table I. In this case, $t_1 = T_{\text{cr}}(1+m_k)/4$ and $t_2 = T_{\text{cr}}(1-m_k)/4$. Similarly, the devices' local rms currents are obtained in the same manner as the one in (6), and the final expression for the case of $m < 0$ and $i_o > 0$ is

$$I_{(S_{1H},\,S_{2L}),\text{rms},k} = I_{\text{ok}}\sqrt{(1+m_k)/2}$$
$$I_{(D_{1L},\,D_{2H}),\text{rms},k} = I_{\text{ok}}\sqrt{(1-m_k)/2}. \quad (7)$$

Following the same procedure, one can see that the current rms values for (S_{1L}, S_{2H}) and (D_{2L}, D_{1H}) are, respectively, identical to those of (S_{1H}, S_{2L}) and (D_{1L}, D_{2H}) in (7) for ($m > 0$, $i < 0$) and in (6) for ($m < 0$, $i < 0$), respectively.

In the next step, the global rms current is calculated. In this article, the squared local rms values are summed and averaged within an output period and its square root is represented as the global rms current. As mentioned earlier and shown via (6) and (7), local and eventually, global rms currents are the same for all the transistors and for all the diodes when unipolar modulation is used. Hence, S_{1H} and D_{2H} are taken as examples for the upcoming calculations. Here, it is assumed that the reference waveform, $m(t)$, and the load current are sampled in every carrier half-period (double-update mode). Thus, there are j sampling times within a half-period of output voltage, T_o, as follows:

$$j = \frac{0.5T_o}{0.5T_{\text{cr}}} + 1 = \frac{T_o}{T_{\text{cr}}} + 1. \quad (8)$$

On the other hand, every switch can conduct either positive or negative load current. Switches S_{1H} and D_{2H} can conduct within $\varphi < \theta < \pi + \varphi$. Based on the double-update-mode sampling strategy and considering the carrier waveform as in Fig. 8, angle φ coincides to the N_1th sample equal to $\lfloor \varphi \times j/\pi \rfloor$, where $\lfloor\rfloor$ indicates the floor function. Considering the reference signal as $m(t) = M\sin(\omega_o t)$ and the load current as $i_o = I_o\sin(\omega_o t - \varphi)$, the global rms current of S_{1H} and D_{2H} is obtained based on (6) and (7) as in (9). In fact, $A1$, $A2$, and $A3$ in (9) represent I_{ok}, $(1+m_k)/2$, and $(1-m_k)/2$ in (6), respectively,

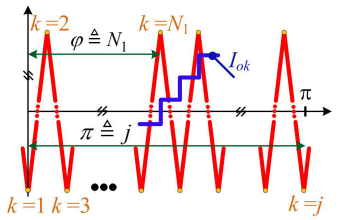

Fig. 8. Sampling the reference and load current in the double-update mode.

TABLE II
DEVICES' GLOBAL RMS CURRENTS OBTAINED FROM THEORETICAL APPROACH AND SIMULATIONS

	M	0.2	0.4	0.6	0.8	1
$I_{S,rms}$	Theoretical	11.43	12.03	12.82	13.45	13.97
$I_{S,rms}$	Simulation	11.51	12.13	12.9	13.51	14.12
$I_{D,rms}$	Theoritical	9.72	8.64	7.63	6.3	4.76
$I_{D,rms}$	Simulation	9.8	8.72	7.7	6.41	4.84

$$I_{S,\text{rms}}^2 = \left[\frac{1}{2j}\sum_{k=N_1+1}^{j+N_1} \underbrace{I_o^2\sin^2\left(\frac{2\pi T_{\text{cr}}}{T_o}(k-1) - \frac{N_1\pi}{j}\right)}_{A1} \times \underbrace{\left(\frac{1 + M\sin\left(\frac{2\pi T_{\text{cr}}}{T_o}(k-1)\right)}{2}\right)}_{A2}\right]$$

$$I_{D,\text{rms}}^2 = \left[\frac{1}{2j}\sum_{k=N_1+1}^{j+N_1} \underbrace{I_o^2\sin^2\left(\frac{2\pi T_{\text{cr}}}{T_o}(k-1) - \frac{N_1\pi}{j}\right)}_{A3} \times \underbrace{\left(\frac{1 - M\sin\left(\frac{2\pi T_{\text{cr}}}{T_o}(k-1)\right)}{2}\right)}_{A4}\right]. \quad (9)$$

To check the correctness of the proposed formulation, the rms value of the transistor current is listed in Table II obtained first from (9) and then from implementing SP-CHB in MATLAB/SIMULINK.[1] In this table, the load rms current, carrier frequency, and power factor angle are fixed at 21 A, 2 kHz, and 20°, respectively, and the modulation index is changing. A good matching is observable between the theoretical and simulation results even with relatively low sampling rate (2 kHz). Obviously, the precision of the proposed formulation enhances as the switching frequency increases. One important advantage of the proposed formulation is that the device current rating can be simply and promptly determined for different working points, while it takes plenty of time via simulations.

[1]Registered trademarked.

B. Local and Global Average Switching Power Losses

Using (1)–(4), the "local average switching power losses" of each transistor and diode, $P_{\mathrm{sw},S,k}$ and $P_{\mathrm{sw},D,k}$, are obtained by integrating the instantaneous switching losses, $p_{\mathrm{sw},S,\mathrm{on}}$, $p_{\mathrm{sw},S,\mathrm{off}}$, and $p_{\mathrm{sw},D,\mathrm{off}}$ in a period of carrier, T_{cr}, as follows:

$$P_{\mathrm{sw},S,k} = \frac{1}{2T_{\mathrm{cr}}} I_{\mathrm{ok}} V_{\mathrm{dc}} \left[\frac{t_{d,\mathrm{on}}}{3} \left(1 + \frac{I_{\mathrm{RR}}}{I_{\mathrm{ok}}} \right) + t_{d,\mathrm{off}} \right]$$
$$P_{\mathrm{sw},D,k} = \frac{1}{2T_{\mathrm{cr}}} I_{\mathrm{RR}} V_{\mathrm{dc}} t_b \tag{10}$$

where $t_{d,\mathrm{on}} = t_{\mathrm{fv}}$ and $t_{d,\mathrm{off}} = t_{\mathrm{fi}} + t_{\mathrm{rv}}$. Also, it is assumed that $t_{d,\mathrm{on}} \simeq t_{\mathrm{ri}} + t_a$ which is reasonable as will be explained in Section VI-B. $P_{\mathrm{sw},S,k}$ in (10) is the sum of local average turn-off and turn-on switching losses. Equation (10) shows that the transistor local average switching losses are dependent on the load current. Consequently, based on the energy conservation law, the local average switching losses in transistor and diode can be expressed as the power dissipated in an equivalent resistance [5], [28], $r_{\mathrm{sw},S,k}$ and $r_{\mathrm{sw},D,k}$ as follows:

$$r_{\mathrm{sw},S,k} = \frac{P_{\mathrm{sw},S,k}}{I^2_{S,\mathrm{rms},k}}; \qquad r_{\mathrm{sw},D,k} = \frac{P_{\mathrm{sw},D,k}}{I^2_{D,\mathrm{rms},k}} \tag{11}$$

where $I_{S,\mathrm{rms},k}$ and $I_{D,\mathrm{rms},k}$ are defined according to (6) and (7). On the other hand, just as in the case of device rms currents calculations, "global average switching losses" of each device can be defined by summing the local average switching losses in a period of output voltage by replacing I_{ok} in (10) by $I_o \sin(2\pi T_{\mathrm{cr}}(k-1)/T_o - N_1\pi/j)$. Consequently, global average switching power losses of each switch will be as in the following:

$$P_{\mathrm{sw},S} = \frac{1}{2j} \sum_{k=N_1+1}^{j+N1} P_{\mathrm{sw},S,k}(I_{\mathrm{ok}})$$
$$P_{\mathrm{sw},D} = \frac{1}{2j} \sum_{k=N_1+1}^{j+N1} P_{\mathrm{sw},D,k}(I_{\mathrm{ok}}). \tag{12}$$

Similar to the approach used for the extraction of local equivalent resistance, the device global equivalent average switching losses resistance, i.e., $r_{\mathrm{sw},S}$ and $r_{\mathrm{sw},D}$, can be obtained based on the energy conservation law as follows:

$$r_{\mathrm{sw},S} = \frac{P_{\mathrm{sw},S}}{I^2_{S,\mathrm{rms}}}; \qquad r_{\mathrm{sw},D} = \frac{P_{\mathrm{sw},D}}{I^2_{D,\mathrm{rms}}} \tag{13}$$

where the expressions for $I_{S,\mathrm{rms}}$ and $I_{D,\mathrm{rms}}$ are obtained from (9). Hence, these equivalent resistances can be connected in series with each switch model representing its switching power losses as shown in Fig. 9.

C. Equivalent Averaged Resistance of Conduction Power Losses

The instantaneous conduction power losses of transistors and diodes can be expressed as $p_{\mathrm{on},S} = r_{\mathrm{on},S} i_S \times i_S$ and $p_{\mathrm{on},D} = \left(V_F + r_{\mathrm{on},D} i_D\right) \times i_D$, respectively, where $r_{\mathrm{on},S(D)}$ is the switch ON-state resistance and V_F is the diode threshold voltage. Accordingly, the global averaged conduction power losses, $P_{\mathrm{on},S(D)}$, and their equivalent resistances, $r_{\mathrm{on},S}$ and $r_{\mathrm{on},D}$, are calculated as follows:

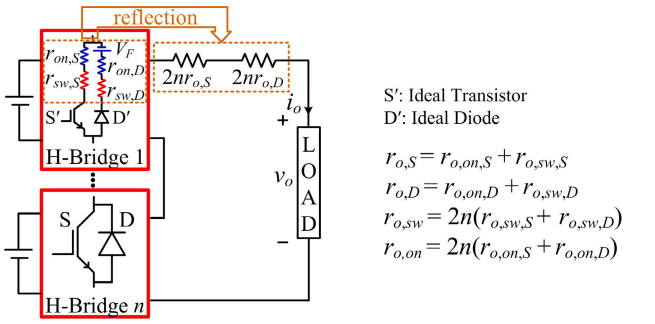

Fig. 9. Representation of devices' equivalent resistances in either series connection to the device or reflected at the inverter output.

$$P_{\mathrm{on},S} = \sum_k \frac{1}{T_{\mathrm{cr}}} \int_{T_{\mathrm{cr}}} p_{\mathrm{on},S,k} dt = r_{\mathrm{on},S} I^2_{S,\mathrm{rms}}$$
$$P_{\mathrm{on},D} = \sum_k \frac{1}{T_{\mathrm{cr}}} \int_{T_{\mathrm{cr}}} p_{\mathrm{on},D,k} dt = r_{\mathrm{on},D} I^2_{D,\mathrm{rms}} + V_F I_{D,\mathrm{rms}}. \tag{14}$$

IV. Estimation of Inverter Output Switching and Conduction Averaged Resistances Using Reflection Rule

In this article, the equivalent averaged resistances for switching and conduction power losses in switching devices are extracted. However, these resistances are functions of load power factor, load rms current, and modulation index. Modulation index and power factor are needed to obtain the switching times and the rms current during each period of the carrier, and the switching characteristics are required to obtain the local switching power losses. On the other hand, further investigations revealed that the reflected equivalent global resistance to the load branch in Fig. 9 is a function of load rms current, irrespective of power factor and modulation index. In fact, this resistance depends on the voltage and the current to be commutated, i.e., dc-link voltage and load current, switching frequency, and the switching characteristics of the device. Consequently, one may arrive at the interesting conclusion that the effect of switching and conduction losses can be modeled by adding equivalent averaged resistances at the inverter output. These conclusions are based on the assumption that the commutating current is continuous in each switching cycle (as it happens in continuous current mode (CCM) in dc–dc converters).

As shown in Fig. 9, the reflection rule can be applied to shift the devices' equivalent averaged resistances to the output terminals of the multilevel CHB. Using the reflection rule, the resistance r_x in branch "x" can be shifted to branch "y" with a resistance of r_y, where

$$r_y = r_x I_x^2 / I_y^2 \tag{15}$$

with I_x and I_y being the rms values of currents in branches "x" and "y," respectively. In Fig. 9, $r_{o,S}$ and $r_{o,D}$ are the transistors' and diodes' reflected resistances to the output, respectively,

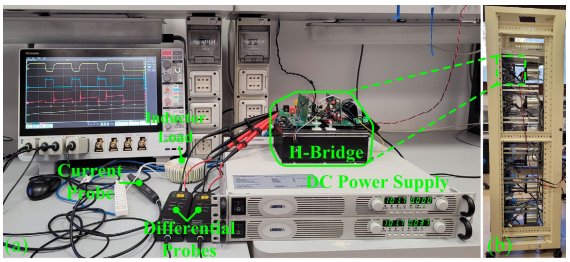

Fig. 10. Photograph of the experimental rig for (a) DPT on HB and (b) test on CHB.

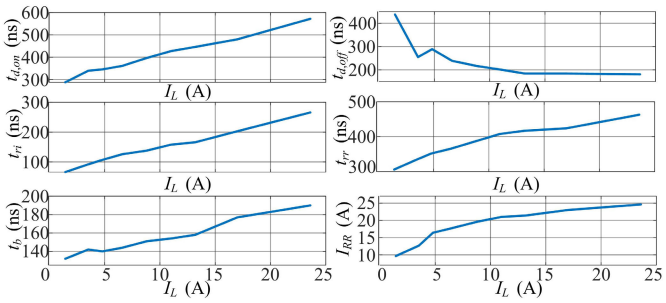

Fig. 11. Switching characteristics of IGBT and diode versus inductive load current, I_L, in DPT.

which, on their own, are the sum of reflected transistor or diode switching, $r_{o,sw,S(D)}$, and conduction, $r_{o,\text{on},S(D)}$, resistances given by the following equations:

$$r_{o,sw,S(D)} = \frac{r_{\text{sw},S(D)} I^2_{S(D),\text{rms}}}{\left(\frac{I_o}{\sqrt{2}}\right)^2}; \quad r_{o,\text{on},S} = r_{\text{on},S} I^2_{S,\text{rms}}$$
$$r_{o,\text{on},D} = \left(r_{\text{on},D} I^2_{D,\text{rms}} + V_F I_{D,\text{ave}}\right). \tag{16}$$

As shown in Fig. 9, the aforementioned resistances are reflected to the CHB output with a factor $2n$ for n series-connected HBs. This is due to the fact that in each HB, there are two switching and two conduction power losses associated with transistors and diodes during every switching period.

V. Experimental Studies

The DPT is used to extract the switching characteristics of the device under test (DUT). Then, the device's equivalent switching resistance is obtained based on the proposed method. DPT is a method to extract reliable data of the devices' switching characteristics, which are IGBT turn-on and turn-off delay times and diode reverse recovery characteristics at different operating conditions [30], [31]. Two pulses with adjustable duration are sent to the DUT, which is usually the lower switch of an HB phase leg, in a clamped inductive load circuit. Then, the devices' (IGBT or MOSFET and diode) transients are captured at the end of the first pulse and the beginning of the second pulse.

Since DPT results are very dependent on the circuit layout, one phase leg of the experimental HB shown in Fig. 10 was used for accurate estimation. The adopted HB, provided as the whole CHB, by DigiPower Ltd. [32], consisted of NGTB30N120LWG IGBTs and STTH6012W discrete diodes used in snubber circuits [25], [33]. For capturing the transients, a 500-MHz Tektronix MSO58 oscilloscope, 200-MHz Tektronix THDP0200 differential probes, and 120-MHz Tektronix TCP0030A current probes were used. The adopted instrumental setup gives satisfactory results for IGBTs as DUT in DPT. According to the device datasheet, the IGBT current rise time (t_{rise}) is up to 200 ns. Hence, the signal bandwidth (BW) would be BW $\simeq 0.35/t_{\text{rise}} \simeq 1.75$ MHz [31]. The minimum BW of the current probe should be three to five times higher than signal BW, which was 120 MHz in our case).

Fig. 6(a) shows a sample of waveforms from DPT to better explain the procedure to extract the switching characteristics, while Fig. 11 shows the DPT results for the IGBT and diode

TABLE III
Equivalent Global Switching Resistance in Ohms for IGBT

M	$\varphi = 0°$	$\varphi = 15°$	$\varphi = 30°$	$\varphi = 45°$	$\varphi = 60°$
0.1	0.243	0.244	0.246	0.249	0.253
0.3	0.210	0.212	0.217	0.225	0.235
0.5	0.185	0.187	0.194	0.205	0.220
0.9	0.149	0.152	0.160	0.173	0.194

TABLE IV
Equivalent Global Switching Resistance in Ohms for Diode

M	$\varphi = 0°$	$\varphi = 15°$	$\varphi = 30°$	$\varphi = 45°$	$\varphi = 60°$
0.1	0.137	0.1371	0.135	0.133	0.131
0.3	0.168	0.166	0.160	0.152	0.143
0.5	0.218	0.211	0.196	0.176	0.157
0.9	0.531	0.466	0.357	0.261	0.196

for different current levels. For the purpose of calculating the local switching losses based on (10), the varying switching characteristics for different load (commutation) currents can be stored in a lookup table and used in every switching period. This update of switching characteristics is necessary since the load current is sinusoidal and changing.

The equivalent global resistance of switching losses, $r_{\text{sw},S}$ and $r_{\text{sw},D}$, of the IGBT and diode is calculated based on the proposed numerical method and listed in Tables III and IV for the load rms current of 17 A and different power factor angles and modulation indices. In Tables III and IV, (I_o, f_{cr}, V_{dc}) = (17 Arms, 5 kHz, 500 V). It can be concluded from the results that $r_{\text{sw},S}$ increases as the power factor and modulation index decrease; on the contrary, $r_{\text{sw},D}$ decreases as the power factor and modulation index decrease. Moreover, the value of output equivalent resistance for switching losses of IGBT and diode, i.e., $r_{o,\text{sw},S(D)}$ in (16), is constant for different power factors and modulation indices and are equal to 65.7 and 31.3 mΩ, respectively. It is worth mentioning that the DUT equivalent switching resistance can be obtained quickly based on the proposed numerical method for various working conditions. The equivalent resistance for the switching losses of the experimental seven-level CHB is shown in Fig. 12 for different current levels.

For the purpose of experimental verification, the method presented in [31] and [34] has also been adopted in this article to verify the local average switching loss of IGBT and diode.

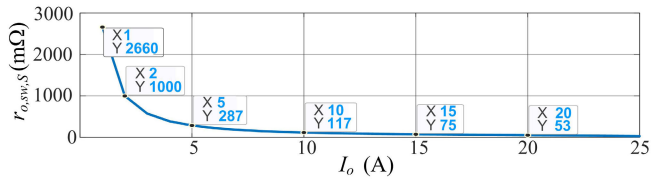

Fig. 12. Equivalent switching loss resistance of the seven-level CHB.

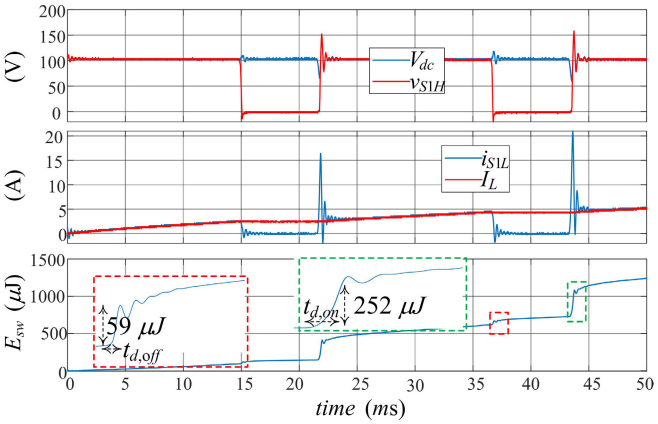

Fig. 13. Experimental waveforms to obtain the switching loss energy.

In DPT, the difference between the energy drawn from the power supply and the energy delivered to the inductive load during the switching intervals is equal to the switching losses, $E_{\rm sw}$, of IGBT and diode, i.e.,

$$E_{\rm sw} = \int_0^{t_d} \left(V_{\rm dc} i_{\rm S_{1L}} - v_{\rm S_{1H}} I_L\right) dt \tag{17}$$

where $i_{\rm S_{1L}}$ and $v_{\rm S_{1H}}$ are the current of lower switch (DUT) and the voltage of the upper switch (or load) during DPT, respectively. Also, t_d is the switching time. The energy transfer between the parasitic elements of the circuit (ringing) occurs after the switching interval defined in Fig. 6 and, thus, is not included in (17).

$E_{\rm sw}$ can be computed in the experiments via oscilloscope. For instance, Fig. 13 shows the math operation of (17) on the four channels of the oscilloscope. In this figure, the jump of the switching energy in the turn-on and turn-off transients at the current of 4.6 A and $V_{\rm dc} = 100$ V is equal to $59 + 252 = 311$ μJ. On the other hand, for the same operating conditions, the local average switching energy, i.e., $2T_{\rm cr}(P_{{\rm sw},S,k} + P_{{\rm sw},D,k})$ in (10), is computed equal to 295 μJ which is close to the experimental results. Comparisons for other current levels are shown in Table V. According to this table, a good matching can be observed between the experiments and the proposed numerical method.

To verify the proposed equivalent output resistance for the switching losses, i.e., the term $r_{o,sw}$ in Fig. 9, experimental studies were carried out using the seven-level CHB shown in Fig. 10(b). In the experiments, $V_{\rm dc} = 100$ V, $n = 3$, $f_{\rm cr} = 5$ kHz with PS-UPWM, and $M = 0.9$. Fig. 14 shows the output voltage and current waveforms when the load rms current is 7 A. In Table VI the experimental voltage drops with respect to the no-load condition, $\Delta v_{\rm exp}$, are compared against the presented theoretical ones, $\Delta v_{\rm th}$. For the purpose of fair

TABLE V

COMPARISONS BETWEEN NUMERICAL, $E_{\rm sw,NUM}$, AND EXPERIMENTAL, $E_{\rm sw,EXP}$, LOCAL SWITCHING ENERGY LOSS OF IGBT

I_L(A)	2.6	3.4	4.6	7	9.5
$E_{sw,num}$ (μJ)	184	244	295	379	403
$E_{sw,exp}$ (μJ)	209	263	311	419	517
I_L(A)	**12.7**	**15**	**17.3**	**20**	**23**
$E_{sw,num}$ (μJ)	606	741	846	1008	1113
$E_{sw,exp}$ (μJ)	655	769	893	1041	1186

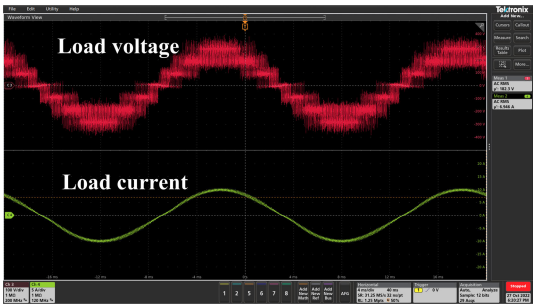

Fig. 14. Output voltage and current of the experimental seven-level SP-CHB.

TABLE VI

COMPARISON BETWEEN EXPERIMENTAL AND THEORETICAL VOLTAGE DROPS

$I_O[A]$	$r_{o,sw}$ [$m\Omega$]	$r_{o,on}$ [$m\Omega$]	Δv_{th} [V]	Δv_{exp} [V]
4.8	1126	588	8.23	8.5
7	920	500	9.92	10.8
9.2	756	454	11.13	12

comparison, first the experimental no-load voltage is captured and the fundamental component of this voltage is extracted via the FFT analysis of data in MATLAB, which is equal to 185 V for the above-mentioned conditions. It should be noted that the dead-time voltage drop, which is a function of $V_{\rm dc}$, $f_{\rm cr}$, and $(T_{dt} + t_{d,\rm on} - t_{d,\rm off})$ [11], is included. Therefore, by neglecting the changes in $(t_{d,\rm on} - t_{d,\rm off})$ with respect to dead-time duration, $T_{dt} = 2$ μs, one can assume the dead-time voltage drop as constant for different loading conditions. Table VI shows that the share of switching losses in the voltage drop is comparable to the conduction voltage drops which should be considered. Thus, the proposed modeling of switching losses is useful for appropriate compensation of inverter output voltage drop in some specific applications.

VI. DISCUSSION ON THE DISCREPANCIES BETWEEN THE EXPERIMENTS AND THEORETICAL MODELING

In the real world, the switching waveforms deviate from those presented in Section II-A mainly due to the interaction between the parasitic capacitances of the devices and the loop inductance during switching transients. In the following, the main sources of discrepancies are listed and explained with experimental evidence.

A. Voltage Spike Across the Switch at Turn-Off

The transistor experiences a voltage spike when its current reaches zero, which amplitude depends on the rate of change

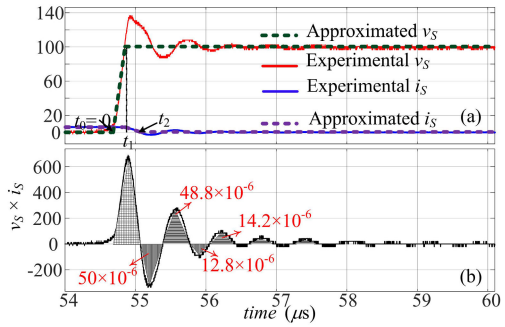

Fig. 15. Comparison between the analytical model of the transistor at turn-off and experimental waveforms. (a) Voltage and current and (b) experimental switching power losses.

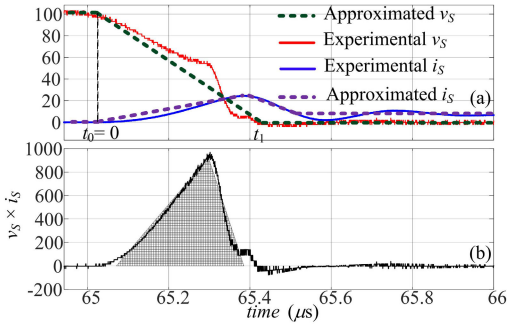

Fig. 16. Comparison between the analytical and experimental waveforms of the transistor at turn-on. (a) Voltage and current and (b) experimental switching power losses.

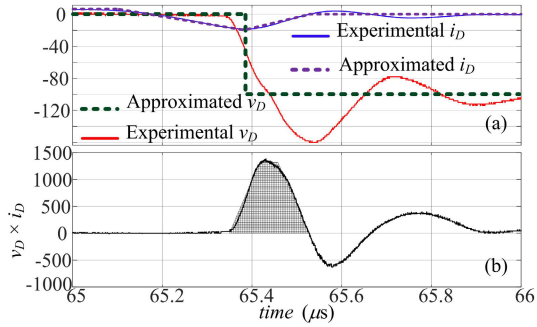

Fig. 17. Comparison between the analytical and experimental waveforms of the diode. (a) Voltage and current and (b) experimental switching power losses.

in switch current (di_S/dt) and loop inductance. An example of the experimental waveforms for the turn-off transient is shown in Fig. 15. In this figure, the experimental waveforms are linearized based on the theory presented in Section II-A. The linear equations of the device's current and voltage are

$$v_S = \begin{cases} 0.52 \times 10^9 t, & 0 < t < t_1 \\ 100, & t_1 < t < t_2 \end{cases}$$
$$i_S = \begin{cases} 6.2, & 0 < t < t_1 \\ -193.75 \times 10^6 t + 43.4, & t_1 < t < t_2. \end{cases} \quad (18)$$

By multiplying the above voltage and current and calculating the integral over $t_{d,\text{off}}$, the switching energy loss results equal to 70 μJ. Also, this multiplication is done in Fig. 15(b) and the surface area under the instantaneous power loss waveform in the desired period is equal to 75 μJ. It is interesting to note that the error is trivial, despite the relatively large voltage spike. This is due to the fact that the wave tail (after the peak) occurs when the current is zero. Furthermore, the duration of $(t_2 - t_1)$ is short compared with t_1, 32 ns versus 192 ns in this case.

B. Linear Approximation of the Switch Voltage and Current at Turn-On

Based on Fig. 5(c), the experimental waveforms of the switch's turn-on shown in Fig. 16(a) are approximated as in the following equations:

$$v_S = -243.55 \times 10^6 t + 100, \quad 0 < t < t_1 = t_{\text{fv}}$$
$$i_S = 59.42 \times 10^6 t, \quad 0 < t < t_1 = t_{\text{fv}}. \quad (19)$$

It should be mentioned that $t_{\text{fv}} \simeq t_{\text{ri}} + t_a$, and there is no need to use the linear approximation of the current for $t_{\text{ri}} + t_a < t < t_{\text{ri}} + t_{\text{rr}}$. The switch turn-on energy loss is obtained by multiplying voltage and current equations in (19) and taking the integral over t_{fv} which yields 167 μJ. The experimental waveform of the instantaneous power loss is also shown in Fig. 16(b) where the surface area under the waveform is nearly 180 μJ. In general, the sum of theoretical turn-on and turn-off switching energy loss is equal to 237 μJ while the experimental one is equal to 255 μJ. Accordingly, the error introduced by the approximations is around 7%.

C. Ringing

Ringing is due to the energy exchanges between the input source, parasitic resistances, and the energy storage elements of the circuit, i.e., the switches' parasitic capacitances and loop inductance [34], [35], [36]. However, in this article, the main purpose is to extract the converter equivalent resistance based on the average switching power losses. For better clarification, the instantaneous switching power losses during turn-off and turn-on transients are shown in Figs. 15(b) and 16(b), respectively. The ringing power during turn-off takes both negative and positive values which declares the power exchange between energy storage elements of the circuit. In Fig. 15(b), the resultant of energy exchange is negligible compared with the main turn-off energy loss. Also, according to Fig. 16(b), the ringing at turn-on transient is trivial.

D. Sudden Change in the Diode Voltage and the Voltage Spike Across the Diode at Turn-Off

The experimental voltage and current waveforms for the high-side body diode in DPT are shown in Fig. 17 together with the approximated plots, based on the analytical model presented in Section II-A. According to this figure, the real diode voltage does not change suddenly but at a very short period and it experiences a spike after reaching the input dc voltage. The approximated equations for the diode voltage and current shown in Fig. 17 are

$$v_S = -243.55 \times 10^6 t + 100, \quad 0 < t < t_1 = t_{\text{fv}}$$
$$i_S = 59.42 \times 10^6 t, \quad 0 < t < t_1 = t_{\text{fv}}. \quad (20)$$

Using (20), the approximated diode switching energy loss is equal to 118 μJ. On the other hand, based on Fig. 17(b), the experimental switching energy of the diode is equal to 133 μJ. Thus, the error is nearly 11% which is mainly due to the voltage spike. For a more accurate modeling, the voltage spike can also be considered. This voltage spikes can be extracted from the DPT and applied to the model if more accuracy is needed.

VII. Conclusion

The switching losses of individual devices in HBs depend on the modulation strategy, load power factor, switching frequency, and devices' switching characteristics. In this article, all these factors have been taken into account, and along with a combined theoretical and experimental approach, a switching loss model of the CHB multilevel converter has been obtained. In the theoretical part, the equivalent switching loss resistance of the devices is obtained based on the concept of energy conservation law and through the calculation of local and global switches' rms currents and average switching losses. Then, an output equivalent resistance is obtained based on the reflection rule which is only a factor of load current. The implementation of this theoretical proposal is very effective without the need to extensive simulation studies. In the experimental part, DPT is conducted to obtain the devices' switching characteristics for different switch operating conditions. This modeling approach can be extended to other PWM schemes such as bipolar PWM. In other words, the local and global rms values of the device current and switching losses can be obtained based on the specific type of PWM technique similar to the proposed approach.

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