Mitigation Technique for Cascaded H-Bridge Multilevel Inverters Based on Pulse Active Width Modulation

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***Abstract*— This article considers *l*-level cascaded H-bridge (CHB) inverters and proposes a new modulation method based on pulse active width modulation (PAWM), capable to minimize all harmonics with order $n < 2l + 1$ and to satisfy the European harmonic standards for medium-voltage-level applications EN 50 160 and CIGRE WG 36-05. A mathematical theorem and its proof are presented, stating the features of the procedure, which is an improvement of the selective harmonic elimination (SHE) PAWM proposed by Buccella *et al.* After a detailed description of the method, simulation and experimental results have been included, showing its capability to reduce low-order harmonics.**

***Index Terms*— Cascaded H-bridge (CHB) multilevel inverter, pulse active width modulation (PAWM), selective harmonic mitigation (SHM), total harmonic distortion (THD).**

I. Introduction

CASCADED H-bridge multilevel converters (CHB-MLCs) offer superior performance, flexibility, modularity, scalability, reduced filter requirements, simple design, and the possibility to implement redundancy. For such a reason, they are increasingly used in a variety of applications, including renewable energy conversion [1], grid-tied inverters [2], [3], high-voltage dc conversion (HVdc) [4], flexible ac transmission systems (FACTSs) [5], motor drives [6], and others.

In almost all applications, it is desirable to reduce the harmonic content from the outputs keeping total harmonic distortion (THD) within the imposed limits [7]. It is compulsory in grid-tied applications, because it can cause unacceptable disturbances to other equipment, adversely affecting overall operations; moreover, it reduces overall efficiency, produces heat, and increases the risk of failures [8]. Harmonic components cannot be completely eliminated from an electrical system, but, in the case of power converters, a proper modulation technique can significantly reduce their impact [3]. High switching frequency modulations reduce THD and offer high dynamics but at the cost of significant switching losses, thus reducing overall converter's efficiency. Low switching frequencies limit switching losses but at the cost of high harmonics content [9], [10], [11] and low dynamics. The latter could be a problem in some applications, but it is not an issue in large power drives or in power converters for the grid. Recently, power levels in the megawatt range are becoming common, and significant research efforts are devoted to the development of low-frequency modulation techniques [12], [13]. The paper [14] proposes an universal formulation of the selective harmonic elimination (SHE)-pulse width modulation (PWM) problem with half-wave symmetry and with the capability to find solutions without using predefined voltage waveforms, and [15] proposes an algebraic-numerical hybrid method capable to calculate the right switching angles in real time and without any requirement on the choice of the initial values. Other strategies provide harmonic cancelation through the use of magnetic coupling. For instance, [16] proposes a method for derivation of an optimal ripple injection strategy for multipulse rectifiers. The current THD was improved in comparison with the 12-pulse mode of operation, and the low-frequency line current harmonics were virtually eliminated. The paper [17] proposes a new modular multilevel converter (MMC) topology in which the fundamental and the second-order harmonic current ripple can be eliminated, as their induced magnetic fluxes are canceled in the coupled core. Power converter's density and efficiency can be significantly improved, since the capacitor size is much reduced. The paper [18] presents a large-power voltage source converter suitable for FACTS, which combines four three-level neutral point clamped inverters that share a common dc bus, by means of intermediate magnetic elements with low VA rating, capable to ensure an equal power sharing between the four inverters. Since they allow harmonic cancelation between inverter poles and eliminate any third harmonic created by the modulation, the output voltage waveform has high quality, and output filtering can be avoided. Using variable dc sources with pulse amplitude modulation (PAM), a higher number of harmonics will be deleted but at the cost of additional unknowns in mathematical formulation [19], [20]. The paper [21] proposes a middle-level SHE-PAM (ML-SHE-PAM) method that calculates the switching angles and synthesizes the reference voltage for the variable dc sources. The paper [22] proposes a new pulse active width modulation (PAWM) method and reports a mathematical proof demonstrating that all harmonics, except

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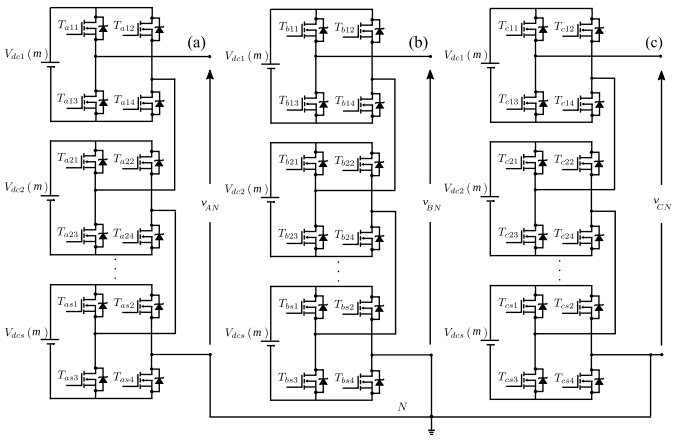


Fig. 1. Three phase l-level CHB inverter.

those of order $n = 2kl \pm 1$ being $k = 1, 2, \ldots$, disappear from the output voltage waveform of an l-level inverter. Further improvements of power quality can be obtained using selective harmonic mitigation (SHM) techniques, which scopes are to mitigate low-order harmonics while maintaining the same switching frequency [23].

To this purpose, this article proposes an SHM-PAWM algorithm, which improves the SHE-PAWM method proposed by Buccella *et al.* [22]. The new modulation works at fundamental switching frequency, minimizes all harmonics with order $n < 2l + 1$, and satisfies the European harmonic standards defined for medium-voltage-level applications. Section II describes the proposed SHM-PAWM. Section III includes some comparison among the proposed procedure and other methods. Section IV gives the experimental validation, while the conclusions are summarized in Section V.

II. Proposed SHM-PAWM

PAWM is a modulation at fundamental frequency applied to an l-level CHB inverter with $s = ((l-1)/2)$ H-bridges (see Fig. 1), in which both switching angles and a set of unequal dc voltage sources $V_{\mathrm{dc}i}$, $i = 1, \ldots, s$, are calculated, applying an interpolating criterion and not chosen as the unknowns of the problem [22].

The Fourier series expansion of output phase voltage $v_{\Gamma N}$, $\Gamma = A, B, C$, is

$$v_{\Gamma N}(\omega t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{1}{2k-1} \sum_{i=1}^{s} V_{\mathrm{dc}i} \times \cos((2k-1)\alpha_i) \sin((2k-1)\omega t). \quad (1)$$

The amplitude of the harmonic $(2k-1)$ is

$$F_{2k-1} = \frac{4}{\pi(2k-1)} \sum_{i=1}^{s} V_{\mathrm{dc}i} \cos((2k-1)\alpha_i) \quad (2)$$

where the values of α_i, $i = 1, 2, \ldots, s$, are the switching angles, and the values of $V_{\mathrm{dc}i}$, $i = 1, 2, \ldots, s$, are the dc voltage sources feeding the H-bridges.

The PAWM assumes a sinusoidal waveform at fundamental frequency ($f = 50$ Hz), called reference sinusoidal signal

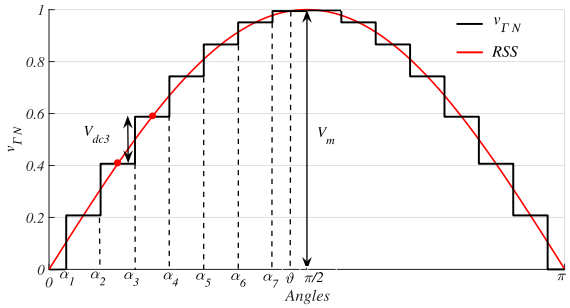


Fig. 2. Output phase voltage waveform $v_{\Gamma N}(\omega t)$ for a 15-level inverter.

(RSS) the modulating signal. Then, as shown in Fig. 2, the $V_{\mathrm{dc}i}$ dc sources are assumed, such that the obtained staircase output phase voltage intersects the RSS in the midpoints between two consecutive switching angles. Therefore, their amplitudes are given by

$$V_{\mathrm{dc1}} = V_m \sin\left(\frac{\alpha_1 + \alpha_2}{2}\right) \quad (3)$$

$$V_{\mathrm{dc}i} = V_m \left[\sin\left(\frac{\alpha_i + \alpha_{i+1}}{2}\right) - \sin\left(\frac{\alpha_{i-1} + \alpha_i}{2}\right)\right] \quad i = 2, \ldots, s-1 \quad (4)$$

$$V_{\mathrm{dc}s} = V_m \left[\sin\left(\frac{\alpha_s + \vartheta}{2}\right) - \sin\left(\frac{\alpha_{s-1} + \alpha_s}{2}\right)\right] \quad (5)$$

where $\vartheta = ((2s+1)\pi)/(2(l+1))$, and V_m is the peak value of the RSS shown in Fig. 2. The latter is assumed to be equal to 1 p.u. when the modulation index is $m = 1$.

While SHE-PAWM in [22] assumes the switching angles

$$\alpha_i = \frac{(2i-1)\pi}{2l}, \quad i = 1, \ldots, s \quad (6)$$

the SHM-PAWM proposed in this article assumes

$$\alpha_i = \frac{(2i-1)\pi}{2(l+1)}, \quad i = 1, \ldots, s. \quad (7)$$

Fig. 3 shows the switching pulses for phase A within the period $[0, 2\pi]$. Since the modulation technique works at fundamental switching frequency, only one pulse in a period is generated. Switching pulses for phases B and C can be obtained by applying a $\pm(2/3)\pi$ phase shift.

It will be demonstrated that the choice of the switching angles and of the unequal voltage sources (3)–(5) and (7) guarantees that the harmonics of order $n < 2l + 1$ satisfy the European voltage harmonic standards for medium-voltage-level applications [24], [25].

A. Mathematical Proof

Lemma 1: Given $F_n = (4/(n\pi)) \sum_{i=1}^{s} V_{\mathrm{dc}i} \cos(n(((2i-1)\pi)/(2(l+1))))$, where $n = 2k-1$, $k = 1, 2, \ldots, s = ((l-1)/2)$, $l \geq 5$ odd, and

$$V_{\mathrm{dc}i} = V_m \left[\sin\left(\frac{i\pi}{l+1}\right) - \sin\left(\frac{(i-1)\pi}{l+1}\right)\right], \quad i = 1, \ldots, s \quad (8)$$

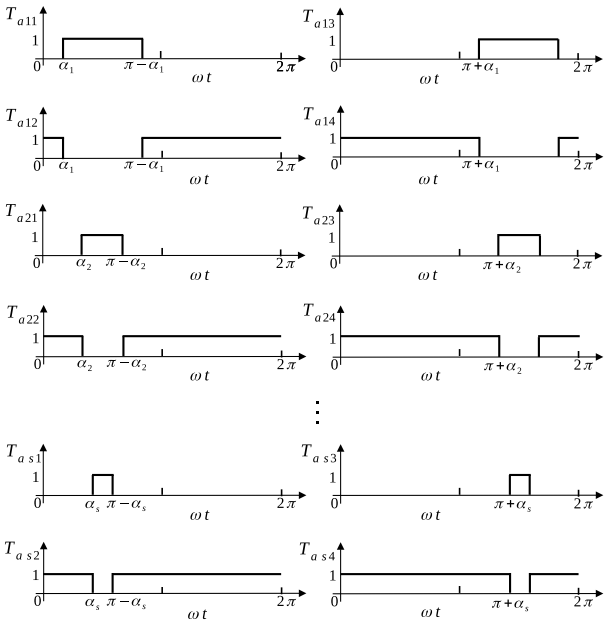


Fig. 3. Switching pattern for phase A in an l-level inverter in the period $[0, 2\pi]$.

then

$$|F_n| = \begin{cases} \dfrac{8V_m}{n\pi}\sin^2\left(\dfrac{\pi}{2(l+1)}\right)\left|\sin\left(\dfrac{n\pi}{2(l+1)}\right)\right|, \\ \qquad \text{if } n\pm 1 \neq 2k(l+1), \quad k=1,2,3,\ldots \\ \dfrac{4V_m}{n\pi}\sin\left(\dfrac{\pi}{2(l+1)}\right)\left|\dfrac{l-1}{2}+(-1)^k\cos\dfrac{\pi}{l+1}\right|, \\ \qquad \text{if } n\pm 1 = 2k(l+1), \quad k=1,2,3,\ldots \end{cases} \tag{9}$$

Proof: In (2), calling $n = 2k-1$, $k = 1, 2, 3, \ldots$, and substituting (7) follows:

$$F_n = \frac{4}{n\pi}\sum_{i=1}^{s} V_{\mathrm{dc}i}\cos\left(n\left(\frac{(2i-1)\pi}{2(l+1)}\right)\right). \tag{10}$$

Substituting (8) in (10) follows:

$$F_n = \frac{4V_m}{n\pi}\sum_{i=1}^{s}\left[\sin\left(\frac{i\pi}{l+1}\right)-\sin\left(\frac{(i-1)\pi}{l+1}\right)\right] \times\cos\left(n\frac{(2i-1)\pi}{2(l+1)}\right) \tag{11}$$

and applying Prosthaphaeresis and Werner formulas

$$\begin{aligned} F_n &= \frac{4V_m}{n\pi}\sin\left(\frac{\pi}{2(l+1)}\right)\sum_{i=1}^{s}\left[\cos\left((n+1)\frac{(2i-1)\pi}{2(l+1)}\right)\right. \\ &\qquad \left.+\cos\left((n-1)\frac{(2i-1)\pi}{2(l+1)}\right)\right] \\ &= \frac{4V_m}{n\pi}\sin\left(\frac{\pi}{2(l+1)}\right)(S_{n+1}+S_{n-1}) \end{aligned} \tag{12}$$

where $S_{n\pm1} = \sum_{i=1}^{s}\cos((n\pm1)((2i-1)\pi/(2(l+1))))$ with $S_0 = s$.

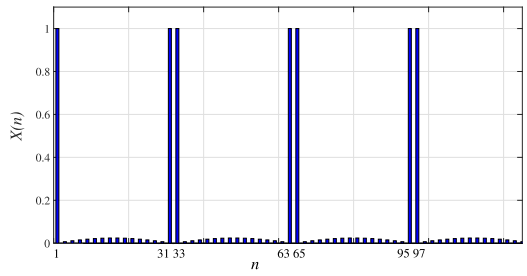


Fig. 4. $|(S_{n+1}+S_{n-1})/(S_2+S_0)|$ for a 15-level CHB inverter.

The goal is to find the values of n, such that $F_n \le l_n$, where the values of l_n are the levels resulting from the fulfillment imposed by the grid code requirements. The following equality holds [22]:

$$\begin{aligned} S_{n\pm1} &= \sum_{i=1}^{s}\cos\left((n\pm1)\frac{(2i-1)\pi}{2(l+1)}\right) \\ &= \begin{cases} \dfrac{1}{2}\sin\left(\dfrac{(n\pm1)(l-1)\pi}{2(l+1)}\right)/\sin\left(\dfrac{(n\pm1)\pi}{2(l+1)}\right), \\ \qquad \text{if } n\pm1 \neq 2k(l+1), \quad k=1,2,3,\ldots \\ (-1)^{\frac{n\pm1}{2}}s, \quad \text{otherwise, if } n\pm1 \neq 2k(l+1), \\ \qquad k=1,2,3,\ldots, \text{ then.} \end{cases} \end{aligned} \tag{13}$$

$$\begin{aligned} s_{n\pm1} &= \frac{1}{2}\sin\left(\frac{(n\pm1)(l-1)\pi}{2(l+1)}\right)\Big/\sin\left(\frac{(n\pm1)\pi}{2(l+1)}\right) \\ &= \frac{1}{2}\sin\left((n\pm1)\frac{\pi}{2}-\frac{(n\pm1)\pi}{(l+1)}\right)\Big/\sin\left(\frac{(n\pm1)\pi}{2(l+1)}\right). \end{aligned} \tag{14}$$

Therefore

$$\begin{aligned} S_{n\pm1} &= \frac{-\frac{1}{2}\cos\left((n\pm1)\frac{\pi}{2}\right)\sin\left((n\pm1)\frac{\pi}{(l+1)}\right)}{\sin\left(\frac{(n\pm1)\pi}{2(l+1)}\right)} \\ &= \frac{(-1)^{\frac{(n\pm1)}{2}+1}}{2}\sin\left(\frac{(n\pm1)\pi}{(l+1)}\right)\Big/\sin\left(\frac{(n\pm1)\pi}{2(l+1)}\right) \end{aligned} \tag{15}$$

$$S_{n+1}+S_{n-1} = 2(-1)^{\frac{n+1}{2}}\sin\left(\frac{\pi}{2(l+1)}\right)\sin\left(\frac{n\pi}{2(l+1)}\right). \tag{16}$$

If $n\pm1 = 2k(l+1)$, $k = 1, 2, 3, \ldots$, then

$$S_{n+1}+S_{n-1} = (-1)^{\frac{n\pm1}{2}}\left[s+(-1)^k\cos\left(\frac{\pi}{l+1}\right)\right]. \tag{17}$$

The function $|S_{n+1}+S_{n-1}|$ is periodic of $2k(l+1)$, with $k = 1, 2, 3, \ldots$ From (17), for $n = 2k(l+1)\pm1$ follows that it assumes values greater than $(s-1)$ that are much greater than those assumed in the others n values. As an example, as shown in Fig. 4, for a 15-level CHB inverter, the function $X(n) = |(S_{n+1}+S_{n-1})/(S_2+S_0)|$ is periodic with period 32, i.e., $X(n) = X(n+32k)$, $k = 1, 2, \ldots$

Substituting (16) or (17) in (10), it follows (9). ■

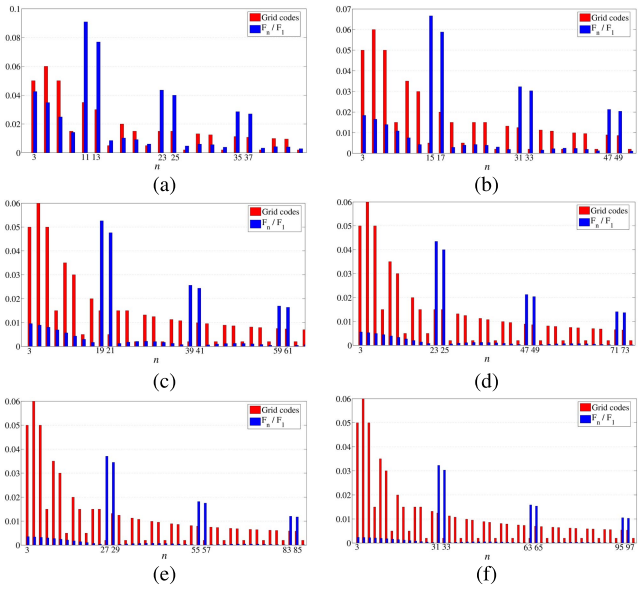


Fig. 5. $|(F_n/F_1)|$ in the single-phase CHB inverter. (a) 5 level. (b) 7 level. (c) 9 level. (d) 11 level. (e) 13 level. (f) 15 level.

TABLE I
GRID CODES EN 50 160 AND CIGRE WG 36-05

ODD HARMONICS				EVEN HARMONICS	
Not multiple of 3		Multiple of 3			
n	l_n (%)	n	l_n (%)	n	l_n (%)
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.5	6....10	0.5
13	3	21	0.5	>10	0.2
17	2	>21	0.2		
19	1.5				
23	1.5				
25	1.5				
>25	0.2+32.5/n				

From (9), it is possible to observe that, depending on n, the behavior of the numerator of $|F_n|$, when $n\pm1 \neq 2k(l+1), k = 1, 2, 3, \ldots$, is periodic with period $2k(l+1)$.

The behaviors of the ratios $|(F_n/F_1)|$ are shown in Fig. 5, which include the limits l_n of the European code requirements [24], [25], summarized in Table I.

It can be observed that, for $n < 2l + 1$, the quantities $|(F_n/F_1)|$ satisfy the European harmonic standards for medium-voltage-level applications.

III. COMPARISON WITH OTHER METHODS

The percent THD factor THD% is defined as

$$\text{THD\%} = \frac{\sqrt{\sum_{k=3,5,\ldots}^{49} F_k^2}}{F_1} \cdot 100 \tag{18}$$

where F_k and F_1 are the amplitudes of the kth and of the fundamental harmonics, respectively. The THD% of the output phase voltage obtained using the proposed method is compared

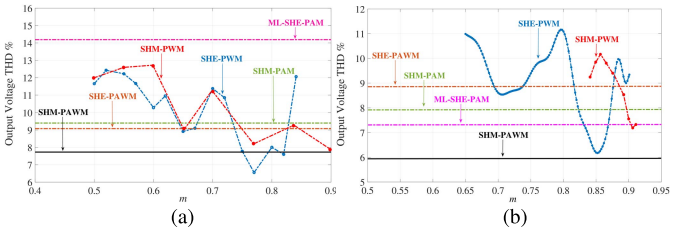


Fig. 6. THD% in a three-phase CHB inverter. (a) Seven level. (b) Nine level.

with those obtained using the following fundamental switching frequency techniques:

1) SHM-PWM mitigating low-order harmonics in [13] and [26];
2) SHE-PWM eliminating low-order harmonics in [13];
3) SHM-PAM mitigating low-order harmonics, assuming dc voltage sources depending on modulation index in [20] and [23];
4) ML-SHE-PAM eliminating all harmonics except those of order $2(l-1)k \pm 1, k = 1, 2, \ldots$, in [21];
5) SHE-PAWM eliminating all harmonics except those of order $2lk \pm 1, k = 1, 2, \ldots$, in [22].

Fig. 6(a) and (b) compares THD% results obtained by previously listed methods using three-phase seven-level or nine-level CHB inverters, respectively. It is possible to observe that the proposed technique always returns lower THD% than the other methods. Only around $m = 0.77$, the SHE-PWM technique, applied to a seven-level inverter, returns lower THD%.

With a three-phase seven-level CHB inverter, SHE-PWM deletes the fifth and seventh harmonics within the modulation index interval $m = [0.5, 0.84]$; SHM-PWM mitigates the 5th, 7th and 11th harmonics within the interval: $m = [0.5, 0.9]$ [13]. By applying the SHE-PAWM, the 5th, 7th, and 11th harmonics are deleted [22]; the ML-SHE-PAM cancels the fifth and seventh harmonics [21]. With the proposed SHM-PAWM, the mitigated harmonics are the 5th, 7th, 11th, and 13th. When applied to the nine-level CHB inverter, the SHE-PWM deletes the 5th, 7th, and 11th harmonics within the interval $m = [0.65, 0.9]$; the SHM-PWM mitigates the 5th and 7th and minimizes the THD within the interval $m = [0.84, 0.92]$ [26]. The SHE-PAWM deletes the 5th, 7th, 11th, and 13th harmonics [22]; using the ML-SHE-PAM, the 5th, 7th, 11th, and 13th harmonics are canceled [21]. The proposed SHM-PAWM reduces the 5th, 7th, 11th, 13th, and 17th harmonics.

As shown in Fig. 7(a), with a single-phase l-level inverter, the proposed SHM-PAWM always returns lower THD than SHE-PAWM and ML-SHE-PAM. In three-phase configurations, THD% is fluctuating, due to the automatic cancelation of the third harmonic and its multiples, as shown in Fig. 7(b).

If $(2l-1)$ is not multiple of 3, using the SHM-PAWM, the first not mitigated harmonic is the $(2l+1)$th if $(2l+1)$ is not multiple of 3, or the $(2l+3)$th if $(2l+1)$ is multiple of 3. Instead, using the SHE-PAWM, the first not canceled harmonic is the $(2l-1)$th, for instance, using the SHM-PAWM and a 15-level inverter THD% = 4.16. The first not mitigated

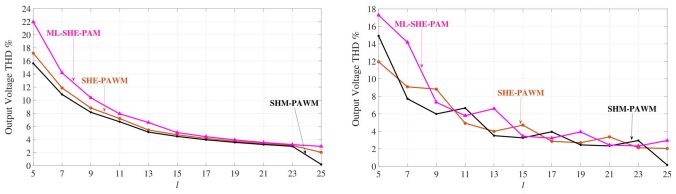


Fig. 7. THD% in l-level CHB inverters depending on the number of levels and considering up to the 49th harmonic. (a) Single phase. (b) Three phase.

TABLE II

THD% OBTAINED BY THE SHM-PAWM AND SHE-PAWM IN [22] FOR SINGLE-PHASE (SF) AND THREE-PHASE (TF) l-LEVEL CHB INVERTERS, CONSIDERING UP TO THE 301th HARMONIC

	THD%			
	SHM-PAWM		SHE-PAWM	
l	SF	TF	SF	TF
5	16.45	15.76	18.14	12.80
7	11.69	8.43	12.84	9.87
9	9.13	6.95	9.92	9.92
11	7.49	7.45	8.07	5.85
13	6.36	4.63	6.80	5.13
15	5.43	4.16	5.88	5.88
17	4.88	4.87	5.15	3.74
19	4.37	3.18	4.58	3.43
21	3.94	2.95	4.14	4.14
23	3.61	3.60	3.76	2.74
25	3.30	2.39	3.46	2.58
27	3.06	2.27	3.17	3.17
29	2.86	2.85	2.95	2.14
31	2.64	1.92	2.72	2.02
33	2.48	1.84	2.56	2.56

harmonic is the 31th, being the 33th automatically canceled. With a 17-level inverter, THD% = 4.87, and the first not mitigated harmonics are the 35th and 37th, both not multiple of three. Therefore, the latest case returns higher THD%. Notice that, for this reason, when $l = 11, 17, 23, 29, 35, \ldots$, the proposed procedure returns similar THD values both in single- and three-phase inverters. Table II shows the THD% obtained with the proposed SHM-PAWM and SHE-PAWM in [22] for both a single-phase and a three-phase l-level CHB inverter, considering up to the 301th harmonic. Table III shows the first not mitigated harmonics in a single-phase, l-level, CHB inverter using the proposed procedure and the first not eliminated harmonics with the one in [22] and with the ML-SHE-PAM in [21]. The proposed method increases the order of the first mitigated harmonic, hence allowing the use of lighter and cheaper output filters. Using the proposed SHM-PAWM with a 25-level inverter and considering the first 49th harmonics, THD is zero. The behaviors of a five-level inverter with symmetrical load until $t = 40$ ms and asymmetrical load since $t = 40$ ms have been considered in two distinct situations. Case #1: unbalancing in phase "C"; Case #2: unbalancing in phase "B" and phase "C." Table IV resumes the values of the resistances and inductances in imbalanced loads. Fig. 8(a) shows voltage waveforms before and after a load step for

TABLE III

FIRST NOT MITIGATED HARMONICS (x) USING THE PROPOSED SHM-PAWM AND FIRST NOT ELIMINATED HARMONICS WITH THE SHE-PAWM (o) OR ML-SHE-PAM (+), CONSIDERING A SINGLE-PHASE CHB l-LEVEL INVERTER

	l											
n	5		7		9		11		13		15	
3												
5												
7	+											
9	+	o										
11		o	x	+								
13			x	+	o							
15	+				o	x	+					
17	+					x	+	o				
19		o						o	x	+		
21		o							x	+	o	
23	+		x	+							o	x
25	+		x	+							x	+
27					o							o
29		o			o							x
31	+	o				x	+					
33	+					x	+					
35			x	+				o				
37			x	+				o				
39	+	o					x	+				
41	+	o			o			x	+			
43					o				o			
45									o			
47	+		x			x	+					
49	+	o	x	+		x	+					

Case #1. Similar voltage behaviors were obtained in Case #2. Fig. 8(b) and (c) shows current waveforms during the time interval [0, 80] ms in Case #1 and Case #2, respectively. PAWM algorithms eliminate or mitigate more low-order harmonics than SHE-PWM. Consequently, they allow a reduction of the size of the output filter, decreasing cost and weight, and increasing efficiency; moreover, using a high number of levels, the output filter can be avoided. High efficiency is already ensured, because the proposed modulation works at fundamental switching frequency and with fixed angles, which do not depend on the modulation index. Since the variable dc link voltages required by the PAM method are provided by dc/dc converters, the proposed technique can be used at almost no cost in photovoltaic energy systems, battery energy storage systems (BESSs), or uninterruptable power supply (UPS) applications, which use dc/dc converters regardless of the adopted modulation technique. In conventional modulations, instead, for instance, PWM, switching angles depend on modulation index. Therefore, the duty cycle depends on m, and consequently, also, the losses and the efficiency are the functions of m.

IV. EXPERIMENTAL RESULTS

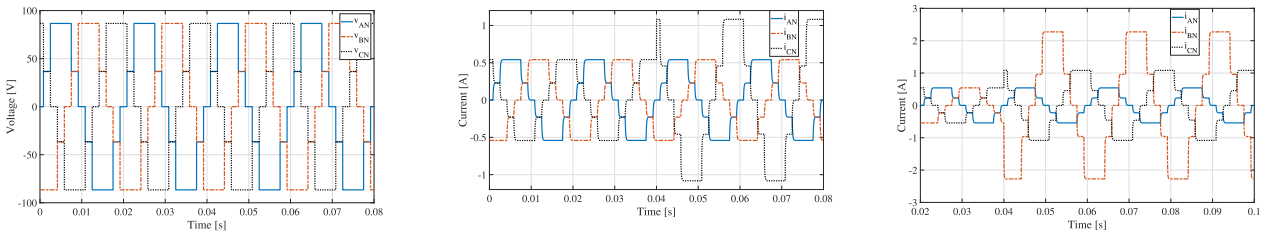
To further validate the proposed mitigation technique, an experimental setup, which can be configured as a single- as well as a three-phase CHB-MLC, was assembled using

TABLE IV
IMBALANCED LOAD IN FIVE-LEVEL INVERTER

V_{dc1} [V]	V_{dc2} [V]	imbalanced load	$Z_A = R_A + j\omega L_A$		$Z_B = R_B + j\omega L_B$		$Z_C = R_C + j\omega L_C$	
		at $t = 40$ms	R_A [Ω]	L_A [mH]	R_B [Ω]	L_B [mH]	R_C [Ω]	L_C [mH]
50	36.6	Case #1	160	18.5	160	18.5	80	5
		Case #2	160	18.5	39	2.2	80	5

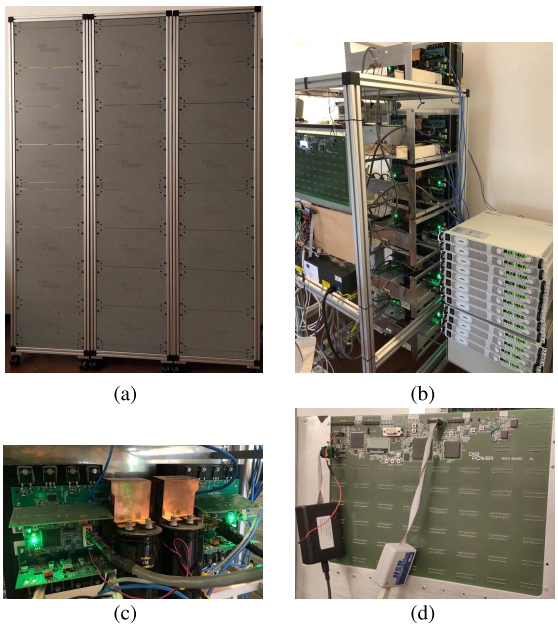
TABLE V
SWITCHING ANGLES AND DC VOLTAGE SOURCES

5-level		7-level		9-level		11-level		13-level	
α_i[rad]	V_{dci}[V]	α_i[rad]	V_{dci}[V]	α_i[rad]	V_{dci}[V]	α_i[rad]	V_{dci}[V]	α_i[rad]	V_{dci}[V]
0.2618	50.0	0.1964	38.3	0.1571	30.9	0.1309	25.9	0.1122	22.3
0.7854	36.6	0.5891	32.4	0.4712	27.9	0.3927	24.1	0.3366	21.1
		0.9818	21.7	0.7854	22.1	0.6545	20.7	0.5610	19.0
				1.0996	14.2	0.9163	15.9	0.7854	15.8
						1.1781	1.0	1.0098	11.9
								1.2342	7.4



(a) (b) (c)

Fig. 8. Output waveforms. (a) Voltage. (b) Current in Case #1. (c) Current in Case #2.



(a) (b) (c) (d)

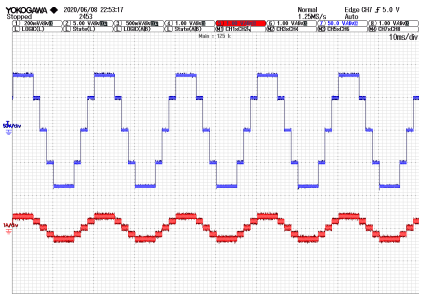
Fig. 9. Experimental setup. (a) 48 H-bridge converter. (b) Rear view of the system. (c) Couple of H-bridges. (d) Control board.

H-bridge cells and a control board developed by DigiPower Ltd. [27]. The test rig is shown in Fig. 9. In particular, Fig. 9(a) and (b) shows the whole converter consisting of 48 H-bridge cells as those shown in Fig. 9(c) and the control board shown in Fig. 9(d). The latter includes one Cyclone V and one MAX 10 field programmable gate array (FPGA). Modulation algorithms were written in very high speed integrated circuit hardware description language (VHDL) using Altera Quartus software [29] and then uploaded on the FPGA, which executes the modulation algorithm in real time and sends the command signals to each H-bridge through a bidirectional serial peripheral interface (SPI).

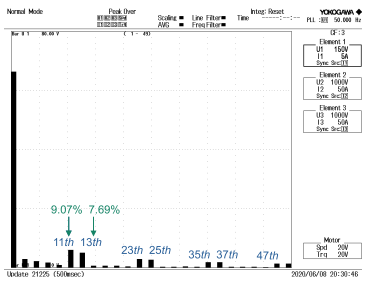
The system is highly complex and reconfigurable, and its features are used only in part in this application. Each H-bridge cell includes four STW75NF20 MOSFETs, rated 200 V, 75 A [27] and was supplied by a Lambda GEN600-2.6 programmable dc power supply, rated 1.5 kW. Table V shows the applied switching angles and the corresponding supply voltage values that were obtained choosing $V_m = 100$ V.

In three-phase configurations, computed switching angles obtained for phase "A" were shifted $(2\pi/3)$ and $(4\pi/3)$ and applied to phases "B" and "C." R–L loads with $R = 160\ \Omega$ and $L = 18.5$ mH were used both in single- and three-phase configurations.

A harmonic spectrum and THD were measured using a YOKOGAWA WT 1800 power meter. Experimental results show harmonic analysis for single- and three-phase CHB inverters with five, seven, and nine levels. Fig. 10 compares, for the five-level single-phase CHB inverter, the harmonic analysis obtained by the proposed SHM-PAWM and the



(a)



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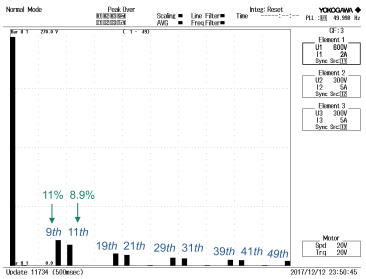


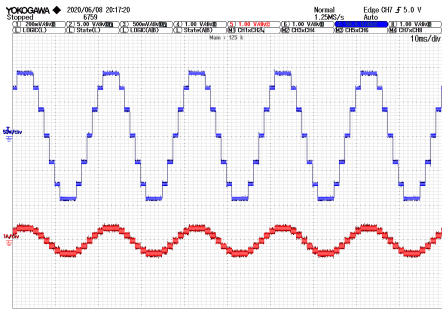
(c)

Fig. 10. Comparison between SHM-PAWM and SHE-PAWM in a single-phase five-level CHB inverter. (a) Output voltage and current of single-phase five-level CHB inverter. (b) Harmonic analysis obtained using the proposed SHM-PAWM. (c) Harmonic analysis obtained using SHE-PAWM in [22].

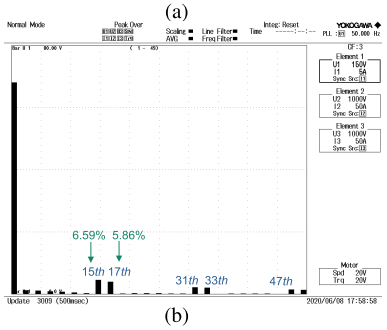
TABLE VI

MEASURED AMPLITUDES OF LOW-ORDER HARMONICS FOR A SINGLE-PHASE FIVE-LEVEL CHB INVERTER

k	F_k[V]	$\frac{F_k}{F_1}\%$	$l_k\%$ in Table I
1	66.37	100	
3	2.88	4.34	5
5	2.26	3.41	6
7	1.69	2.55	5
9	0.92	1.39	1.5
11	6.02	9.07	3.5
13	5.11	7.69	3



(a)



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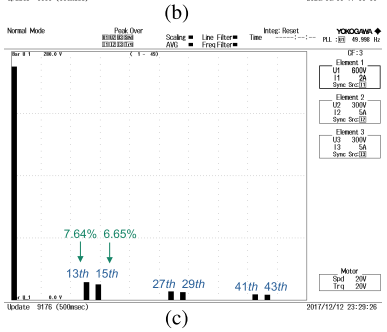


(c)

Fig. 11. Tests with the single-phase seven-level CHB inverter. (a) Output voltage and current with the proposed SHM-PAWM. (b) Harmonic analysis with the proposed SHM-PAWM. (c) Harmonic analysis with SHE-PAWM in [22].

TABLE VII

MEASURED AMPLITUDES OF LOW-ORDER HARMONICS FOR A SINGLE-PHASE SEVEN-LEVEL CHB INVERTER

k	F_k[V]	$\frac{F_k}{F_1}\%$	$l_k\%$ in Table I
1	68.24	100	
3	1.30	4.34	5
5	1.15	3.41	6
7	0.98	2.55	5
9	0.71	1.39	1.5
11	0.47	9.07	3.5
13	0.27	7.69	3
15	4.5	6.59	0.5
17	4	5.86	2

SHE-PAWM previously proposed by Buccella *et al.* [22]. Table VI summarizes the obtained absolute and weighted values with harmonics up to the 13th. Experiments were performed setting the scope at 50 V/div for the voltage and 1 A/div for the current. Fig. 11 and Table VII refer to a single-phase seven-level CHB inverter; Fig. 12 and Table VIII refer to a single-phase nine-level CHB configuration. Notice that the proposed SHM-PAWM mitigates the first $2l-1$ harmonics, meeting power quality standards. The SHE-PAWM in [22], instead, deletes the first $2l-3$ harmonics, but not the $(2l-1)$th harmonic, resulting higher overall distortion. For instance, using a five-level inverter, using the proposed algorithm, the first not mitigated harmonic is the 11th; instead,

TABLE VIII

MEASURED AMPLITUDES OF LOW-ORDER HARMONICS FOR A SINGLE-PHASE NINE-LEVEL CHB INVERTER

k	F_k[V]	$\frac{F_k}{F_1}$%	l_k% in Table I
1	65.69	100	
3	0.07	0.99	5
5	0.39	0.84	6
7	0.12	0.81	5
9	0.01	0.73	1.5
11	0.08	0.52	3.5
13	0.12	0.43	3
15	0.25	0.36	0.5
17	0	0	2
19	3.63	5.27	1.5
21	3.38	4.91	0.5

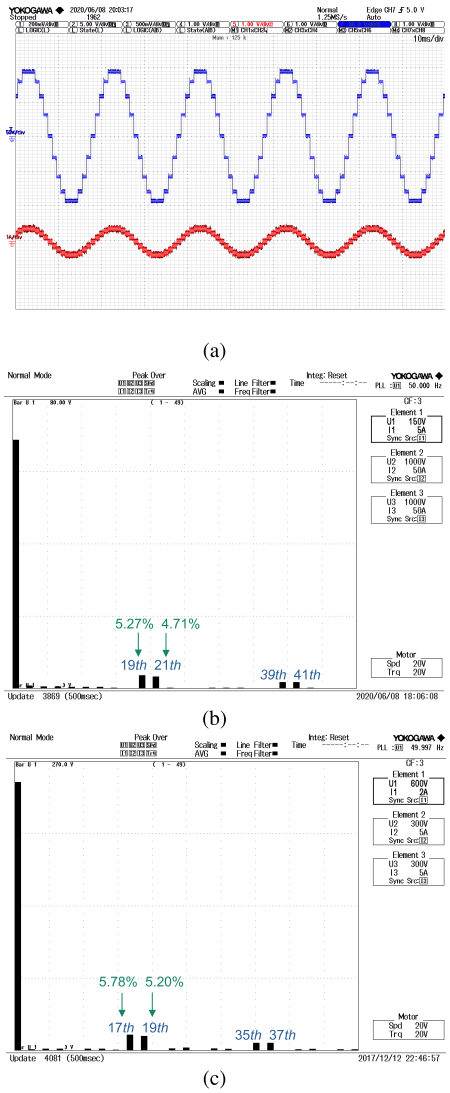


Fig. 12. Tests with the single-phase nine-level CHB inverter. (a) Output voltage and current of the single-phase nine-level CHB inverter. (b) Harmonic analysis with the proposed SHM-PAWM. (c) Harmonic analysis with SHE-PAWN in [22].

using the SHE-PAWM in [22], the first not deleted harmonic is the ninth; hence, the proposed method increases the order of the first mitigated harmonic and needs a lighter

TABLE IX

COMPUTED AND MEASURED THD%

	Single Phase		Three Phase	
	Computed	Measured	Computed	Measured
l	THD%	THD%	THD%	THD%
5	15.62	15.45	14.91	14.75
7	10.87	10.82	7.73	7.93
9	8.16	8.15	5.99	5.99

TABLE X

EXPERIMENTAL COMPARISON BETWEEN SINGLE-PHASE l-LEVEL CHB INVERTERS WITH SHM-PAWM OR SHE-PAWM

	Measured THD%	
l	SHM-PAWM	SHE-PAWM
5	15.45	17
7	10.82	11.8
9	8.15	10.5

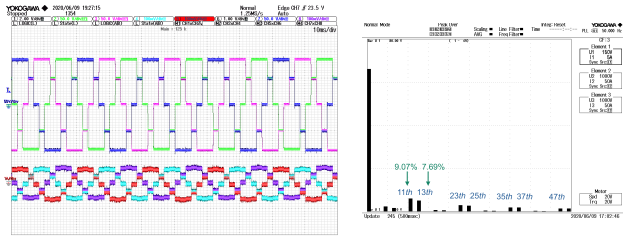


Fig. 13. Three-phase five-level CHB inverter. (a) Phase voltages and currents. (b) Harmonic analysis.

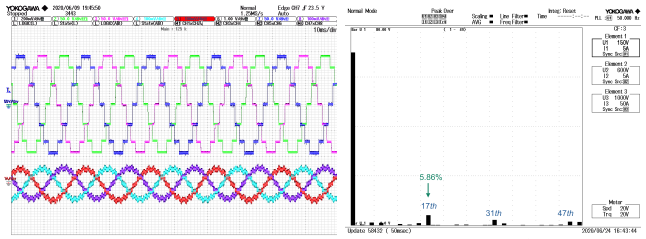


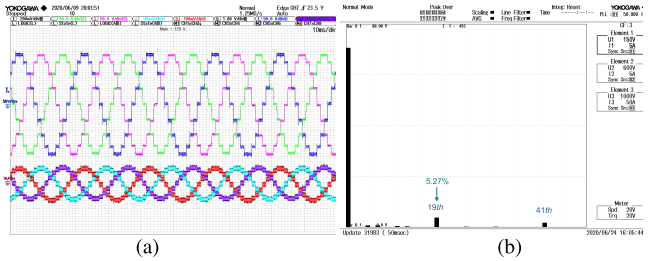
Fig. 14. Three-phase seven-level CHB inverter. (a) Phase voltages and currents. (b) Harmonic analysis.

and cheaper output filter. Table IX shows computed and measured THD%, considering harmonics up to the 49th. Good agreement between simulated and experimental results can be observed. For three-phase configurations, the SHM-PAWM allows a THD reduction with respect to the SHE-PAWM, for 7, 9, 13, 15, 19, 21, 25, . . . level inverters. Table X shows that, for the single-phase configuration, the proposed SHM-PAWM always returns lower THD rather than the SHE-PAWM in [22]. Figs. 13–15 refer to three-phase five-level, seven-level, and nine-level CHB inverters, respectively.

The experimental response of the seven-level CHB inverter with the same load is measured during a change of the modulation index from 0.65 to 0.95, and it is shown in Fig. 16,

TABLE XI
OUTPUT VOLTAGE THD% IN CASE OF IMBALANCED DC LINK VOLTAGES

	V_{dc1} [V]	V_{dc2} [V]	V_{dc31} [V]	α_i [rad]	THD%
Designed DC voltages	V_{dc1r}=164.9	V_{dc2r}=132.2	V_{dc3r}=73.38	$\frac{\pi}{14}, \frac{3\pi}{14}, \frac{5\pi}{14}$	11.86
Case #1	V_{dc1r}-10%=148.4	V_{dc2r}+10%=145.4	V_{dc3r}+5%=77.1	$\frac{\pi}{14}, \frac{3\pi}{14}, \frac{5\pi}{14}$	12.32
Case #2	V_{dc1r}-20%=131.9	V_{dc2r}+20%=158.7	V_{dc3r}+10%=80.7	$\frac{\pi}{14}, \frac{3\pi}{14}, \frac{5\pi}{14}$	13.51
Case #3	V_{dc1r}-30%=115.4	V_{dc2r}+30%=171.9	V_{dc3r}+20%=88.1	$\frac{\pi}{14}, \frac{3\pi}{14}, \frac{5\pi}{14}$	15.46



(a) (b)

Fig. 15. Three-phase nine-level CHB inverter. (a) Phase voltages and currents. (b) Harmonic analysis.

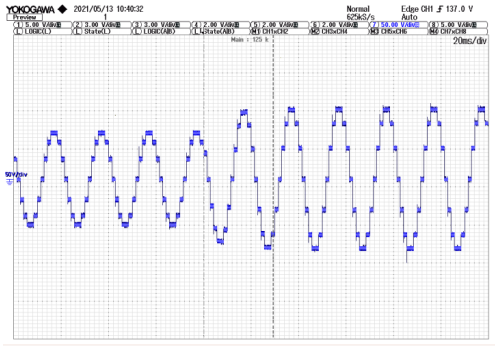


Fig. 16. Output voltage during variation of the modulation index from $m = 0.65$ to $m = 0.95$.

where it can be observed that, similar to [22], the steady-state condition is reached after about 30 ms.

For single-phase configurations with $l = 5, 7, 9$, the measured THD% values obtained by SHM-PAWM and SHE-PAWM in [22] are shown in Table X. It can be observed that SHM-PAWM reduces THD.

Finally, experimental tests named Case #1, Case #2, and Case #3, with imbalances, were performed for a single-phase seven-level inverter, assuming the rated (designed) dc voltages equal to $V_{\text{dc1}r} = 164.9$ V, $V_{\text{dc2}r} = 132.2$ V, and $V_{\text{dc3}r} = 73.38$ V, respectively. The results are shown in Table XI where the THD% is reported for each case: in Case #1, the THD% increases about 3.8%, in Case #2, about 14%, and in Case #3, about 30%.

V. CONCLUSION

In this article, a novel SHM–PAWM technique has been proposed for l-level cascaded H-bridge inverters. The method has been successfully implemented and experimentally validated using both single-phase and three-phase, five-, seven-, and nine-level inverters. The method reduces all harmonics of order $n < 2l+1$ and satisfies the European harmonic standards for medium-voltage-level applications.

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