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Guest Editorial: Special Section on Emerging Trends and Computing Paradigms for Testing, Reliability and Security in Future VLSI Systems

STEFANO DI CARLO, (Senior Member, IEEE), PEILIN SONG, AND ALESSANDRO SAVINO

With the rapid advancement of computing technologies in all domains (i.e., handheld devices, autonomous vehicles, medical devices, and massive supercomputers), testability, reliability, and security of electronic systems are crucial challenges for the safety of human life.

Emerging technologies coupled with new computing paradigms (e.g., approximate computing, neuromorphic computing, in-memory computing) are together exacerbating these problems posing significant challenges to researchers and designers. To address this increased complexity in the hardware testing, reliability, and security domains, engineers must employ design and analysis methods working at all levels of abstraction, starting from the system level down to the gate and transistor level.

This Special Section on Emerging Trends and Computing Paradigms for Testing, Reliability, and Security in Future VLSI Systems is a peer-reviewed special section of *IEEE Transactions on Emerging Topics in Computing*. The section includes twelve high-quality papers covering relevant cutting-edge results and theories on all aspects of design, manufacturing, test, monitoring, and securing VLSI systems affected by defects and malicious attacks.

The first four papers address reliability and safety at application level also considering new computing paradigms.

The paper entitled "FTxAC: Leveraging the Approximate Computing Paradigm in the Design of Fault-Tolerant Embedded Systems to Reduce Overheads" proposes approximate computing techniques in conjunction with radiation-induced mitigation strategies for the design of fault-tolerant systems with minimal overheads. Given the nature of the approximate computing paradigm, FTxAC is suitable for error-resilient applications.

The paper entitled "In Detection, Location and Concealment of Defective Pixels in Image Sensors" presents the construction process of defective pixel detection and concealment methods for image sensor online diagnosis and self-healing. The proposed process is based on pixel neighborhood analysis using only simple arithmetic operations on the image files produced by the image sensor under test to optimize the processing speed.

The paper entitled "Online Safety Checking for Delay Locked Loops via Embedded Phase Error Monitor" presents a phase error monitoring scheme for DLLs, using circuits made of only standard cells. The proposed scheme can monitor the phase error continuously to record its worst-case values during a designated monitoring session. As a result, hazardous phase error glitches can be exposed, and an alarm can be raised.

The paper entitled "Protecting Memories against Soft Errors: The Case for Customizable Error Correction Codes" proposes an automation of error correction code design for memory protection. To that end, the paper introduces a software tool that, given a word length and the error patterns that need to be corrected, produces a linear block code described by its parity check matrix and also the bit placement. The benefits of this automated design approach are illustrated with several case studies.

Reliability and testing of next generation VLSI systems are also discussed in three interesting papers:

The paper entitled "Defect and Fault Modeling Framework for STT- MRAM Testing" presents a systematic device-aware defect and fault modeling framework for STT-MRAM to derive accurate fault models that reflect the physical defects appropriately, thus providing optimal and high-quality test solutions. An overview and classification of manufacturing defects in STT-MRAMs are provided, emphasizing those related to the fabrication of magnetic tunnel junction (MTJ) devices, i.e., the data-storing elements.

The paper entitled "A Statistical Gate Sizing Method for Timing Yield and Lifetime Reliability Optimization of Integrated Circuits" proposes a new two-phase gate sizing approach to improve the reliability of the circuit considering the combined effect of process variation and transistor aging. In the first stage, the initial delay of the circuit is optimized to improve the circuit's timing yield. Then, in the second stage, the delay degradation induced by aging and process variations is reduced. Two novel concepts called aging probability and delay degradation-aware gate criticality are introduced, enabling the authors to perform gate sizing efficiently using an adaptive multi-objective ranking approach.

The paper entitled "Autonomous Scan Patterns for Laser Voltage Imaging" demonstrates how to reuse on-chip Embedded Deterministic Test (EDT) Compression to generate and apply Low Voltage Imaging (LVI)-aware scan patterns for

advanced contactless test procedures. The presented approach avoids the repetitive loading of scan chains, requires no seed patterns to encode LVI tests, has virtually no area overhead, and offers a flexible selection of non-toggling scan chains in a low power test mode.

Security of VLSI system is discussed in two interesting papers.

The paper entitled "Design and analysis of secure emerging crypto-hardware using HyperFET devices" analyzes the usage of HyperFET devices for security applications proposing new paradigms for enhancing security against Power Analysis. The paper starts from classical dual-precharge logic primitives implemented with 14nm FinFET and upgrades them to incorporate HyperFET devices. It then demonstrates using Simulation-based Differential Power Analysis significant improvements in security levels in an x25 factor, with negligible degradation in performance.

The paper entitled "Attacks toward Wireless Network-on-Chip and Countermeasures" discusses new security vulnerabilities and countermeasures to protect against them in a WiNoC based system. In particular, the paper describes the Malicious Threshold Configuration (MTC) Attack, Disruptive Token Passing (DTP) Attack, Data Stealing by Broadcast (DSB) Attack, and Hybrid Attack against the WiNoC.

Finally, reliability and security of 3D emerging fabrication technologies are covered by the last three papers of this section:

The paper entitled "3D Ring Oscillator based Test Structures to Detect a Trojan Die in a 3D Die Stack in the Presence of Process Variations" addresses the fact that 3D integrated circuits introduce both advantages and disadvantages for security. Among the disadvantages unique to 3D is the potential insertion of a Trojan die into the stack between two legitimate dies. This paper explores the use of in-stack circuitry and various testing procedures to detect an extra die through delay analysis, even in the presence of process variations.

The paper "Defect Analysis and Parallel Testing for 3D Hybrid CMOS-Memristor Memory" analyzes the electrical defects in a CMOS Molecular (CMOL) circuit used in large-scale memory systems. A parallel March-like test algorithm is presented for the CMOL architecture, which covers the faults caused by the open and bridge defects and parametric variations during its fabrication. Results show that the algorithm's test time is reduced significantly compared with the enhanced methods of March-MOM and March C* for CMOL architectures.

The paper entitled "TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology" addresses the problem of optimizing chain-type time division multiplexing access (TDMA)-based fault tolerance in 3D-ICs. The proposed technique bundles six TSVs per group in a honeycomb pattern, and the TSVs on the edges are connected, enhancing the repair rate per group and the whole TSV yield.

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STEFANO DI CARLO
Politecnico di Torino

PEILIN SONG
IBM Thomas J. Watson Research Center

ALESSANDRO SAVINO
Politecnico di Torino

STEFANO DI CARLO (Senior Member, IEEE) received the MS equivalent and PhD degrees in computer engineering and information technology from the Politecnico di Torino in Italy, in 1999 and 2003, respectively. He is an associate professor with the Department of Control and Computer Engineering, Politecnico di Torino, Italy, since 2014. His research interests include reliability analysis, FPGA design, memory testing, reliability analysis of NVM memories with ECC, design for testability, built-in self-test, fault simulation, and automatic test generation. He has authored more than 200 papers peer-reviewed publications in transactions/journals and proceedings of IEEE/ACM sponsored events. He serves on the Editorial Board of top tier journals. He has served (and regularly serves) on several Organizing and Program committees of major IEEE and ACM conferences and Symposia. He is a golden core member of the IEEE Computer Society and receipt of an Outstanding and a Meritorious Award for his volunteer activity in the IEEE Computer Society.

PEILIN SONG received the PhD degree in electrical engineering from the University of Rhode Island, in 1997. He is a principle research staff member with IBM Thomas J. Watson Research Center, where he manages the Circuit Diagnostics and Testing Technology department. He joined IBM in 1997 and has since worked in the area of design for testability, fault diagnostics, and recently hardware security and reliability. He has more than 100 publications and holds 78 US patents. He has served on several Program committees of major IEEE conferences, including IEEE VLSI Test Symposium (VTS) and International Test Conference (ITC). He is the co-Program Chair of 2019 and 2020 VTS. In 2004, he received the IEEE Electron Device Society (EDS) Paul Rappaport Award. He has been a Golden Core Member of IEEE Computer Society since 2006 and a recipient of the IEEE Computer Society Outstanding Contribution Award in 2006. He received the IEEE 2005, 2006, and 2007 Computer Society Outstanding Contribution and Meritorious Service Awards. In 2015, he received the Paul F. Forman Team Engineering Excellence Award from OSA.

ALESSANDRO SAVINO received the MS equivalent and PhD degrees in computer engineering and information technology from the Politecnico di Torino in Italy, in 2005 and 2009, respectively. He is an assistant professor with the Department of Control and Computer Engineering, Politecnico di Torino, Italy, since 2018. His research interests include reliability analysis, software-based self-test, approximate computing and image analysis. He has authored several transactions/journals papers and peer-reviewed publications in the proceedings of IEEE/ACM sponsored events. He regularly serves as reviewer of the IEEE Transactions on Reliability, Springer Journal of Electronic Testing: Theory and Applications (JETTA), and several other IEEE journals. He has been Guest Editor for a Special Issue on MDPI Electronics. He has served (and regularly serves) on several Organizing and Program committees of major IEEE and INSTICC conferences and Symposia.