Digital Object Identifier 10.1109/TETC.2021.3053795

Guest Editorial: *IEEE Transactions on Emerging Topics in Computing* Special Issue on Advanced Command, Control and On-Board Data Processing for Space Avionic Systems

GIANLUCA FURANO AND MARCO OTTAVI, (Senior Member, IEEE)

The domain of space avionic systems is changing extremely rapidly, compared to other technical domains in the spacefaring industry, under the pressure of intense competition, the continuous emergence of new markets and players, the need for cost reduction, as well as an increased obsolescence rate of components and processes due to the relative reduction of hi-rel parts market share with respect to booming volumes of consumer electronics.

The emergence of "new space" paradigm, with new (mostly private) players taking the risk of compromising with system's dependability in favour of stripped down cost further contributes to this rapidly changing landscape: new opportunities are opening for the space avionic systems. Among the most striking examples there are: the new high-performance processors architectures and silicon processes, which offer the possibility to integrate different functions until now implemented on several boards either in a single chip (SoC), or in application-specific standard products (ASSP) or in new large FPGAs are allowing multi-fold gains in performances and miniaturization for electronic systems. Reliability and availability constraints remain the main driving requirements for established space hardware manufacturers. In this context, the emergence of space systems based on Commercial-Off-The-Shelf (COTS) only and aggressive commercial platforms adds further uncertainties and possibilities to an already very dynamic landscape. New creative and technically sound solutions are needed to provide a valid and attractive alternative to the tempting shortcut of cutting costs by waiving the rigorous test and quality assurance processes applied to 'institutional' satellites.

This Special Section consists of five papers that cover a wide spectrum of techniques: software techniques, CAN-based instrumentation, characterization methodologies, and on FPGA based accelerators. While focusing on different topics, all the papers have a common denominator: the complexity and capabilities of electronic systems in space is growing at a fast pace and new platforms and methodologies are emerging.

In "*CAN implementation and performance for Raman Laser Spectrometer (RLS) Instrument on Exomars 2020 Mission*" the authors show the results of the use of the CAN bus in the ESA Exomars mission, this is a good example of the faster pace of innovation in space which is bringing to the adoption of standards from other applications such as CAN initially conceived for automotive.

"*A Platform-Aware Model-Driven Embedded Software Engineering Process Based on Annotated Analysis Models*" focuses on the development of embedded software systems in state of the art space platforms: in particular the authors propose a framework to enable the integration of complex systems; this is representative of the increasing complexity of on board computing which brings great challenges to the verification process.

Similarly, the development of complex software systems for Space is the focus of "*Surrogate Applications for Early Design Stage Multicore Contention Modeling*". The paper introduces a method to optimally allocate software development time between early design phases and late design phases by proposing surrogate applications and a framework to generate them.

Another important push happening in the development of On Board Computing Systems is the widespread use of FPGA acceleration to enable acceleration, "*A 3.3 Gbps CCSDS 123.0-B-1 Multispectral & Hyperspectral Image Compression Hardware Accelerator on a Space-Grade SRAM FPGA*" proposes beyond state of the art implementation of hyperspectral image compression accelerator using space grade FPGA.

With the increase of complexity of on board computing, it becomes extremely important to support standard characterization methods with low complexity and cost based screening, "*First tests of a new facility for device–level, board-level and system-level neutron irradiation of microelectronics*" introduces the neutron facility ChipIR. Irradiation with high-energy neutrons can be used for system level screening of soft errors at board level due to the beam uniform intensity over hundreds of cm^2 provided by ChipIR.

We hope you will find the contents of this Special Issue interesting. We would like to acknowledge the reviewers for providing valuable reviews, which have greatly improved the quality of the final submissions for this issue. Finally we wish to thank the authors for submitting their outstanding research to this Special Issue, and for their commitment and patience through all the stages of the review process. We are grateful to IEEE Transactions on Emerging Topics in Computing in particular the former Editor-in-Chief Prof. Fabrizio Lombardi, and Prof. Cecilia Metra, and the current Editor-in-Chief Prof. Paolo Montuschi, for making this Special Issue possible.

Sincerely,

Gianluca Furano
Marco Ottavi
Guest Editors

GIANLUCA FURANO received the PhD degree. He has worked in European Space Agency's Data System Division since 2003. He is in charge of research and development activities and he coordinates ESA activities on on-board artificial intelligence. His research interest include ESA are on-board computers and their major components, such as space grade microprocessors and support electronics, meeting very stringent requirements in terms of radiation tolerance, reliability, availability, and safety; key avionics building blocks such as platform mass memories, remote terminal units, on-board buses and data networks; on-board and space to ground data communication protocols including protocol security aspects. He also provides support to European standardisation (CCSDS, ECSS) in areas such as telemetry, telecommand and on-board data, wireless and monitoring control interfaces. He has authored or co-authored more than 100 publications.

MARCO OTTAVI (Senior Member, IEEE) is currently an associate professor with National Scientific Qualification for full professor in electronic engineering with the University of Rome Tor Vergata. In 2009 he was the recipient of a prestigious "rientro dei cervelli" fellowship, awarded by the Italian Ministry of University and Research. Previously, he was a senior design engineer at AMD in Boxborough, (MA) USA, and he held postdoctoral positions with Sandia National Laboratories in Albuquerque, (NM) USA, and with the ECE Department of Northeastern University in Boston, (MA) USA. His research interests include VLSI yield and reliability modeling, fault-tolerant computer architectures for highly dependable systems, and online testing and design of nanoscale circuits and systems. In these fields, he has published more than 130 articles on archival journals and peer-reviewed conferences. From December 2011 to November 2015 he was the chair of COST Action IC1103 "Manufacturable and Dependable Multicore Architectures at Nanoscale" (MEDIAN). He serves as a member of several conference program committees and as a reviewer for various IEEE journals and highly cited conferences. He has served as an associate editor of *IEEE Transaction on Emerging Topics in Computing* and is currently an associate editor of *IEEE Transactions on Nanotechnology* and of *IEEE Nanotechnology Magazine*.