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Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS

AIBIN YAN, CHAOPING LAI, YINLEI ZHANG, JIE CUI, ZHENGFENG HUANG, JIE SONG, JING GUO, AND XIAOQING WEN, (Fellow, IEEE)

A. Yan, C. Lai, Y. Zhang, J. Cui, and J. Song are with the School of Computer Science and Technology, Anhui University (AHU), Hefei 230601, China
and also with Anhui Engineering Laboratory of IoT Security Technologies, Anhui University (AHU), Hefei 230601, China
Z. Huang is with the School of Electronic Science & Applied Physics, Hefei University of Technology, Hefei 230009, China
J. Guo is with the Key Laboratory of Instrumentation Science and Dynamic Measurement, North University of China, Taiyuan 030051, China
X. Wen is with the Department of Creative Informatics, and the Graduate School of Computer Science and Systems Engineering,
Kyushu Institute of Technology, Fukuoka 8208502, Japan
CORRESPONDING AUTHOR: A. YAN (abyan@mail.ustc.edu.cn)

ABSTRACT This paper presents two novel low cost, double-and-triple-node-upset tolerant latch designs. First, a novel low cost and double-node-upset (DNU) completely tolerant (LCDNUT) latch design is proposed. The latch mainly comprises a storage module (SM) feeding back to a 3-input C-element. The SM mainly consists of eight input-split inverters. Since the inputs of the C-element cannot be simultaneously flipped, the latch tolerates any DNU in the SM. When a single node in the SM and the output node are affected, the latch can self-recover from the DNU. Second, to completely tolerate any triple-node-upset (TNU), by replacing the C-element in the LCDNUT latch with a two-level error-interceptive module constructed from triple C-elements, a novel low cost and TNU completely tolerant (LCTNUT) latch design is proposed. Simulation results demonstrate the robustness of the proposed latches. Furthermore, due to the use of a high-speed transmission path, the clock-gating technology and fewer transistors, the proposed LCTNUT latch reduces the delay-power-area product by approximately 99.39 percent and has a low sensitivity to the process-voltage-and-temperature variation effects, compared with currently the only TNU completely tolerant latch design.

INDEX TERMS Circuit reliability, radiation hardening, triple-node upset, double-node upset, single node upset, soft error

I. INTRODUCTION

In the nano-scale CMOS technology, the electron devices in circuits and systems are becoming more sensitive to soft errors due to the aggressive scaling down of the feature sizes of transistors. Soft errors are typically caused by the striking of particles like neutrons, protons and heavy ions in space, alpha particles in packaging, and high-energy electrons [1], [2]. When an energetic particle hits the diffusion region of a reverse bias transistor of a storage module, the generated charge can be collected by the nearby junctions via drift and diffusion mechanisms, resulting in voltage transients referred as a single node upset (SNU). Besides, due to the aggressive decrease of node capacitances and node spacing, one particle striking may affect multiple nodes, resulting in a double-node upset (DNU) or even triple-node upset (TNU) through charge sharing [3]. Since any upset can cause date corruption, execution error, or even system crash in the worst case, there is a strong need to design upset tolerant or even self-recoverable storage modules for the purpose of constructing highly reliable large scale integration systems.

Radiation hardening by design (RHBD) is one of the most effective techniques to mitigate soft errors. In the last decade, researchers have mostly focused on the radiation hardening for memory cells [4], [5], flip-flops [6], [7] and latches [1], [8]–[21] using RHBD techniques like multiple-modular redundancy, temporal redundancy, and so on. This paper mainly focuses on these latch designs. In these latch designs, some are only SNU-hardened [8]–[15] and some are simultaneously hardened for both SNU and DNU [16]–[21]. As far as we know, there is currently only one design that is simultaneously hardened for SNU, DNU and TNU [1].

Among these SNU-hardened latch designs, some are only partially SNU-hardened since there is at least one node that can be flipped, which may cause invalid data retaining like

those in [8], [9]. Some are completely SNU-hardened but there is at least one node that cannot self-recover from an SNU though such a latch can still output correct data like the High performance, Low cost and Robust (HLR) design in [11] and those in [10], [12]–[14]. Some are completely SNU self-recoverable, such as the designs referred as HLR-CG1/CG2 in [11] and the self-Recoverable, Frequency-aware and Cost-effective (RFC) design in [15]. Among these DNU-hardened latch designs, some are only partially DNU-hardened [16] and some are completely DNU-hardened [17]–[21], in which the designs in [18]–[21] are completely DNU self-recoverable. As for currently the only one design in [1] that completely tolerates any TNU, there are some problems, such as not being completely DNU self-recoverable and having high cost penalties.

In this paper, novel low cost, DNU and/or TNU completely tolerant latch designs are proposed. First, using eight input-split inverters, a storage module is constructed for keeping values. By feeding back three specific nodes in the storage module to a 3-input C-element, a novel Low Cost and DNU completely Tolerant (LCDNUT) latch is proposed. Since all the inputs of the C-element cannot be simultaneously flipped, the latch tolerates any DNU in the storage module. If one node in the storage module and the output node are affected, the latch can self-recover from the DNU. Second, a novel low cost and TNU completely tolerant latch design is proposed by replacing the C-element in the LCDNUT latch with a two-level error-interceptive block constructed from three C-elements. Due to the use of the high-speed transmission path, the clock-gating technology and fewer transistors, the costs of these latch designs are also low. Simulation results demonstrate the robustness, low cost and low sensitivity to the process-voltage-and-temperature variation effects for the proposed latch designs.

The rest of the paper is organized as follows: Section II reviews some typical SNU/DNU/TNU hardened latch designs. Section III describes the implementation, normal working principles and fault tolerance verifications for the proposed latch designs. Section IV presents the evaluation and comparison results for overheads. Section V concludes the paper.

II. TYPICAL LATCH DESIGNS

In many hardened latch designs, the C-element [22] is widely used. A C-element outputs an inverted value if its inputs are identical and retains its previous value if its inputs are different. Figure 1 shows the 2-input and 3-input C-elements. It is also easy to create a 4-input one. The C-element is also controllable by the system clock signals. Figure 1 shows the clock-gating based C-elements. This section reviews typical examples of SNU, DNU and/or TNU hardened latch designs as shown in Figure 2 including the FEedback Redundant SNU-Tolerant (FERST) [10], RFC [15], the so-called HRPU [16], Double-Node Charge Sharing (DNCS) [17], Double-Node Upset Resilient (DNUR) [18], Non-Temporally Hardened LaTCH (NTHLTCH) [19] and TNU Hardened Latch (TNUHL) [1].

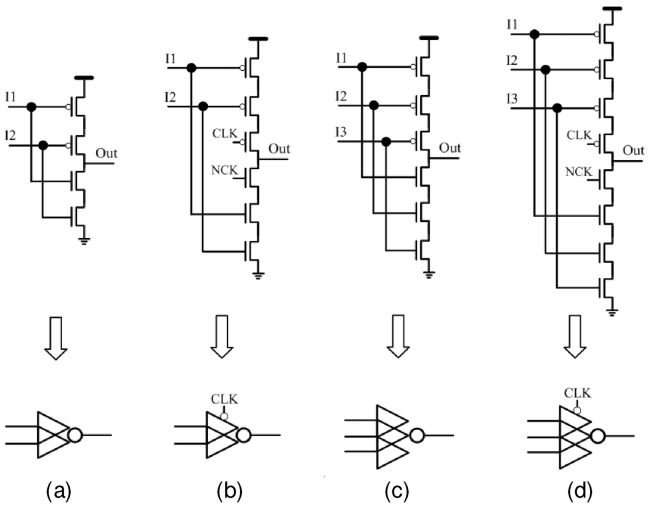

FIGURE 1. Different C-elements. (a) 2-input C-element. (b) Clock-gating based 2-input C-element. (c) 3-input C-element. (d) Clock-gating based 3-input C-element.

To completely tolerate any SNU, the FERST latch in [10] mainly uses two interlocked feedback loops as shown in the left part of Figure 2a. The C-element in the right part is used for a voter. In this figure, the switches are transmission gates (TGs). As for clock signal connection to a TG, we take the TG between the nodes D and I1 as an example. Since it is marked with the negative system clock (NCK), the gate terminal of the pMOS transistor is connected to NCK and the gate terminal of the nMOS transistor is connected to the system clock (CLK). This rule is applicable for all designs in this paper.

To completely self-recover from any SNU, as shown in Figure 2b, the RFC latch in [15] mainly employs three interlocked C-elements, making it SNU self-recoverable. However, the latch is not DNU-tolerant since if the outputs of any two C-elements are flipped, it will retain invalid data. The HRPU latch in [16] mainly consists of four interlocked C-elements, as shown in Figure 2c, enabling the latch to self-recover from any SNU. However, the latch cannot completely tolerate any DNU since it will retain invalid data if I1 and I2 are flipped.

To completely tolerate any DNU, as shown in Figure 2d, the DNCS latch in [17] mainly uses a large feedback loop in the left part connected to a 3-input C-element at the output stage; however, the latch is not completely DNU self-recoverable.

To completely self-recover from any DNU, as shown in Figure 2e, the DNUR latch in [18] uses three delta cells, each being an RFC cell as shown in Figure 2b. However, the latch cannot completely tolerate any TNU (e.g., a TNU at $<$I2, I3, I4$>$). Similarly, the NTHLTCH latch shown in Figure 2f cannot completely tolerate any TNU either.

To completely tolerate a TNU, as shown in Figure 2g, the TNUHL latch in [1] mainly employs eight multiple-input C-elements and five inverters to construct many interlocked feedback loops to robustly keep data. However, the latch

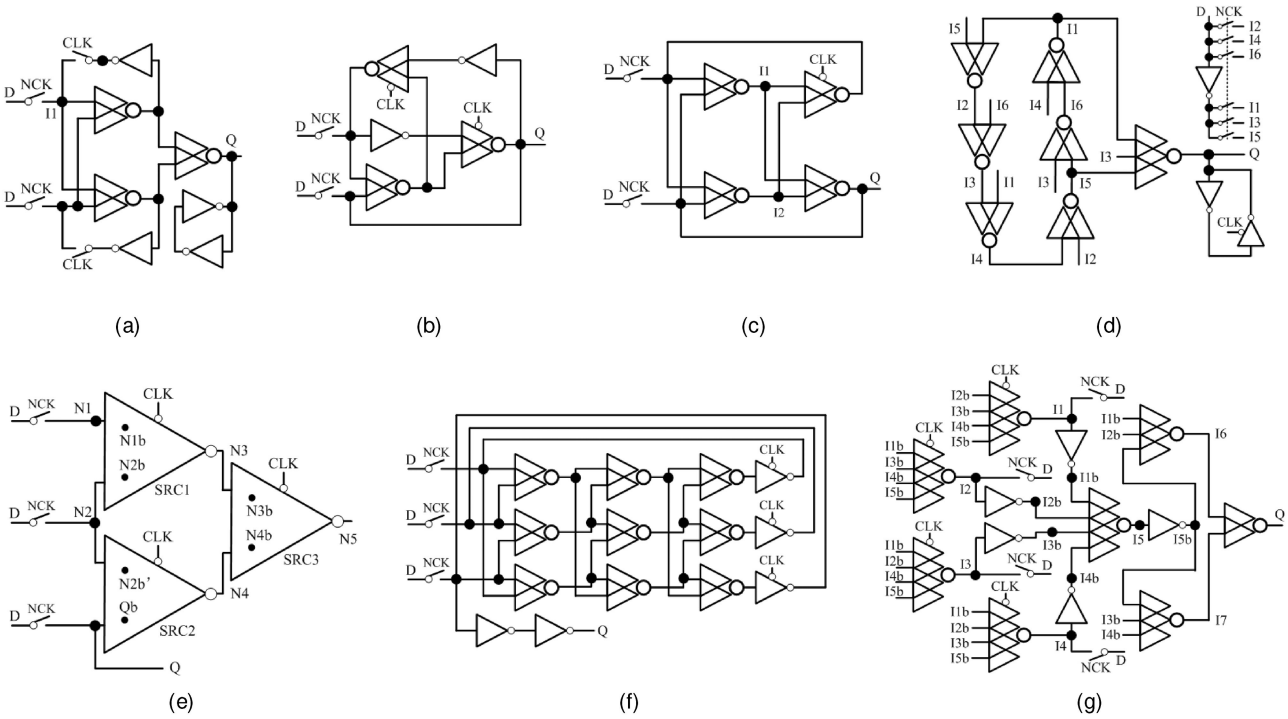

FIGURE 2. Schematics of some typical latch designs. (a) FERST. (b) RFC. (c) HRPU. (d) DNCS. (e) DNUR. (f) NTHLTCH. (g) TNUHL.

contains many node pairs that cannot self-recover from a DNU and its costs are high.

III. PROPOSED LATCH DESIGNS

A. PROPOSED DNU COMPLETELY TOLERANT LATCH DESIGN

Figure 3 shows the schematic of the proposed Low Cost and DNU-completely Tolerant (LCDNUT) latch design. It can be seen from Figure 3 that the latch is mainly constructed from a storage module in the left part and a clock-gating (CG) based error-interceptive 4-input C-element in the right part. The storage module consists of four input-split inverters (IINV1, IINV2, IINV3, and IINV4), four CG-based input-split inverters (CG-IINV1, CG-IINV2, CG-IINV3, and CG-IINV4) and four TGs (TG1, TG2, TG3, and TG4). In the proposed latch, I1 to I8 are internal nodes for retaining data. D, Q, CLK, and NCK are the input, the output, the system clock, and the negative system clock, respectively.

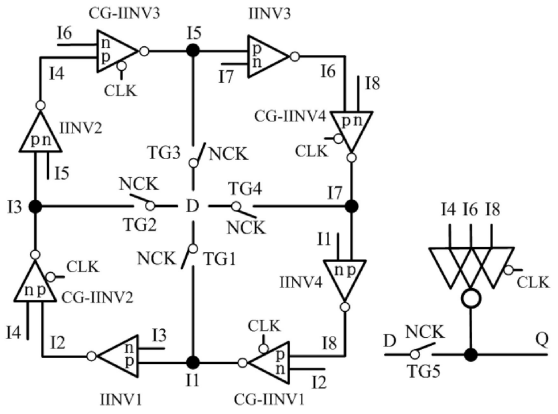

FIGURE 3. Schematic of the proposed LCDNUT latch design.

When CLK = 1 and NCK = 0, the latch works in transparent mode and all the TGs are ON. Assumed that D = 1, i.e., I1 = I3 = I5 = I7 = 1. In this case, the nMOS transistors in IINV1, IINV2, IINV3, and IINV4 are ON, resulting in I2 = I4 = I6 = I8 = 0. This way, the signals of all the internal nodes in the latch can be determined. Furthermore, the CG-based transistors in the CG-based input-split inverters are OFF to prevent the formation of feedback loops in transparent mode so as to reduce current competitions on the internal nodes I1, I3, I5, and I7 so as to save power dissipation. On the other hand, since TG5 is ON and the CG-based transistors in the C-element are OFF, Q can only be quickly determined through TG5 (Q = D = 1) and hence D to Q transmission delay can be reduced to improve performance.

When CLK = 0 and NCK = 1, the latch switches to hold mode. All the TGs are OFF and hence the internal nodes I2, I4, I6, and I8 currently retain their previous values. Meanwhile, the CG-based transistors in the CG-based input-split inverters are ON and hence the signals of the nodes I1, I3, I5, and I7 can only be determined by the signals of the nodes I2, I4, I6, and I8 through the CG-based input-split inverters. Subsequently, the signals of the nodes I1, I3, I5, and I7 feed back to I2, I4, I6, and I8. This way, the feedback loops can be formed in the latch to robustly retain data. On the other hand, Q can only be determined by the internal nodes I4, I6, and I8 through the C-element. Therefore, the latch can retain and output the correct value in hold mode.

Next, the SNU/DNU/TNU tolerance principles for the latch are discussed. Note that, we just take the example of storing 1 of the latch for all fault-tolerance discussions throughout this paper and at that time $Q = I1 = I3 = I5 = I7 = 1$ and $I2 = I4 = I6 = I8 = 0$. In general, only the principles for hold mode are analyzed.

First, as for the storage module of the latch, the SNU/DNU/TNU tolerance principles are discussed. In the presence of an SNU, due to the symmetry of the storage module, we consider the case where I1 is affected by the SNU. Since I1 is temporarily flipped, the nMOS transistor in IINV4 will be temporarily OFF. However, I7 is not immediately affected and I8 retains its previous correct value ($I8 = 0$) since the transistors in IINV4 are OFF. On the other hand, I3 is not immediately affected, thus the nMOS transistor in IINV1 is still ON and I2 outputs 0 (strong 0). The temporarily flipping from 1 to 0 of I1 results in that the pMOS transistor in IINV1 is temporarily ON, thus I2 outputs 1 (weak 1). However, the strong 0 of I2 can neutralize the weak 1 of I2, thus I2 is still correct ($I2 = 0$) and the nMOS transistor in CG-IINV1 is still OFF. Meanwhile, as mentioned above, since $I8 = 0$, I1 outputs 1 (strong 1). The temporal flipping from 1 to 0 of I1 results in that I1 outputs 0 (weak 0). However, the strong 1 of I1 can neutralize the weak 0 of I1, thus I1 is still correct. It can be seen that all nodes still retain their correct values. It can be found through a simple investigation that the storage module is completely self-recoverable from any SNU no matter what value (1 or 0) is stored.

Next, the DNU tolerance principles for the storage module are discussed. Due to the symmetry of the storage module, we consider three possible cases where a pair of nodes is affected by a DNU in the following.

Case D1. Since any node pair is constructed from two of the nodes I2, I4, I6, and I8, it is obvious that there are a total of six node pairs. Note that the node pairs $<I4, I8>$ vs. $<I2, I6>$, $<I8, I2>$ vs. $<I4, I6>$ and $<I2, I4>$ vs. $<I6, I8>$ are symmetrical as shown in Figure 3. Hence, it is only necessary to consider the node pairs $<I8, I2>$, $<I4, I8>$, and $<I6, I8>$ for the DNU tolerance discussions. Besides, since the node pairs $<I8, I2>$ and $<I6, I8>$ are also symmetrical, it is only necessary to consider the node pairs $<I4, I8>$ and $<I4, I6>$ for the DNU tolerance discussions.

Before a DNU occurs at the node pair $<I4, I8>$, $I4 = I8 = 0$ and the pMOS transistors in CG-IINV1 and CG-IINV3 are ON. Hence both I1 and I5 output their correct values. When a DNU occurs at $<I4, I8>$, i.e., I4 and I8 are temporarily flipped from 0 to 1, the pMOS transistors in CG-IINV1 and CG-IINV3 are temporarily OFF. Hence both I1 and I5 can retain their previous values ($I1 = I5 = 1$). Before a DNU occurs at the node pair $<I4, I8>$, $I2 = I6 = 0$ and the pMOS transistors in CG-IINV2 and CG-IINV4 are ON. Hence both I3 and I7 output 1 (strong 1). When a DNU occurs at $<I4, I8>$, i.e., I4 and I8 are temporarily flipped from 0 to 1, the nMOS transistors in CG-IINV2 and CG-IINV4 are temporarily ON. Hence both I3 and I7 output 0 (weak 0). However, as for I3 and I7, the strong 1 of them will neutralize the weak 0 of them. As a result, they will still keep the correct values. As mentioned above, I1 and I5 are also correct. Therefore, I4 and I8 can self-recover from the DNU through IINV2 and IINV4, respectively. Similarly, when a DNU occurs at the node pair $<I4, I6>$, it can be found that the node pair can also completely self-recover from the DNU.

On the other hand, in the case of 0 being stored, it can be found through a simple investigation that the storage module is completely self-recoverable from the DNU at $<I4, I8>$. However, the storage module cannot self-recover from the DNU at $<I4, I6>$ and it can be found that I4 and I7 enter into undetermined states and I5 and I6 are flipped. In the following, similar discussions are presented. Note that, this paper defines an undetermined state as a state that it is neither the supply voltage value nor the ground value, though it looks like the supply voltage value or ground value in the subsequent simulation diagrams.

Case D2. Any node pair is constructed from two of the nodes I1, I3, I5, and I7, and obviously there are a total of six node pairs. The indicative node pairs are $<I3, I7>$ and $<I3, I5>$ according to Case D1. Since the analysis flow is similar to that of Case D1, the detailed discussions are omitted here except conclusions. The node pair $<I3, I7>$ is completely self-recoverable from the DNU no matter what value (1 or 0) is stored. The node pair $<I3, I5>$ cannot self-recover from the DNU. This is because I3 and I6 enter into undetermined states and I4 and I5 are flipped in the case of 1 being stored; I2 and I5 enter into undetermined states and I3 and I4 are flipped in the case of 0 being stored.

Case D3. Any node pair is constructed from one of the nodes I2, I4, I6, I8, and one of the nodes I1, I3, I5, I7, it is obvious that there are a total of 16 node pairs. Since the nodes I2, I4, I6, and I8 are symmetrical, it is only necessary to consider the node pairs $<I1, I8>$, $<I3, I8>$, $<I5, I8>$, and $<I7, I8>$ for the DNU toleration discussions. Besides, since the node pairs $<I8, I1>$ vs. $<I7, I8>$ and $<I8, I3>$ vs. $<I5, I8>$ are symmetrical, it is only necessary to consider the node pairs $<I8, I1>$ and $<I8, I3>$ for the DNU toleration discussions.

When a DNU occurs at $<I8, I1>$, i.e., I8 is flipped from 0 to 1 and I1 is flipped from 1 to 0, the nMOS transistor in CG-IINV4 and the pMOS transistor in IINV1 will be ON. Since I6 is not immediately affected ($I6 = 0$), the pMOS transistor in CG-IINV4 is ON. Hence, I7 enters to an undetermined state since all transistors are ON in CG-IINV4. At this time, all transistors in IINV3 are OFF and I6 retains its previous value. Meanwhile, the transistors in IINV4 are OFF and hence I8 cannot self-recover. On the other hand, since I3 is not immediately affected ($I3 = 1$), the nMOS transistor in IINV1 is ON. Since the flipping of I1 results in that the pMOS transistor in IINV1 is ON, I2 enters into an undetermined state since all transistors are ON in IINV1. At this time, all transistors in CG-IINV1 are OFF and I1 has to retain the flipped value ($I1 = 0$). Meanwhile, the transistors in CG-IINV2 are OFF, hence I3 retains its correct value. Obviously, I4 and I5 also keep their correct values. Therefore, the DNU

at <I8, I1> results in that I2 and I7 enter into undetermined states and I8 and I1 are flipped. Similarly, when a DNU occurs at <I8, I3>, it can be found that the node pair can completely self-recover from the DNU.

On the other hand, in the case of 0 being stored, it can be found through a simple investigation that the storage module is completely self-recoverable from the DNU at <I8, I1>. However, the storage module cannot self-recover from the DNU at <I8, I3> and accordingly, it can be found that only the nodes I3 and I8 enter into undetermined states and I1 and I2 are flipped.

As mentioned above, the storage module can completely self-recover, or partially self-recover, or cannot self-recover from a DNU. Next, the TNU tolerance principles for the storage module are discussed. Due to the symmetry of the storage module, we consider three possible cases where a node-list is affected by a TNU in the following.

Case T1. The adjacent triple-node of the storage module is affected by a TNU (e.g., <I1, I2 I3> and <I2, I3 I4>). When <I1, I2 I3> flips, the inputs and output of IINV1 (its nMOS turns OFF) flip. At this time, since I5 is not affected, the transistors in IINV2 are ON. Hence, I4 enters into an undetermined state. Meanwhile, CG-IINV2 cannot output the correct value since all transistors in CG-IINV2 are OFF. Hence, I3 retains the invalid value 0 and I2 cannot self-recover to its correct value 0 through IINV1 by I3. Meanwhile, the invalid value 1 of I2 in IINV1 feeds back to I1 through CG-IINV1 (its pMOS is still ON due to the correct I8), thus I1 enters into an undetermined state since all the transistors in CG-IINV1 are ON. Hence, I8 retains its previous value since all transistors in IINV4 are OFF. Therefore, the TNU at <I1, I2 I3> only results in that I1 and I4 enter into undermined states and I2 and I3 are flipped. Similarly, when a TNU occurs at the node list <I2, I3 I4>, it can also be found that I1 and I4 enter into undermined states and I2 and I3 are flipped.

On the other hand, in the case of 0 being stored, it can be found through a simple investigation that the storage module also cannot self-recover from the TNU at <I1, I2 I3> or <I2, I3 I4>. As for the TNU at <I1, I2 I3>, it can be found that I3 and I8 enter into undetermined states and I1 and I2 are flipped. As for the TNU at <I2, I3 I4>, it can be found that I2 and I5 enter into undetermined states and I3 and I4 are flipped.

Case T2. The separated triple-node of the storage module is affected by a TNU (e.g., <I1, I3, I5>, <I1, I4 I6> and <I1, I5 I7>). When <I1, I3, I5> flips, since I7 is not immediately affected (I7 = 1) and I1 flips from 1 to 0, I8 retains its correct value (I8 = 0) since the transistors in IINV4 are OFF. Meanwhile, since I5 flips from 1 to 0 and I7 = 1, the transistors in IINV3 are ON and hence I6 enters into an undetermined state. At this time, I7 still retains its correct value since all transistors in CG-IINV4 are OFF. On the other hand, the flipping of I2 from 0 to 1 results in that the nMOS transistor in CG-IINV1 is ON (the pMOS transistor in CG-IINV1 is also ON due to the correct I8), thus I1 enters into an undetermined state and the pMOS transistor in IINV1 becomes OFF. Meanwhile, the flipping of I3 from 1 to 0 results in that the nMOS transistor in IINV1 becomes OFF and hence I2 retains the flipped value (I2 = 1) since all transistors in IINV1 are OFF. Since I2 is flipped from 0 to 1, I3 cannot self-recover from the flipped value 0 to 1 through CG-IINV2 by I2, i.e., I3 retains the invalid value (I3 = 0) and the pMOS transistor in IINV2 becomes ON. Furthermore, the flipping of I5 from 1 to 0 results in that the nMOS transistor in IINV2 becomes OFF, thus IINV2 outputs an invalid value, i.e., I4 = 1. Hence, the pMOS transistor in CG-IINV3 becomes OFF. As mentioned above, I6 has entered an undetermined state, thus I5 retains the flipped value since all transistors in CG-IINV3 are OFF. Therefore, the TNU at <I1, I3, I5> results in that I1 and I6 enter into undermined states and I2 to I5 are flipped. Similarly, when a TNU occurs at the node list <I1, I4 I6>, it can be found that the node list can completely self-recover from the TNU. When a TNU occurs at the node list <I1, I5 I7>, it can be found that I2 and I5 enter into undermined states and I1, and I6 to I8 are flipped.

On the other hand, in the case of 0 being stored, it can be found through a simple investigation that the storage module cannot self-recover from the TNU at <I1, I3, I5>, <I1, I4 I6> or <I1, I5 I7>. As for the TNU at <I1, I3, I5>, it can be found that I5 and I8 enter into undetermined states and I1 to I4 are flipped. As for the TNU at <I1, I4 I6>, it can be found that I1, I4 and I5 enter into undetermined states and I6 to I8 are flipped. As for the TNU at <I1, I5 I7>, it can be found that I1 and I4 enter into undetermined states and I5 to I8 are flipped.

Case T3. The adjacent double-node with a separated node of the storage module is affected by a TNU (e.g., <I1, I2 I4>, <I3, I4 I7> and <I5, I6 I8>). When <I1, I2 I4> flips, I6 is not affected (I6 = 0). The flipping of I4 from 0 to 1 results in that the pMOS transistor in CG-IINV3 becomes OFF. Thus I5 retains its correct value (I5 = 1) since all transistors in CG-IINV3 are OFF. As a result, I4 outputs 0 (strong 0) through IINV2 due to I5 = 1. The flipping of I4 from 0 to 1 results in that I4 tends to output 1 (weak 1). However, the strong 0 of I4 can neutralize the weak 1 of I4, thus I4 retains its correct value (I4 = 0) and the nMOS transistor in CG-IINV2 is OFF. The flipping of I2 from 0 to 1 results in that the pMOS transistor in CG-IINV2 is OFF. Hence, I3 retains its correct value (I3 = 1) since all transistors in CG-IINV2 are OFF. Meanwhile, I2 outputs 0 (strong 0) through IINV1 due to I3 = 1. The flipping of I2 from 0 to 1 results in that I2 tends to output 1 (weak 1). However, the strong 0 of I2 can neutralize the weak 1 of I2, thus I2 retains its correct value (I2 = 0) and the nMOS transistor in CG-IINV1 is OFF. Since I7 is not affected (I7 = 1), all transistors in IINV4 will be OFF if I1 is flipped. As a result, I8 always retains its correct value (I8 = 0) and the pMOS transistor in CG-IINV1 is ON. At this time, since I2 = 0 as mentioned above, I1 outputs 1 (strong 1) through CG-IINV1. The flipping of I1 from 1 to 0 results in that I1 tends to output

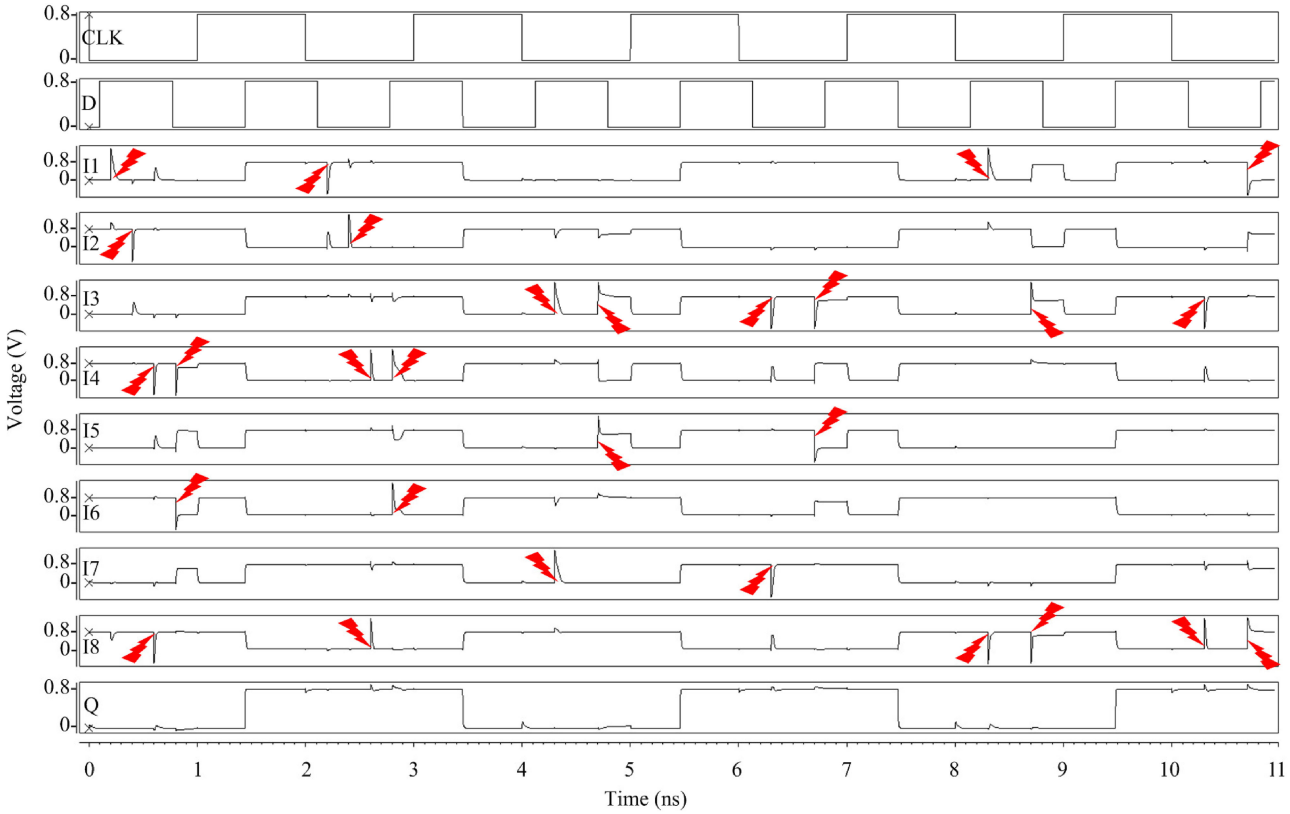

FIGURE 4. **Simulation results for the key SNU and DNU injections of the LCDNUT latch design.**

0 (weak 0). However, the strong 1 of I1 can neutralize the weak 0 of I1, thus I1 retains its correct value (I1 = 1). Therefore, as for the TNU at $<$I1, I2 I4$>$, all nodes can completely self-recover from the TNU. Similarly, when a TNU occurs at the node list $<$I3, I4 I7$>$ or $<$I5, I6 I8$>$, it can be found that the node lists can also completely self-recover from the TNU.

On the other hand, in the case of 0 being stored, it can be found through a simple investigation that the storage module cannot self-recover from the TNU at $<$I1, I2 I4$>$, $<$I3, I4 I7$>$ or $<$I5, I6 I8$>$. As for the TNU at $<$I1, I2 I4$>$, it can be found that I5 and I8 enter into undetermined states and I1 to I4 are flipped. As for the TNU at $<$I3, I4 I7$>$, it can be found that I2 and I7 enter into undetermined states and I3 to I6 are flipped. As for the TNU at $<$I5, I6 I8$>$, it can be found that I1 and I4 enter into undetermined states and I5 to I8 are flipped.

From the above discussions, three important conclusions can be drawn for the storage module of the latch as follows.

(a) The storage module is completely self-recoverable from any SNU no matter what value (1 or 0) is stored.

(b) The storage module can completely self-recover, or partially self-recover, or cannot self-recover from a DNU. However, as for any DNU, two (let alone three and four) of the internal nodes I1, I3, I5, and I7 cannot be simultaneously flipped to wrong values and the other two nodes are correct. This is also true for the internal nodes I2, I4 I6, and I8, no matter what value (1 or 0) is stored.

(c) The storage module can completely self-recover, or partially self-recover, or cannot self-recover from a TNU. However, as for any TNU (let alone DNU), three (let alone four) of the internal nodes I1, I3, I5, and I7 cannot be simultaneously flipped to wrong values. This is also true for the internal nodes I2, I4 I6 and I8, no matter what value (1 or 0) is stored.

Second, as for the LCDNUT latch, the SNU/DNU tolerance principles are discussed. Obviously, the latch is SNU completely self-recoverable since the storage module is SNU completely self-recoverable. On the other hand, if one node in the storage module and Q are affected by a DNU, the latch can completely self-recover from the DNU since the storage module can first self-recover and then Q can self-recover. Besides, if two nodes in the storage module are affected by a DNU, the latch can tolerate the DNU (Q is still correct) since all the inputs of the C-element (i.e., I4, I6, and I8) cannot be completely flipped as mentioned in (c) of the three important conclusions for the storage module. Therefore, the latch tolerates any DNU.

Figure 4 shows the simulation results for the key SNU and DNU injections of the LCDNUT latch design. It can be seen from Figure 4 that the LCDNUT latch can completely tolerate any key SNU and DNU since Q always retains the correct value. According to Figure 4, Table 1 shows the statistic results for the key SNU and DNU injections of the LCDNUT

TABLE 1. Statistic results for the key SNU and DNU injections of the LCDNUT latch design according to Fig. 4.

Time (ns)	SNU/ DNU	State	Result	Time (ns)	SNU/ DNU	State	Result
0.2	I1	Q = 0	A	2.2	I1	Q = 1	A
0.4	I2	Q = 0	A	2.4	I2	Q = 1	A
0.6	I4, I8	Q = 0	A	2.6	I4, I8	Q = 1	A
0.8	I4, I6	Q = 0	B	2.8	I4, I6	Q = 1	A
4.3	I3, I7	Q = 0	A	6.3	I3, I7	Q = 1	A
4.7	I3, I5	Q = 0	B	6.7	I3, I5	Q = 1	B
8.3	I1, I8	Q = 0	A	10.7	I1, I8	Q = 1	B
8.7	I3, I8	Q = 0	B	10.3	I3, I8	Q = 1	A

latch design. In Table 1, the results A and B denote "Completely self-recoverable" and "Completely tolerant", respectively. It can be seen from Table 1 that any key SNU can get an "A" demonstrating that the LCDNUT latch is completely self-recoverable from any SNU. However, as for the 12 states for DNUs, there are 5 states of "B", meaning that the LCDNUT latch design cannot completely self-recover from any DNU but the latch can completely tolerate any DNU. Therefore, the following conclusions can be drawn.

(1) The latch can completely self-recover from any SNU, demonstrating that the storage module is completely self-recoverable from any SNU no matter what value (1 or 0) is stored.
(2) The cases D1, D2 and D3 are validated. The latch can completely tolerate any DNU though the storage module can completely self-recover, or partially self-recover, or cannot self-recover from a DNU.
(3) As for any DNU, two (let alone three and four) of the internal nodes I1, I3, I5, and I7 cannot be simultaneously flipped to wrong values (the worse case is that one is flipped and another one enters into an undetermined state, e.g., the DNU at $<$I4, I6$>$ in Figure 4 results in that I6 is flipped but I4 enters into an undetermined state, and meanwhile, I5 is flipped but I7 enters into an undetermined state) and the other two nodes are correct. This is also true for the internal nodes I2, I4 I6, and I8, no matter what value (1 or 0) is stored.

As mentioned above for Case D2, the DNU at $<$I3, I5$>$ results in that I4 can be flipped no matter what value (1 or 0) is stored and hence the C-element enters into a high impedance state. At this time, if Q is simultaneously flipped, Q cannot self-recover through the C-element. In other words, the LCDNUT latch cannot tolerate the TNU at $<$I3, I5, Q$>$. Therefore, the latch cannot completely tolerate any TNU since a counter-example, i.e., the TNU at $<$I3, I5, Q$>$, can be easily found. In order to achieve complete TNU tolerance, we propose a novel TNU completely tolerant latch design in the following.

B. PROPOSED TNU COMPLETELY TOLERANT LATCH DESIGN

Figure 5 shows the schematic of the proposed Low Cost and TNU-completely Tolerant (LCTNUT) latch design. The

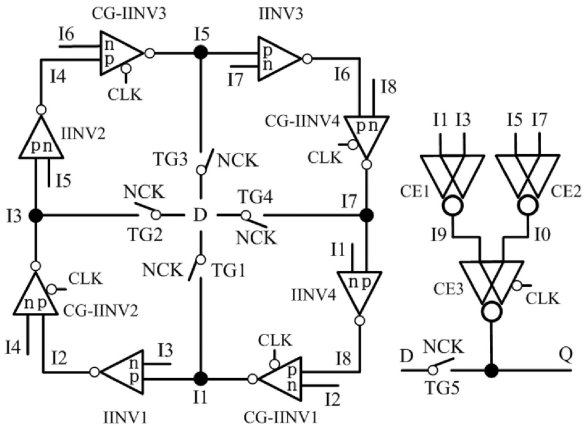

FIGURE 5. Schematic of the proposed LCTNUT latch design.

main idea is to intercept the errors accumulated in the storage module. It can be seen from Figure 5 that the latch is mainly constructed by replacing the CG-based 3-input C-element in the LCDNUT latch with a CG-based 2-input C-element (i.e., CE3) whose inputs (i.e., I9 and I0) are respectively connected to the outputs of two 2-input C-elements (i.e., CE1 and CE2). Other details are the same to that of the LCDNUT latch design.

Next, the SNU/DNU/TNU tolerance principles for the LCTNUT latch are discussed. In the presence of an SNU, if the storage module or Q is affected, as discussed for the LCDNUT latch, the latch can completely self-recover from the SNU. If I9 or I0 is affected, since the nodes in the storage module correctly retain values, I9 or I0 can also self-recover. Therefore, the LCTNUT latch is completely SNU self-recoverable. In the following, we consider the four possible cases where a pair of nodes is affected by a DNU.

Case D1. This is the same as the Case D1 discussed for the storage module. Furthermore, as for a DNU, since three (let alone four) of I1, I3, I5, and I7 cannot be simultaneously flipped as mentioned in (c) of the three important conclusions for the storage module, the worse scenario is that either I9 or I0 is flipped and the other one of them is correct. Hence, CE3 can retain its correct value on Q, i.e., the latch can completely tolerate this kind of DNUs.

Case D2. This is the same as the Case D2 discussed for the storage module. It is also the same as the above Case D1 discussed for the LCTNUT latch. Hence, the detailed analysis for this case is omitted and we only provide the conclusion that the latch can completely tolerate this kind of DNUs.

Case D3. This is the same as the Case D3 discussed for the storage module. It is also the same as the above Case D1 discussed for the LCTNUT latch. Hence, the detailed analysis for this case is omitted and we only provide the conclusion that the latch can completely tolerate this kind of DNUs.

Case D4. Either no or one node is affected in the storage module. If no node is affected in the storage module, the two nodes affected by a DNU should be two of I9, I0, and Q (e.g., $<$I9, I0$>$). Besides, if one node is affected in the storage module, another node should be one of I9, I0, and Q

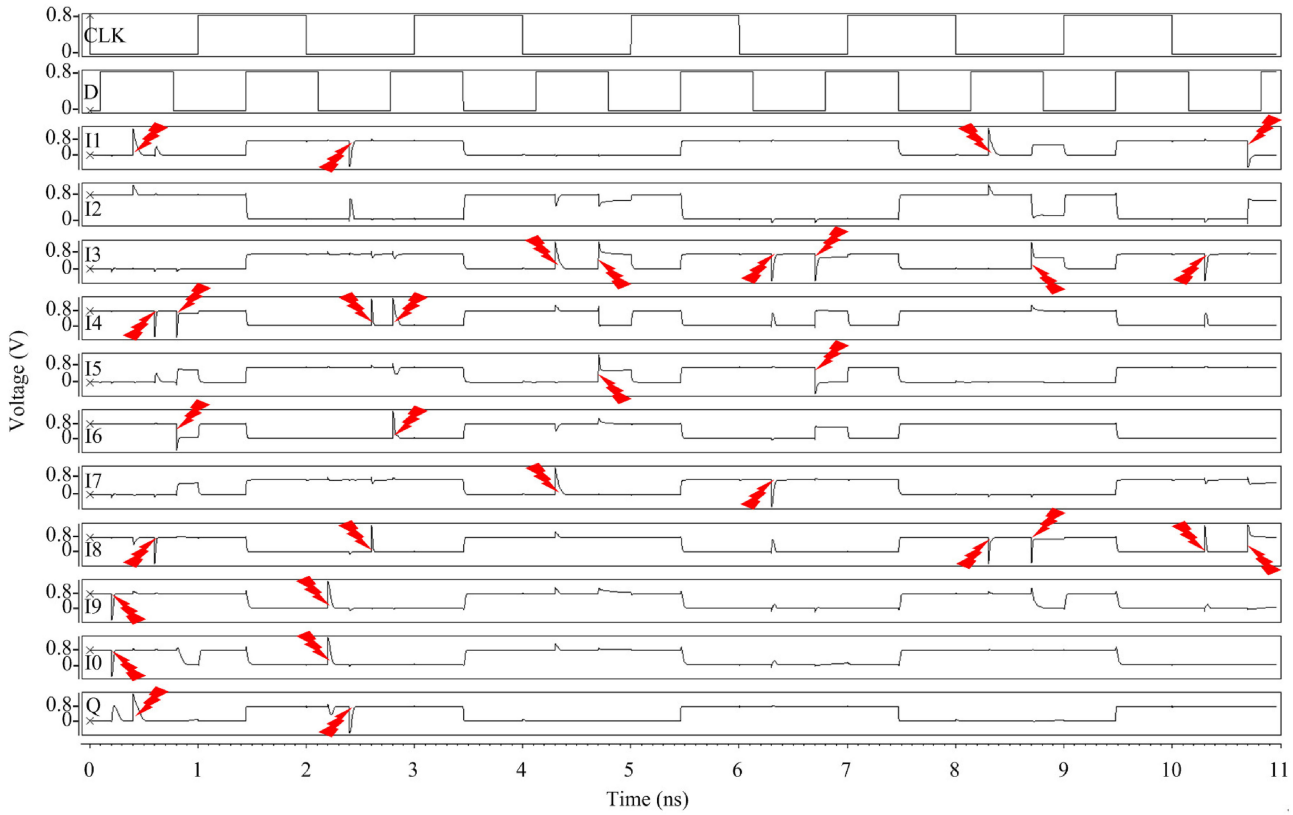

FIGURE 6. **Simulation results for the key DNU injections of the LCTNUT latch design.**

(e.g., $<$I1, Q$>$). Obviously, the storage module can always retain correct values in this case and hence all nodes in the latch can completely self-recover from the DNU through the storage module.

As discussed above, the LCDTNUT latch can tolerate any DNU since Q is always correct although some nodes cannot self-recover from a DNU. In the following, we consider the four possible cases where a node-list is affected by a TNU.

Case T1. This is the same as the Case T1 discussed for the storage module. Furthermore, as for a TNU, since three (let alone four) of I1, I3, I5, and I7 cannot be simultaneously flipped as mentioned in (c) of the three important conclusions for the storage module, the worse scenario is that one of I9 and I0 is flipped and another one of I9 and I0 is correct. Hence, CE3 can retain its correct value on Q, i.e., the latch can completely tolerate this kind of TNUs.

Case T2. This is the same as the Case T2 discussed for the storage module. It is also the same as the above Case T1 discussed for the LCTNUT latch. Hence, the detailed analysis for this case is omitted and we only provide the conclusion that the latch can completely tolerate this kind of TNUs.

Case T3. This is the same as the Case T3 discussed for the storage module. It is also the same as the above Case T1 discussed for the LCTNUT latch. Hence, the detailed analysis for this case is omitted and we only provide the conclusion that the latch can completely tolerate this kind of TNUs.

Case T4. Two nodes are affected in the storage module, and simultaneously, one node of I9, I0, and Q is affected (e.g., $<$I3, I5 I9$>$ and $<$I3, I5, Q$>$). As for any DNU in the storage module, according to (b) of the three important conclusions for the storage module mentioned above, two of the internal nodes I1, I3, I5, and I7 cannot simultaneously flipped to wrong values and the other two nodes are correct, resulting that I9 and I0 can always retain correct values through CE1 and CE2, respectively. However, if the third node I9 or I0 is affected, Q can retain its correct value since I9 and I0 cannot simultaneously be flipped. If the third node Q is affected, Q can self-recover through CE3 by the correct I9 and I0. Therefore, the latch can completely tolerate this kind of TNUs.

Case T5. Either no or one node is affected in the storage module. If no node is affected in the storage module, the triple nodes affected by a TNU should be $<$I9, I0, Q$>$. Besides, if one node is affected in the storage module, another two nodes should be two of I9, I0 and Q. Obviously, the storage module can always retain correct values in this case and hence all nodes in the latch can completely self-recover from the DNU through the storage module.

Figure 6 shows the simulation results for the key DNU injections of the LCTNUT latch design. According to Figure 6, Table 2 shows the statistic results for the key DNU injections of the LCTNUT latch design. It can be seen that Figure 6 is almost the same as Figure 4, and so does that for Table 2 vs. Table 1, demonstrating that the LCTNUT latch is partially DNU self-recoverable and completely DNU-tolerant.

TABLE 2. Statistic results for the key DNU injections of the LCTNUT latch design according to Fig. 6.

Time (ns)	SNU/ DNU	State	Result	Time (ns)	SNU/ DNU	State	Result
0.2	I9, I10	Q = 0	A	2.2	I9, I10	Q = 1	A
0.4	I1, Q	Q = 0	A	2.4	I1, Q	Q = 1	A
0.6	I4, I8	Q = 0	A	2.6	I4, I8	Q = 1	A
0.8	I4, I6	Q = 0	B	2.8	I4, I6	Q = 1	A
4.3	I3, I7	Q = 0	A	6.3	I3, I7	Q = 1	A
4.7	I3, I5	Q = 0	B	6.7	I3, I5	Q = 1	B
8.3	I1, I8	Q = 0	A	10.7	I1, I8	Q = 1	B
8.7	I3, I8	Q = 0	B	10.3	I3, I8	Q = 1	A

Figure 7 shows the simulation results for the key TNU injections of the LCTNUT latch design. Note that, in all the above simulations, a controllable double exponential current source model was used to perform all the SNU/DNU/TNU injections [15], [18]. The time constant of the rise and fall of the current pulse was set to be 0.1ps and 3ps, respectively. The worst case deposited charge was chosen to be up to 45fC for a single node, which was large enough since the purpose was to validate the circuit operation under extreme SNU/DNU/TNU conditions that might disturb circuit nodes.

According to Figure 7, Table 3 shows the statistic results for the key TNU injections of the LCTNUT latch design. In Table 3, the results A and B have the same meanings as mentioned above. It can be seen from Table 3 that any key TNU can get either an "A" or "B" demonstrating that the LCTNUT latch is partially TNU self-recoverable and completely TNU-tolerant.

TABLE 3. Statistic results for the key TNU injections of the LCTNUT latch design according to Fig. 7.

Time (ns)	SNU/ DNU	State	Result	Time (ns)	SNU/ DNU	State	Result
0.7	I1, I2, I3	Q = 0	B	20.7	I1, I2, I4	Q = 0	B
2.7	I1, I2, I3	Q = 1	B	22.7	I1, I2, I4	Q = 1	A
4.7	I2, I3, I4	Q = 0	B	24.7	I3, I4, I7	Q = 0	B
6.7	I2, I3, I4	Q = 1	B	26.7	I3, I4, I7	Q = 1	A
8.7	I1, I3, I5	Q = 0	B	28.7	I5, I6, I8	Q = 0	B
10.7	I1, I3, I5	Q = 1	B	30.7	I5, I6, I8	Q = 1	A
12.7	I1, I4, I6	Q = 0	B	32.7	I3, I5, I9	Q = 0	B
14.7	I1, I4, I6	Q = 1	A	34.7	I3, I5, I9	Q = 1	B
16.7	I1, I5, I7	Q = 0	B	36.7	I3, I5, Q	Q = 0	B
18.7	I1, I5, I7	Q = 1	B	38.7	I3, I5,Q	Q = 1	B

IV. COMPARISONS

For fair comparisons, the proposed latch designs and typical SNU/DNU/TNU hardened latch designs, namely the FERST [10], RFC [15], HRPU [16], DNCS [17], DNUR [18], NTHLTCH [19] and TNUHL [1] were designed in the same 22nm CMOS technology using the predictive technology model (PTM) in [23]. The supply voltage Vdd was set to 0.8V. The transistor sizes in these latch designs were set to be comparable, e.g., as for all TGs, the pMOS transistor had W/L = 100/22 nm while the nMOS transistor had

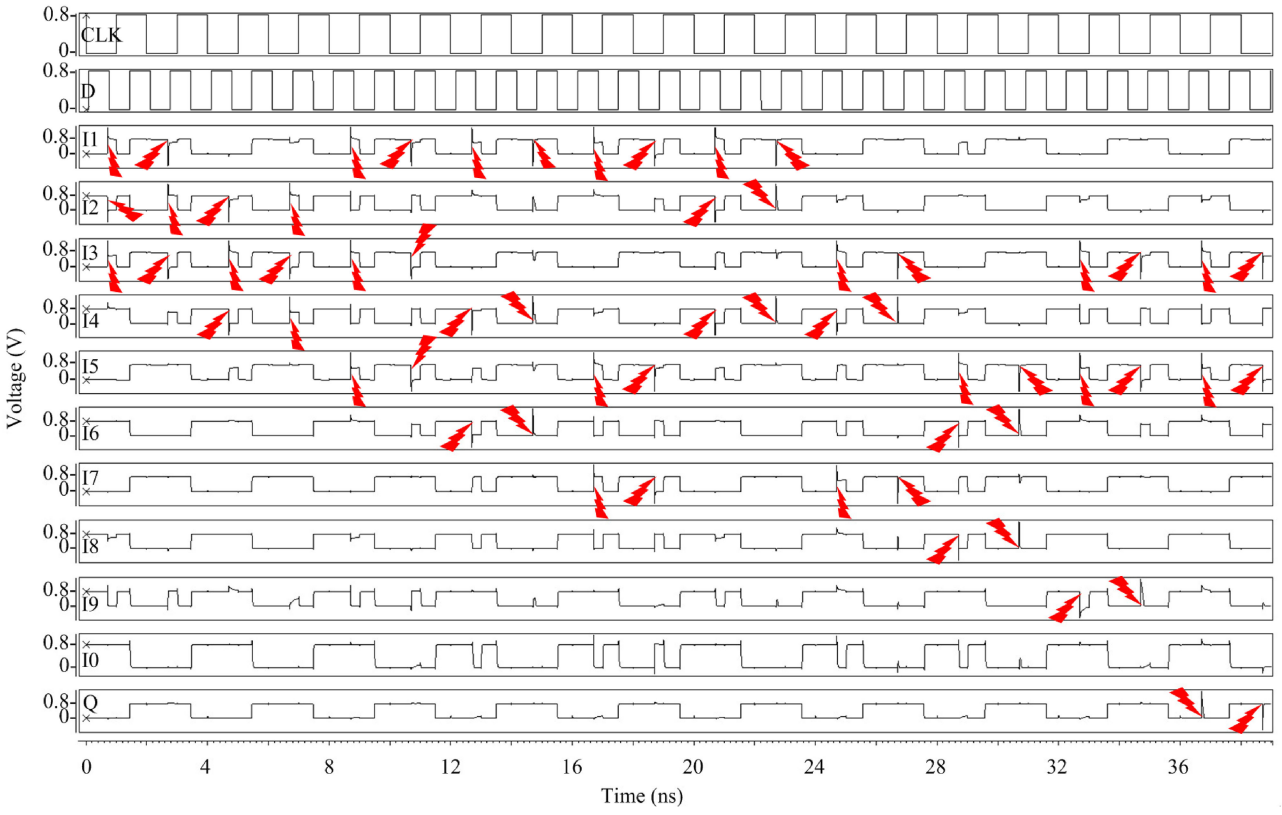

FIGURE 7. Simulation results for the key TNU injections of the LCTNUT latch design.

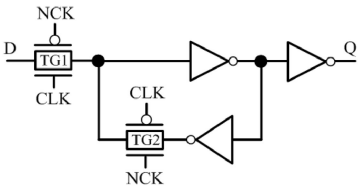

FIGURE 8. Schematic of the unhardened latch (the traditional static D latch).

W/L = 28/22 nm. Besides, the unhardened latch, i.e., the traditional static D latch as shown in Figure 8 was also designed using the same conditions mentioned above for a comparison.

First, in order to make a qualitative comparison, the reliability comparisons among the SNU, DNU, and/or TNU hardened latch designs are shown in Table 4. It can be seen from Table 4 that, the unhardened latch cannot completely tolerate any upset, thus it has a large sensitivity to soft errors. The FERST latch is a SNU-tolerant one, but it cannot completely self-recover from an SNU since there is at least a C-element whose output is feeding back to one of its inputs. Besides, the FERST latch cannot completely tolerate any DNU (let alone TNU) since the inputs of the C-element at the output stage can be completely flipped. As we can see, the latches like RFC and HRPU achieve the SNU resiliency. However, they cannot completely tolerate any DNU (let alone TNU) as mentioned in Section II (Typical Latch Designs). On the other hand, the latches, such as DNCS, DNUR, NTHLTCH, achieve DNU tolerance, but cannot completely tolerate any TNU. Furthermore, it can be seen from Table 4 that there are the same types of latches compared with ours; however ours have lower costs.

Second, in order to make a quantitative comparison, the overhead comparisons among the SNU, DNU, and/or TNU hardened latch designs are shown in Table 5. Note that, the comparison data were extracted by conducting pertinent simulations using HSPICE tool with all the simulation conditions mentioned above. In Table 5, "Delay" means D to Q transmission delay, i.e., the average of rise and fall delays of D to Q. "Power" means the average of dynamic and static power dissipation. "Area" means silicon area measured with

TABLE 4. Reliability comparisons among the SNU, DNU, and/or TNU hardened latch designs.

Latch	Ref.	SNU Tolerant	SNU Resilient	DNU Tolerant	TNU Tolerant
Unhardened	-	×	×	×	×
FERST	[10]	√	×	×	×
RFC	[15]	√	√	×	×
HRPU	[16]	√	√	×	×
DNCS	[17]	√	√	√	×
DNUR	[18]	√	√	√	×
NTHLTCH	[19]	√	√	√	×
TNUHL	[1]	√	√	√	√
LCDNUT	Proposed	√	√	√	×
LCTNUT	Proposed	√	√	√	√

TABLE 5. Overhead comparisons among the SNU, DNU, and/or TNU hardened latch designs.

Latch	Delay (ps)	Power (μW)	$10^{-4}\times$ Area (nm^2)	$10^{-6}\times$ DPAP
Unhardened	13.95	0.38	1.41	0.07
FERST	54.81	1.23	5.04	3.40
RFC	3.74	0.49	3.86	0.07
HRPU	13.06	0.86	4.68	0.53
DNCS	67.38	2.15	7.86	11.39
DNUR	4.61	1.52	12.52	0.88
NTHLTCH	14.95	2.03	8.56	2.60
TNUHL	70.32	2.69	12.93	24.46
LCDNUT	3.89	0.61	5.58	0.13
LCTNUT	3.95	0.66	5.59	0.15

Eq. (1). In Eq. (1), $n1$ denotes the number of nMOS, $L_{\mathrm{nMOS}}(i)$ and $W_{\mathrm{nMOS}}(i)$ denote the effective length and width of each nMOS, respectively. Similarly, $n2$ denotes the number of pMOS, $L_{\mathrm{pMOS}}(i)$ and $W_{\mathrm{pMOS}}(i)$ denote the effective length and width of each pMOS, respectively. "DPAP" means the delay-power-area product calculated by multiplying the delay, power, and area to comprehensively evaluate overheads of latch designs.

$$\begin{aligned}\mathrm{Area} = &\sum_{i=1}^{n1} L_{\mathrm{nMOS}}(i) * W_{\mathrm{nMOS}}(i) \\ &+ \sum_{i=1}^{n2} L_{\mathrm{pMOS}}(i) * W_{\mathrm{pMOS}}(i)\end{aligned} \tag{1}$$

It can be seen from Table 5 that the delay is comparable and small for the proposed latch designs, including our previously published designs, namely the RFC and DNUR, since a high speed transmission path from D to Q was used for these designs. As for power dissipation, due to the smaller silicon area, the first 4 latch designs including ours consume less power. However, the power dissipation of the FERST latch is higher since the feedback loop at Q in the latch is constructed even in transparent mode of operation. In order to achieve DNU/TNU tolerance, a larger silicon area needs to be used so as to ensure sufficient redundant nodes and feedback loops. In other words, the silicon area of the 5 to 8 latch designs is large. Hence, their power dissipation is also large. The power dissipation of the DNUR latch is smaller due to the use of clock-gating technology. Furthermore, since only a few input-split inverters were used to retain data, one or three C-elements were used to intercept the errors accumulated in the upstream storage module, the transistor count and the silicon area of our designs are small, resulting in less power dissipation. It can be seen that, among the DNU and/or TNU-tolerant latch designs as compared in Table 5, the DPAP of ours is small due to the mentioned small delay, power dissipation and silicon area for ours. Therefore, the cost of our proposed latch designs is low.

On the other hand, a quantitative conclusion can be drawn from Table 5 that, compared with the same type state-of-the-art TNU-tolerant TNUHL latch design, the proposed LCTNUT design reduces delay by approximately 94.38 percent, power

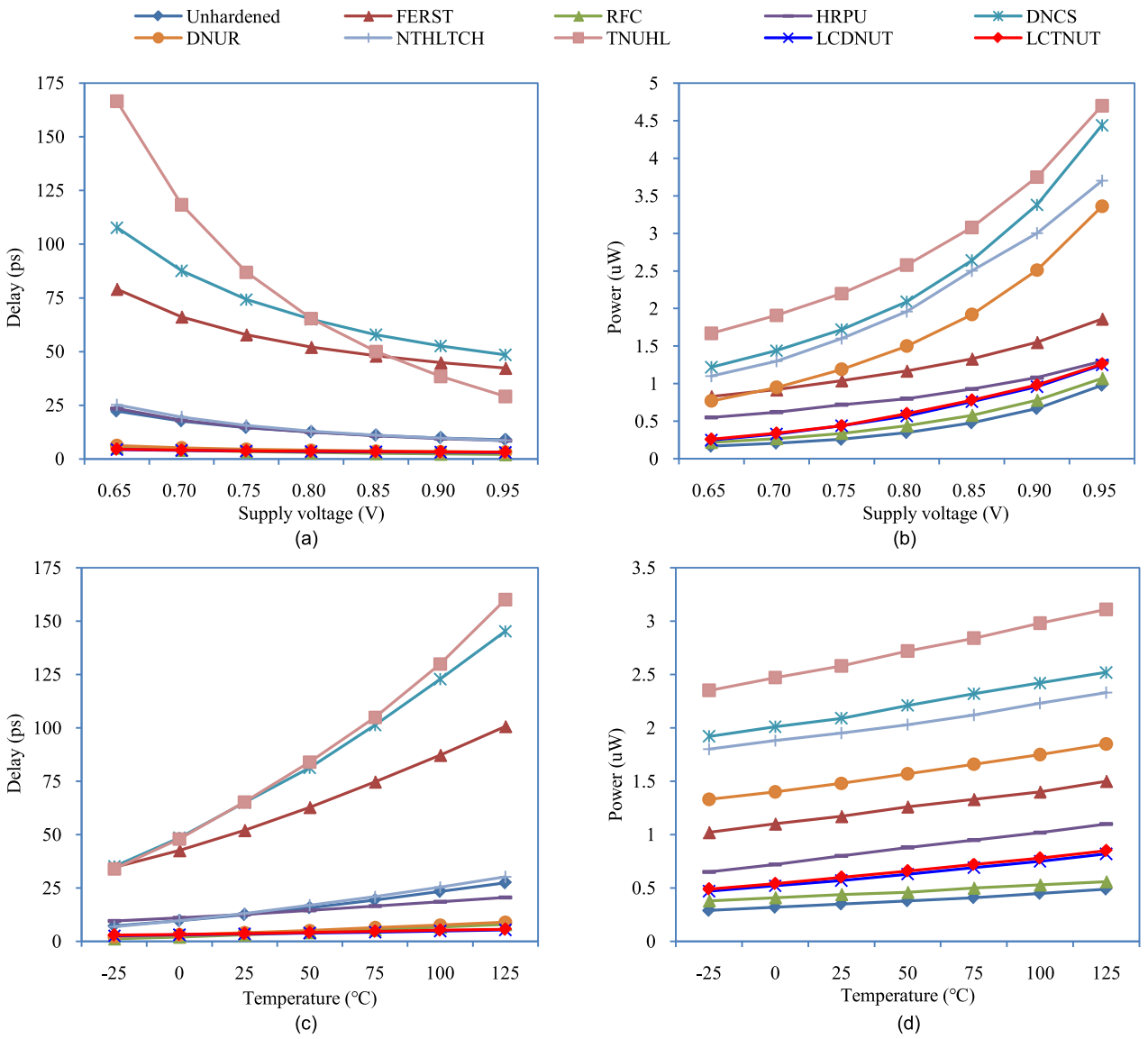

FIGURE 9. Estimation results of the supply voltage and temperature variation effects on delay and power for latches. (a) Supply voltage vs. Delay. (b) Supply voltage vs. Power. (c). Temperature vs. Delay. (b) Temperature vs. Power.

dissipation by approximately 75.46 percent, silicon area by approximately 56.77 percent, and DPAP by approximately 99.39 percent on average. It can be seen from Figure 1g that, the TNUHL latch comprises 82 transistors, which is almost $(82-48)/48 \times 100\% = 70.83\%$ more than our proposed LCTNUT latch that has only 48 transistors. Hence, the silicon area of the TNUHL latch is too large. As a result, the power dissipation of the TNUHL latch is too high. Besides, from D to Q, there are three C-elements and two inverters in the TNUHL latch, resulting in transmission delay that is too large. Hence, the DPAP of the TNUHL latch is also too large. In other words, although the TNUHL latch design of the same type can also be highly reliably operated, it brings about very large cost penalties on the delay, power, area, and DPAP.

Third, the process, voltage and temperature (PVT) variation effects on latches were still estimated, since latches are more sensitive to PVT variation effects especially in the nano-scale CMOS technology [24]. Using the PVT estimation methodologies in [24], Figure 9 shows the estimation results of the supply voltage and temperature variation effects on delay and power for latches. The normal supply voltage was set to 0.8V and the supply voltage variation was varied from 0.65V to 0.95V. The normal temperature was set to 25°C and the temperature was varied from −25°C to 125°C. In Figs. 9a and 9b, the supply voltage variation effect on delay and power is shown, and in Figs. 9c and 9d, the temperature variation effect on delay and power is shown.

It can be seen from Figure 9a that the delay of the TNUHL latch has the largest variation and sensitivity to the supply voltage variation effect, since the latch employs multiple-level C-elements for the interception of TNUs. Meanwhile, the delay of the DNUR, RFC, LCDNUT and LCTNUT latches has a similar-and-very-low variation and sensitivity to the supply voltage variation effect, since these latches

TABLE 6. Normalized average deviation (dev) and standard deviation (σ) for power of latches.

	Unhardened	FERST	RFC	HRPU	DNCS	DNUR	NTHLTCH	TNUHL	LCDNUT	LCTNUT
dev	1.00	2.29	1.84	1.21	2.90	3.16	2.67	3.21	2.44	2.48
σ	1.00	2.34	1.87	1.23	2.93	3.20	2.73	3.23	2.46	2.49

TABLE 7. Normalized average deviation (dev) and standard deviation (σ) for delay of latches.

	Unhardened	FERST	RFC	HRPU	DNCS	DNUR	NTHLTCH	TNUHL	LCDNUT	LCTNUT
dev	1.00	1.88	0.89	0.88	2.17	0.91	1.31	3.13	0.87	0.90
σ	1.00	1.91	0.91	0.91	2.20	0.94	1.33	3.07	0.89	0.92

employ a high-speed transmission path from D to Q to improve performance as in [8], [13]. It can be seen from Figure 9b that the power of the DNCS latch has the largest variation and sensitivity to the supply voltage variation effect, since the latch employs a very-large feedback loop to retain data. The power of the TNUHL and DNUR latches still has a larger variation and sensitivity to the supply voltage variation effect, since the area of these latches is large. Meanwhile, the delay of the LCDNUT and LCTNUT latches has a similar-and-lower variation and sensitivity to the supply voltage variation effect, since these latches employ clock-gating technology and fewer transistors. Similar to Figure 9a, it can be seen from Figure 9c that the delay of the TNUHL latch has the largest variation and sensitivity to the temperature variation effect, and meanwhile, the delay of the DNUR, RFC, LCDNUT and LCTNUT latches has a similar-and-very-low variation and sensitivity to the temperature variation effect. Similar to Figure 9b, it can be seen from Figure 9d that the power of the TNUHL latch has a larger variation and sensitivity to the temperature variation effect, and meanwhile, the power of the LCDNUT and LCTNUT latches has a similar-and-lower variation and sensitivity to the temperature variation effect. In summary, the proposed latches have a lower sensitivity on the variation effects of supply voltage and temperature.

On the other hand, to investigate the process variation effect on latches, Monte Carlo simulations were still performed using the PVT estimation methodologies in [24]. The threshold voltage and oxide thickness of transistors are generated randomly using the normal distribution with ± 5 percent maximum deviations from the original [9]. Note that, the negative varied values (less than the original ones) on the normal distribution curves for the effective channel length of transistors are mapped to positive ones by coordinate transformation in the HSPICE netlist file, since these variations are almost impossible [24]. To get parameters of average deviation (dev) and standard deviation (σ) for latches, 500 times' Monte Carlo simulations were performed, and the calculation formulas for these parameters are given in the following.

$$dev = \frac{\sum |X_i - \varphi|}{N} \tag{2}$$

$$\sigma = \sqrt{\frac{\sum (X_i - \varphi)^2}{N}}. \tag{3}$$

In Eq. (2) and (3), N, X_i and φ denote the number of sample values that is 500, the sample values and the standard value that is 1 due to the normalization, respectively. Accordingly, the normalized average deviation (dev) and standard deviation (σ) for power and delay of latches are calculated and shown in Tables 6 and 7. From Table 6, three conclusions can be drawn. First, compared with the unhardened latch, all the hardened latches have a larger sensitivity to the process variation effect for power, which may due to the increased area for hardening. Second, the TNUHL latch has the largest sensitivity to the process variation effect for power since its area is the largest. Third, the LCDNUT and LCTNUT latches have a similar-and-lower sensitivity to the process variation effect for power, compared with the TNUHL latch. From Table 7, three conclusions can still be drawn. First, compared with the unhardened latch, the RFC, HRPU, DNUR, LCDNUT and LCTNUT latches have a lower sensitivity to the process variation effect for delay, which may due to the employment of the high-speed transmission path from D to Q. Second, the TNUHL latch has the largest sensitivity to the process variation effect for delay, which may due to the employment of the multiple-level C-elements for the interception of TNUs. Third, the LCDNUT and LCTNUT latches have a similar-and-lower sensitivity to the process variation effect for delay, compared with the TNUHL latch. In summary, the proposed latches have a lower sensitivity on the PVT variation effects, compared with the state-of-the-art TNUHL latch.

V. CONCLUSION

As technology scaling, the advanced CMOS integrated circuits are likely to experience the occurrence of a double-node-upset or triple-node upset. This paper has presented two DNU and/or TNU hardened latch designs. First, employing four input-split inverters and four clock-gating based input-split inverters, a storage module with 8 storage nodes is constructed. Since any triple nodes that have the same logic values cannot be flipped simultaneously, a 3-input C-element is used to intercept the accumulated errors in the

storage module to construct the LCDNUT latch to completely tolerate any DNU. Second, in order to completely tolerate any TNU, due to the special features of the storage module, a two-level error-interceptive module using three C-elements is constructed and applied to the storage module to construct the LCTNUT latch. Furthermore, using the high-speed transmission paths, the clock-gating technology and fewer transistors, the costs of the latches are very low. Simulation results have validated the robustness and low costs of the proposed latches. Compared with the state-of-the-art TNUHL latch, the sensitivity to the PVT variation effects for the proposed latches is still low.

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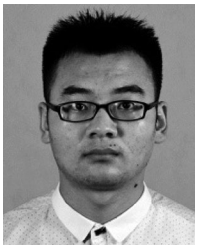
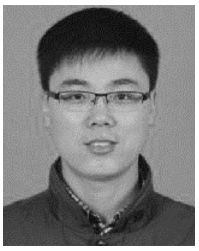
AIBIN YAN received the MS degree in software engineering from the University of Science and Technology of China (USTC), Hefei, in 2015, and the PhD degree in computer application technology from the Hefei University of Technology, in 2009. He is currently working with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China. Currently, he is a supervisor of graduate and undergraduate students. His research interests include soft error rate analysis (SERA), the nano-scale CMOS integrated circuit design automation by developing novel simulation tools, and radiation hardening by design for the nano-scale CMOS integrated circuits like latches, flip-flops and memory cells.

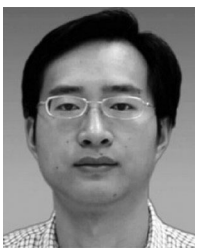
CHAOPING LAI is currently working toward the bachelor's degree in computer science and technology major, and is currently working with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China. His research interests include soft error rate analysis (SERA) and radiation hardening by design for the nano-scale CMOS integrated circuits like latches, flip-flops and memory cells.



YINLEI ZHANG is currently working toward the bachelor's degree in computer science and technology major, and is working with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China.His research interests include the nano-scale CMOS integrated circuit design automation by developing novel simulation tools as well as radiation hardening by design for the nano-scale CMOS integrated circuits like latches, flip-flops and memory cells.



JIE CUI received the PhD degree from the University of Science and Technology of China, Hefei, in 2012. Currently, he is an associate professor with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China. His research interests include IoT security, applied cryptography, software-defined networking, vehicular ad hoc network and radiation hardening for nanoscale ICs.



ZHENGFENG HUANG received the PhD degree from the Hefei University of Technology, Hefei, China, in 2009. In 2014 he was a visiting scholar at the University of Paderborn, Germany. Currently he is a doctoral eesearcher and postgraduate supervisor with the School of Electronic Science & Applied Physics, Hefei University of Technology, Hefei, China. His research interests include VLSI design and test, radiation hardening by design for the nano-scale CMOS integrated circuits and so on.

JING GUO received the BS and MS degrees in electronic science and technology from Heilong Jiang University, Harbin, China, in 2008, and 2011, respectively. He received the PhD degree in microelectronics and solid-state electronics from the Harbin Institute of Technology, Harbin, China, in 2015. He is now an associate professor with the National Key Laboratory for Electronic Measurement Technology and the Key Laboratory of Instrumentation Science and Dynamic Measurement, North University of China, Taiyuan, China. He is the author of 6 technical papers in IEEE journals, *including IEEE Trans. VLSI*, *IEEE Trans. Reliab.*, *IEEE Trans. Circuits Syst.-I: Reg. Papers*, and *IEEE Micro*. He is also the coauthor of more than 2 technical papers in *IEEE Trans. Nucl. Sci.*, and *Microelectronics Reliab.*. His research interests include fault tolerance in VLSI designs, and reliability in memories.

XIAOQING WEN (M'89-SM'08-F'12) received the BE degree from Tsinghua University, China, in 1986, the ME degree from Hiroshima University, Japan, in 1990, and the PhD degree from Osaka University, Japan, in 1993. From 1993 to 1997, he was an assistant professor with Akita University, Japan. He was a visiting researcher with the University of Wisconsin, Madison, USA, from Oct. 1995 to Mar. 1996. He joined SynTest Technologies, Inc., USA, in 1998, and served as its chief technology officer until 2003. In 2004, he joined Kyushu Institute of Technology, Japan, where he is currently a professor and the chair of the Department of Creative Informatics. He founded Dependable Integrated Systems Research Center in 2015 and served as its director until 2017. His research interests include VLSI test, diagnosis, and testable design. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (Springer, 2009). He holds 43 U.S. Patents and 14 Japan Patents on VLSI testing. He received the 2008 IEICE-ISS Best Paper Award for his pioneering work on X-filling-based low-capture-power test generation. He is a fellow of the IEEE, a member of the IEICE, the IPSJ, and the REAJ. He is serving as associate editors for *IEEE Trans. on Computer-Aided Design*, *IEEE Trans. on VLSI*, and the *J. of Electronic Testing: Theory and Applications*.