Digital Object Identifier 10.1109/TETC.2020.2998932

Guest Editor's Introduction: Special Section on Reliability-Aware Design and Analysis Methods for Digital Systems: From Gate to System Level

ANTONIO MIELE, (Member, IEEE), QIAOYAN YU, (Senior Member, IEEE), AND MARIA K. MICHAEL, (Member, IEEE)

A. Miele is with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, 20133 Milano, Italy
Q. Yu is with the Department of Electrical and Computer Engineering, University of New Hampshire, Durham NH 03824, USA
M. K. Michael is with the Department of Electrical and Computer Engineering and the KIOS Research and Innovation Center of Excellence, University of Cyprus, Nicosia 2109, Cyprus

The continuous scaling of CMOS devices as well as the increased interest in the use of emerging technologies make more and more important the topics related to defect and fault tolerance in digital systems. To address the increasing complexity of digital systems and their challenging reliability requirements, it is imperative to employ design and analysis methods to different levels of the abstraction, starting from the system level down to the gate level.

The focus of this Special Section is on investigating novel solutions for the reliability-aware design and analysis in digital systems, comprising a large number of issues and aspects (e.g. fault tolerance techniques, circuit aging and security), focusing on various architectures and devices (such as combinatorial circuits, memories, NoCs or FPGAs), and acting at different levels of abstraction (from circuit level to system level). The special issue comprises 14 articles selected with a rigorous review process from 51 initial submissions.

The guest editors would like to thank the reviewers for the quality and timeliness of their reviews. The reviewers have helped to raise the quality of the final submissions of this issue through their quality feedback. We thank the authors for their patience, diligence and dedication at all stages of the review process. Finally, we are grateful to the current and past Editors-in-Chief of the *IEEE Transactions on Emerging Topics in Computing*, Prof. Cecilia Metra and Prof. Fabrizio Lombardi respectively, for making this special section possible.

The first article, "Scrubbing-aware Placement for Reliable FPGA Systems," focuses on the minimization of the execution time of the scrubbing method, used to correct single event upsets (SEUs) in the FPGA configuration memory. The proposed approach consists in a reliability-aware Simulated Annealing placement algorithm to properly organize the system under design on the FPGA reconfigurable elements.

The second article, "Scalable design methodology and online algorithm for TSV-cluster defects recovery in highly reliable 3D-NoC systems," proposes a scalable and efficient Through Silicon Vias (TSVs) usage and design method for 3D-NoC architectures to overcome open defects. The paper presents also an adaptive online algorithm to assist the proposed system to immediately work around the newly detected defects without using redundancies.

The third article, "A Flexible Scan-in Power Control Method in Logic BIST and Its Evaluation with TEG Chips," focuses on the critical issue of High power dissipation in scan-based logic built-in self-test (LBIST). The proposed method receives pseudo-random patterns received from an embedded test pattern generator (TPG) and modifies them to have the specified toggle rate without sacrificing fault coverage and test time.

The fourth article, "Reliability Aware Design and Lifetime Management of Computing Platforms," proposes a reliability-aware design and lifetime management framework aimed 1) at design-time, at defining a reliability enhanced adaptive architecture fabric for the system under design, and 2) at run-time, at monitoring and dynamically managing fabrics wear-out profile in order to fulfill the used-defined Quality-of-Service requirements.

The fifth article, "Radiation Hardened Latch Designs for Double and Triple Node Upsets," proposes new latch design methods to tolerate double and triple node upsets. The proposed radiation hardened latch is more power efficient than existing latch designs for clock gating.

The sixth article, "Self-Adjusting Monitor for Measuring Aging Rate and Advancement," proposes an online, adjustable and configurable monitoring structure that predicts the age of the system and detects progressive changes in delay, and provides the required information about the present state of the system and its aging rate. Dual sampling is performed on the data propagated to monitored nodes and then the two samples are compared for consistency to set a warning flag.

The proposed sampling with a negative phase shift is able to predict the system aging before a failure occurs.

The seventh article, "A Dynamic Sufficient Condition of Deadlock-Freedom for High-Performance Fault-Tolerant Routing in Networks-on-Chips," addresses the throughput underutilization issues induced by the routing algorithms that are overly restrictive and static partitioning of virtual channels (VCs). That article presents a generic, topology-agnostic routing algorithm design methodology to construct highly flexible routing algorithms. As the proposed routing provides packets with a very high degree of routing freedom, the NoC can switch freely between classes.

The eighth article, "Securing Cyber-Physical Systems from Hardware Trojan Collusion," aims for protecting Cyber-Physical Systems (CPS) from simultaneously activated multiple Trojans. The proposed defense framework is a collaboration of network deployment and runtime detection stages. When deploying the network, a security requirement that any pair of neighboring nodes are from different vendors is enforced. At runtime, a mutual auditing protocol is utilized to check whether it is correctly encrypted by the source node and whether its content is maliciously changed by any other node on the routing path. That framework effectively prevents hardware Trojan collusion with low latency overhead and almost no impact on packet completion rate and network throughput.

The 9th article, "On the Theory and Design of Polynomial Division Circuits," proposes a theoretical analysis method to estimate the aliasing rate for the polynomial division circuits. Two types of scalable design techniques are examined for mixed-signal circuit analyzers. The proposed devices have both low hardware complexity and aliasing rate. That work also proposes design techniques and devices for general arithmetic/algebraic error-control coding, cryptography, digital broadcasting and communication.

A new design-for-trust technique to increase the immunity of a design against a Trojan attacks is proposed in the next article entitled "A Novel Low Complexity Logic Encryption Technique for Design-for-Trust." The authors propose a new encryption algorithm which reduces the number of vulnerable-nets with minimum overhead, using light-weight gate topologies.

The article "Memory Physical Aware Multi-Level Fault Diagnosis Flow" provides a further insight to multi-level based fault detection and diagnosis methods for memories, by proposing a generalized flow which utilizes scrambling for physical aware fault diagnosis. The approach applies to both planar and FinFET memories. Furthermore, it considers the classification of static and dynamic faults and validates its results using FPGA-based prototyping as well as different chips for physical failure analysis.

Safety-critical computers are considered in the next article, "Analysis of Design Parameters in Safety-Critical Computers" which, in particular, focuses on evaluating the effect of different design parameters on the safety of the system. The authors employ Markov modeling to analyse the sensitivity of safety of well known parameters such as failure rate, failure diagnostic coverage, common cost failure ration, etc, and provide new understanding on the impact of these parameters on safety.

The next article, entitled "Mitigating Process Variability for Non-Volatile Cache Resilience and Yield" addresses the issue of process variations in Non-Volatile memories caused by vulnerabilities in the sensing instrumentation. The authors propose a Self-Organized Sub-bank (SOS) design which assigns a sense amplifier to each sub-bank based on its process variation assessment. Moreover, they propose two new sense amplifiers with improved reliability and power profiles, demonstrating significant mitigation from sensing vulnerability in their SOS design.

The final article in this special section, "Gate Level NBTI and Leakage Co-optimization in Combinational Circuits with Input Vector Cycling," addresses circuit aging and proposes an approach based on input vector control to recover from NBTI stress during idle times in combinational circuits. The focus of the work is on the generation of two appropriate input vectors, via a simulated annealing followed by a deterministic process, which are applied in an alternate order. The approach is validated in 45nm technology for the ISCAS85 benchmarks, demonstrating NBTI stress improvements.

All of the articles selected for this Special Section represent world-leading current research into reliability-aware design methods for digital systems and provide interesting and valuable insights into current and future trends in the considered research areas. We hope you will enjoy reading the papers and find them a source of inspiration for your own work.

ANTONIO MIELE (Member, IEEE) received the MSc degree in computer engineering from the Politecnico di Milano, and the MSc degree in computer science from the University of Illinois at Chicago, he received the PhD degree in information technology from the Politecnico di Milano, in 2010. He is an assistant professor with the Politecnico di Milano, since 2014. His main research interests are related to the definition of design methodologies for computing systems systems, in particular focusing fault tolerance and reliability issues, runtime resource management in heterogeneous multi-/many-core systems and FPGA-based systems design. He has served on several technical program committees of international conferences, including DATE, FPL, DFT, IOLTS, and others, and guest editor for special issues in *IEEE Transactions on Emerging Topics in Computing* and *IET Computers and Digital Techniques Journals*. He is co-author of more than 70 peer-reviewed publications.

QIAOYAN YU (Senior Member, IEEE) received the BS degree from Xidian University, Xian, China, in 2002, the MS degree from Zhejiang University, Hangzhou, China, in 2005, and the PhD degree in electrical engineering from the University of Rochester, Rochester, New York, USA, in 2011. She is currently an associate professor with the Department of Electrical and Computer Engineering, University of New Hampshire, Durham, New Hampshire, USA. Her research interests include hardware security and trust, embedded system security, cyber-physical system, error control for networks-on-chip, fault-tolerance for VLSI circuits and systems. She is the recipient of the National Science Foundation CAREER Award, in 2017. She has served on the technical program committees of HOST, DAC, FDTC, Asian HOST, ISVLSI, DFT, ASP-DAC, GLSVLSI, and ISCAS. She is a member of the editorial boards of Integration, the *VLSI Journal*, *Microelectronics Journal*, and *Journal of Circuits, Systems, and Computers*.

MARIA K. MICHAEL (Member, IEEE) received the PhD degree from Southern Illinois University, USA. She is currently an associate professor at the ECE Department at the University of Cyprus. She is also a co-founding faculty member of the KIOS Center of Excellence. Prior to joining the University of Cyprus, she taught as a lecturer at the ECE Department at Southern Illinois University, and as an assistant professor of computer science and engineering at the University of Notre Dame, USA. At the University of Cyprus, she leads research activities in the areas of test and dependability in integrated and embedded systems. Her current research focuses on hardware-inspired security and cyber-security in intelligent embedded systems and industrial control systems, fault diagnosis and edge intelligence in large-scale cyber-physical systems, and dependability/reliability/availability in the hardware backbone of the computing continuum, enabling IoT and cyber-physical systems. She has published her work in more than 85 refereed journals, book chapters and international conferences. Furthermore, her research has been already funded by several local and international organizations such as EU FP7, EU H2020, EU COST, Intel Corp., and the Cyprus Research Promotion Foundation. She has been serving regularly on the Steering, Organizing and Program Committees of numerous IEEE and ACM conferences, such as DATE, VTS, ETS, DFTS, VLSISoC, IOLTS, etc.