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# Comprehensive Study of Inversion Capacitance in Metal-Insulator-Semiconductor Capacitor With Existing Oxide Charges

KUNG-CHU CHEN<sup>1</sup>, KUAN-WUN LIN<sup>1</sup> (Graduate Student Member, IEEE), SUNG-WEI HUANG<sup>1</sup>,  
JIAN-YU LIN<sup>1</sup>, AND JENN-GWO HWU<sup>1,2</sup> (Senior Member, IEEE)

<sup>1</sup> Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan

<sup>2</sup> Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan

CORRESPONDING AUTHOR: J.-G. HWU (e-mail: jghwu@ntu.edu.tw)

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**ABSTRACT** The impact of oxide charges on the metal-insulator-semiconductor (MIS) device's capacitance ( $C$ ) and conductance ( $G$ ) was studied in this work. A model to calculate MIS device's  $C$  and  $G$  under the considerations of oxide charges, doping concentration, device dimension, and AC signal frequency ( $\omega$ ) was proposed. A relation of  $C - C_D \propto \omega^{-0.5}$  was found, where  $C_D$  is the depletion capacitance under the electrode. The relation is examined by the experimental and the TCAD simulation. The capacitance of a MIS device with oxide charges can be calculated according to the proposed model and is well-matched with the TCAD simulation under light to moderate doping concentration. For heavily doped substrates, the modeling deviates from the simulation results because of quantum confinement and concentration-dependent mobility. However, the trend of the capacitance value is still able to be estimated by our modeling. From the modeling, it was found that for  $Q_{ox}/q = 7.5 \times 10^{10} \text{ cm}^{-2}$ , the MIS capacitor with substrate doping concentration  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  exhibits a long lateral AC signal decay length of  $52 \mu\text{m}$  at 1 kHz under the inversion region. The findings of this work are fundamental and are helpful for device engineering.

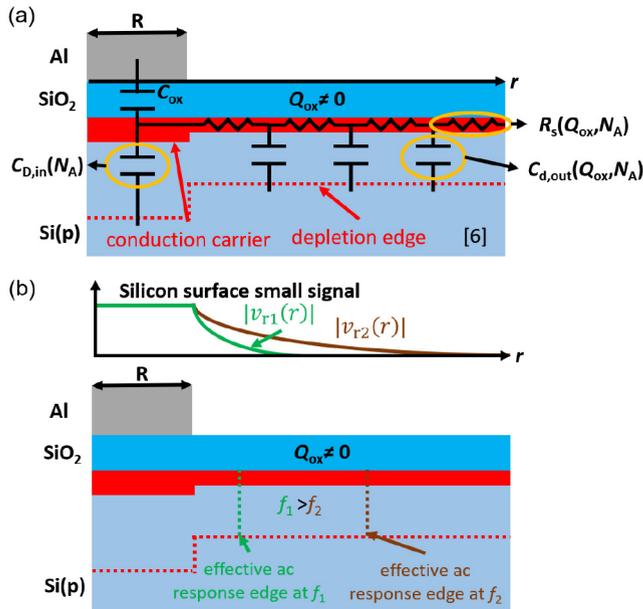
**INDEX TERMS** Capacitance, frequency dependency, lateral coupling, metal-insulator-semiconductor (MIS), oxide charges.

## I. INTRODUCTION

Electrical characterizations of metal-insulator-semiconductor (MIS) devices are essential in studying the dielectric property. When studying MIS capacitors, capacitance ( $C$ ) and conductance ( $G$ ) measurements at different frequencies ( $\omega$ ) are generally considered. Many pioneers had widely studied the methods of analyzing MIS devices, such as extracting interface traps by conductance's peak, estimating the number of oxide charges by flat band voltage shift, and finding carrier lifetime by transfer frequency of capacitance. The studies are fully described in [1] and [2] systematically.

When measuring the MIS capacitor, the existence of oxide charges is an important issue because the oxide charges will affect the flat band voltage and perturb the measured

$C$  and  $G$  [1]. Hofstein et al. first reported the impact of the oxide charges when measuring capacitance on the MIS capacitor with silicon as substrate and silicon dioxide as an insulating layer in 1964 [3]. In [3], a significant difference between the minority response speed of MIS capacitor with n-type substrate doping (MIS(n)) and p-type (MIS(p)) had been observed. The thermal generation mechanism is proposed for MIS(n)'s slow response speed [4]. In 1965, Hofstein et al. and Nicollian et al. suggested that oxide charge is responsible for MIS(p)'s fast minority response speed [5], [6]. Because the main oxide charges in silicon dioxide are generally positive, the oxide charges will induce an electron channel in MIS(p), as shown in Fig. 1. The electron channel will laterally connect electrons and increase



**FIGURE 1.** (a) The equivalent circuit for lateral AC response. The oxide charge induced electron channel will laterally connect with the minority carriers and increase the response signal of the minority. The measured impedance will be disturbed. (b) The effective AC response edge for two different frequencies. A higher frequency will have a smaller effective lateral AC response region because the equivalent circuit outside the electrode forms a low pass filter.

the response speed of the minority carriers in MIS(p). The dependencies of capacitance on frequency are therefore perturbed. The equivalent circuit in Fig. 1(a) was first proposed in [6]. Though [5] and [6] had proposed the mechanism, the comparison between theoretical and experimental was not completely studied, and the relations between oxide charges, doping concentration, capacitance, conductance, and frequency are still lack of discussion. In 1968, Pierret fabricated a metal-oxide-semiconductor transistor with the drain connected to the ground to study the impact of lateral AC current flow [7]. The case in [7] has a well-defined boundary condition and shows sufficient electrons supplied from the drain. The calculated result in [7] is well-matched with the experimental and indicates the impact of the lateral supplement on the minority. However, the phenomenon discussed in [7] is different from those discussed in [5] and [6]. The discussion on the effect of oxide charge was few since 1970s, and many researchers have worked on the annealing process to improve the oxide quality [8], [9], [10], [11]. When the oxide charges were reduced to  $Q_{ox}/q = 10^{11} \text{ cm}^{-2}$  or even less, the effect of the minority's lateral supplement is less pronounced.

Though the influence of the lateral supplement on minorities seems to decrease because of the reduction of oxide charges, it still attracts some researchers. For example, some works had observed very different minority frequency responses on MIS(n) and MIS(p) when studying MIS structure [12], [13], [14]. Two different generation carrier lifetimes were observed on MIS(n) and MIS(p) [12].

However, only the longer one matches with the finding of [15]. The phenomenon of lateral supply minority still lacks detailed discussion in the above works. Except for the minority response speed, other observations also imply the importance of the oxide charges. Yang et al. discovered that the coupling between two nearby MIS(p) is severely weakened when the oxide beyond the electrode is removed [16]. Furthermore, it is pointed out that the conductance of the MIS structure follows the relation of  $G \propto \omega^s$  when oxide charges and lateral-coupled minority carriers are non-negligible [17].

Except for the traditional MIS devices, we predict that the effect of lateral coupling will affect the performance of the junctionless field effect transistor (JLFET). JFET is a novel structure proposed in 2010 [18]. The characteristic of JLFET is that the source and drain have the same doping as the channel. Thus, no junction exists between the source/drain and channel. The device is predicted to become a potential candidate for transistors with aggressively scaled channel lengths [19], [20], [21] and 3D vertical transistors [22]. The JLFET is actually a MIS structure on a uniformly doped semiconductor. If any oxide charge or surface charge exists outside the gate electrode of JLFET, the gate control signal has the opportunity to laterally extend into the source/drain by the oxide-charge-induced carriers. The laterally extended control region will affect the gate capacitance and, thus, the performance of JLFET.

From existing literature, it is believed that the influence caused by oxide charges still makes its impact on MIS devices [12], [13], [14], [16], [17]. We also predict that the effect will affect the performance of JLFET, because JLFET is basically a MIS on a uniformly doped substrate. In this work, we discuss the effect of oxide charges in more detail by modeling, experimental observation, and TCAD simulation. We theoretically find the relation between capacitance and frequency when considering the oxide-charge-induced minority carriers. The relation is  $C - C_D \propto \omega^{-0.5}$ , where  $C_D$  is the depletion capacitance under the electrode. This relation is also observed in the experimental and the TCAD simulation. Based on the modeling, we can directly calculate the capacitance values of a MIS device when the number of oxide charges, doping concentration, and measuring frequency are decided. Our modeling is also well-matched with TCAD simulation under light to moderate substrate dopings and is still able to predict the trend under heavily doped substrates. It is believed that the modeling is useful for fundamental studies on MIS devices.

## II. EXPERIMENTAL AND SIMULATION

To study the phenomenon, we chose silicon as the substrate. As mentioned in [3], [5], [6], oxide charges in silicon dioxide are usually positive. Positive oxide charges will induce electrons in the p-type substrate. Thus, boron-doped p-type silicon wafers with a doping concentration of  $10^{16} \text{ cm}^{-3}$  and surface orientation (100) are adopted. The wafers are first cleaned by the Radio Corporation of America (RCA) clean

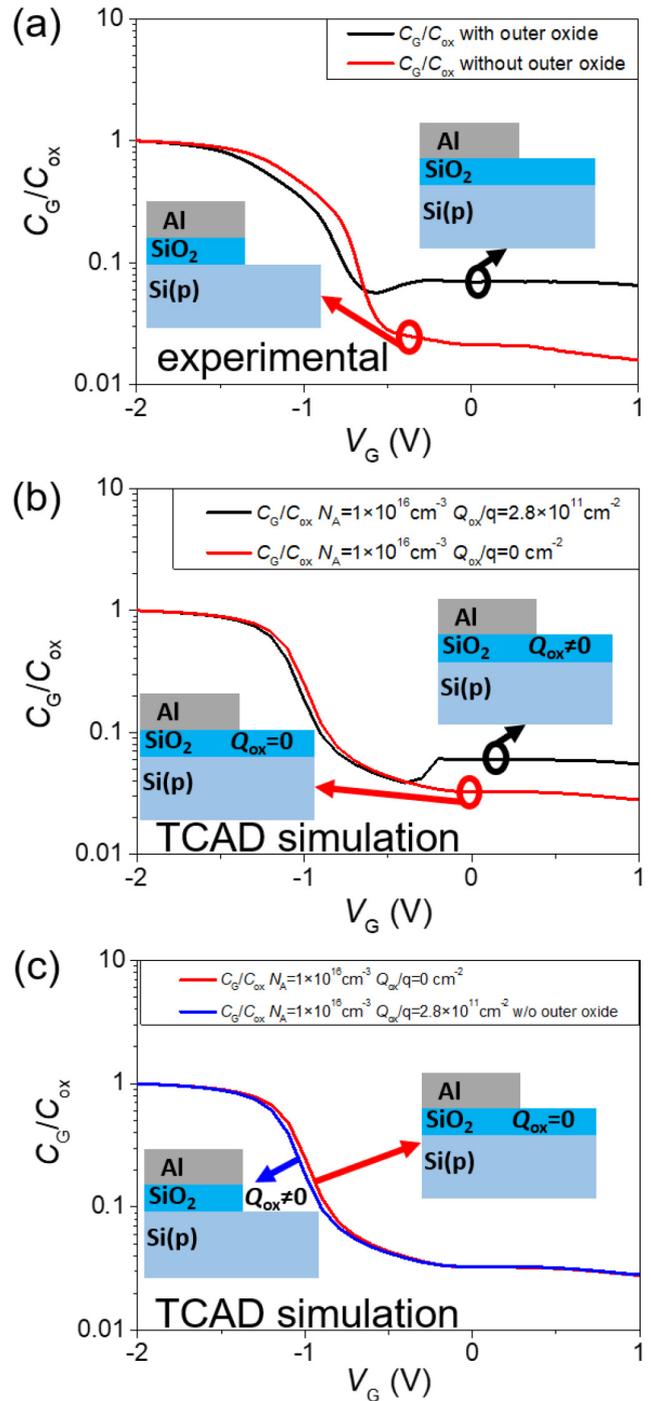
process [23]. The oxide with a thickness of 3 nm is grown by anodic oxidation (ANO). After the growth of the oxide, a rapid thermal annealing (RTA) process of 15 s in 20 torr 950 °C N<sub>2</sub> ambient is conducted to improve oxide quality. A 200 nm thick aluminum layer is then formed by thermal evaporation as the top electrode. A circle pattern with a diameter of 200 μm is defined by photolithography and wet etching. After defining the electrode pattern, the oxide layer outside the electrodes for one of the wafers is removed by diluted HF. The device with outer oxide removed was served as the control group. Finally, buffer oxide etchant (BOE) is adopted to remove the native back oxide, and a 200 nm thick aluminum layer is deposited as back contact. The capacitance of the devices are measured by Agilent B1500A.

To confirm our proposed modeling of capacitance under different situations, TCAD simulations were carried out. We use Silvaco ATLAS for simulation. In the simulations, the simulation models of direct tunneling, quantum confinement, band-to-band tunneling, concentration-dependent mobility, velocity saturation, Shockley-Read-Hall recombination, and band-gap narrowing are considered to have the results closer to reality. Devices with a radius of 100 μm and an oxide thickness of 3 nm is first considered to simulate the effects of  $N_A$  and  $Q_{ox}/q$ . By the way, devices with different radii from 100 μm to 100 nm and different oxide thicknesses from 3 nm to 200 nm are examined by TCAD simulation at  $N_A = 10^{15} \text{ cm}^{-3}$  and  $Q_{ox}/q = 10^{11} \text{ cm}^{-2}$ .

### III. RESULT AND DISCUSSION

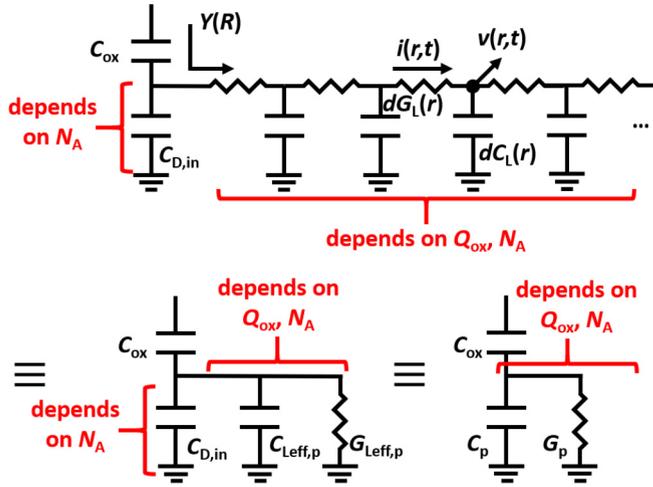
#### A. MEASUREMENT AND SIMULATION RESULTS

We named the electrode as “gate” and bias voltage as  $V_G$ . The capacitance is named as  $C_G$ . Fig. 2 is the normalized capacitance  $C_G/C_{ox}$  of MIS from experimental and simulation at 1 kHz, where  $C_{ox}$  is the oxide capacitance. We use the capacitance values extracted at  $V_G = -2\text{V}$  as  $C_{ox}$  for both the experimental and simulation. In Fig. 2(a), a measurement result of a MIS device without outer oxide is shown to imitate the device without oxide charges. Fig. 2 is plotted in log scale to highlight the separation in the inversion region. For devices without outer oxide charges (red curves in Figs. 2(a) and (b)), 1 kHz is still too high for the minority carriers in silicon to follow. The thermal generation is too slow to follow the variation of the inversion layer [5]. Thus, only the majority carriers at depletion region edge give response to the AC signal and the MIS device exhibits the phenomenon of classical high-frequency capacitance [1]. However, when outer oxide charges exist, which induce minority carriers and lateral supply of the inversion layer,  $C_G/C_{ox}$  rises in the inversion region at 1 kHz because of the stronger minority carriers’ response signal. We further show the simulated result of the MIS device with oxide charge but without outer oxide, which is the same as the experimental device without outer oxide, as shown in Fig. 2(c). From Fig. 2(c), one



**FIGURE 2.** (a) Normalized capacitance  $C_G/C_{ox}$  of MIS with and without outer oxide measured at 1 kHz. (b) Normalized capacitance  $C_G/C_{ox}$  of MIS with and without oxide charge at 1 kHz by simulation. (c) Normalized capacitance  $C_G/C_{ox}$  of MIS simulated at 1 kHz in the situation of 1) with outer oxide but without oxide charges and 2) with oxide charges but without outer oxide. The device with outer oxide in experimental and the device with oxide charges at outer oxide in TCAD simulation both rise in inversion region at 1 kHz because of the AC response of the lateral region.

can observe that the device without outer oxide can suitably imitate the device without oxide charge in the inversion region.



**FIGURE 3.** Equivalent circuit for lateral extending. Capacitance just under the electrode  $C_{D,in}$  only depends on the doping concentration  $N_A$ . The equivalent circuit beyond the electrode depends on  $N_A$  and  $Q_{ox}$ . AC response of series-connected conductance  $dG_L(r)$  and parallel-connected  $dC_L(r)$  can be simplified to equivalent  $G_{Leff,p}$  and  $C_{Leff,p}$ . The equivalent circuit can be further reduced to a parallel-connected  $G_p$  and  $C_p$  by combining  $C_{Leff,p}$  and  $C_{D,in}$ .

## B. EFFECT OF LATERAL COUPLING

The equivalent circuit in Fig. 1(a) helps one to understand the impact of oxide charges. The positive oxide charges outside the electrode will deplete majority hole carriers in p-type silicon to form a depletion capacitance  $C_{d,out}(N_A, Q_{ox})$  and attract minority electron carriers to form a lateral conduction channel with a sheet resistance of  $R_s(N_A, Q_{ox})$ . Both of  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$  are dependent on doping concentration  $N_A$  and oxide charges  $Q_{ox}$ .  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$  will laterally form serially connected low-pass filters, as shown in Fig 1(a). The applied AC signal on the electrode will laterally extend through these low-pass filters. This laterally extended area will contribute to the measured  $C_G$  and raise  $C_G$ , as shown in Fig. 2. The measured conductance  $G_G$  will also be affected by the above mechanism. Fig. 1(b) is plotted to show the schematic of lateral contribution. As shown in Fig. 1(b), the AC signal can fully apply to the region under the electrode but start to decay from the edge of the device. An AC response edge at the place where the amplitude of the AC signal decays to a relatively small value, i.e.,  $e^{-1}$ , was defined. The region between the device edge and the AC response edge will effectively contribute an extra value to  $C_G$ . In Fig. 1(b), the effective lateral region decreases when operating under a higher frequency because of the low pass filters formed by  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$ . Thus, one can obtain a lower  $C_G$  under a higher measuring frequency.

## C. MODELING OF LATERAL COUPLING

To quantitatively calculate the capacitance contributed by lateral area, one needs to know the distribution of AC voltage and current signal outside the electrode. The AC voltage and current signal are labeled in the upper part of Fig. 3 as  $v(r, t)$

and  $i(r, t)$ . With the derivation in the Appendix,  $v(r, t)$  and  $i(r, t)$  can be expressed as

$$v(r, t) = C_1 K_0 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha(N_A, Q_{ox})} \right) e^{j\omega t}, \quad r \geq R, \quad (1)$$

and

$$i(r, t) = C_1 2\pi r \sqrt{\frac{\omega C_{d,out}(N_A, Q_{ox})}{R_s(N_A, Q_{ox})}} K_1 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha(N_A, Q_{ox})} \right) e^{j\omega t}, \quad r \geq R, \quad (2)$$

where  $t$  is the time,  $r$  is the radius of cylindrical coordinates with origin at the center of the electrode as plotted in Fig. 1,  $R$  is the radius of the electrode,  $C_1$  is a constant,  $\omega$  is the angular frequency,  $\alpha(N_A, Q_{ox})$  is the product of  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$ ,  $K_0$  and  $K_1$  are modified Bessel function of the second kind with orders 0 and 1, respectively. Be mentioned that eqs. (1) and (2) are the distribution of AC signal outside the electrode where  $r \geq R$ . With the known  $v(r, t)$  and  $i(r, t)$ , we can further calculate the capacitance and conductance contributed by the lateral area by the equivalent circuits in Fig. 3. In Fig. 3,  $C_{ox}$  is oxide capacitance, and  $C_{D,in}$  is the depletion capacitance under the electrode. The series connection of  $C_{ox}$  and  $C_{D,in}$  is the classical model of high-frequency capacitance. It is noticed that for silicon, conductance contributed by generation is relatively low and is not considered here [5]. However, when considering lateral supplement of minority carriers, one needs to include a set of series connected  $dG_L(r)$  and a set of parallel connected  $dC_L(r)$  as shown in the upper part of Fig. 3. These  $dG_L(r)$  and  $dC_L(r)$  can be simplified as an equivalent circuit of parallel connected effective capacitance  $C_{Leff,p}$  and effective conductance  $G_{Leff,p}$ .  $C_{D,in}$  and  $C_{Leff,p}$  can be added together as  $C_p$ .  $G_{Leff,p}$  is equivalent to  $G_p$ . The relations between these equivalent circuits are shown in Fig. 3.  $C_{Leff,p}$  and  $G_{Leff,p}$ , which stem from the area outside the electrode, contribute to the admittance  $Y(R)$  seen at the electrode's edge, where  $r = R$ .  $Y(R)$ , also plotted in upper part of Fig. 3 can be expressed as

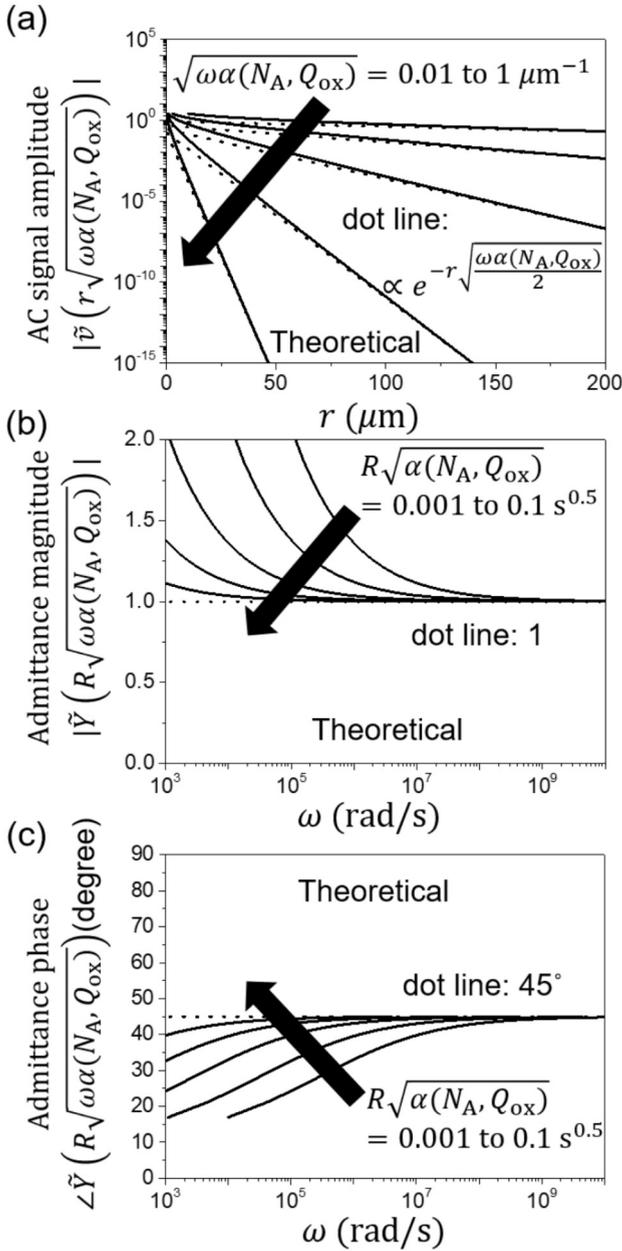
$$Y(R) = \frac{i(R, t)}{v(R, t)} = 2\pi R \sqrt{\frac{\omega C_{d,out}(N_A, Q_{ox})}{R_s(N_A, Q_{ox})}} \frac{K_1 \left( j^{\frac{1}{2}} R \sqrt{\omega \alpha(N_A, Q_{ox})} \right)}{K_0 \left( j^{\frac{1}{2}} R \sqrt{\omega \alpha(N_A, Q_{ox})} \right)} j^{\frac{1}{2}}, \quad (3)$$

where  $R$  is the radius of the electrode. The relation between  $Y(R)$ ,  $C_{Leff,p}$ , and  $G_{Leff,p}$  is

$$Y(R) = G_{Leff,p} + j\omega C_{Leff,p}. \quad (4)$$

One can eliminate the constant part of eq. (1) and (3) to get a dimensionless AC voltage distribution  $\tilde{v}(r\sqrt{\omega \alpha(N_A, Q_{ox})})$  as

$$\tilde{v}(r\sqrt{\omega \alpha(N_A, Q_{ox})}) = K_0 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha(N_A, Q_{ox})} \right) e^{j\omega t}, \quad (5)$$



**FIGURE 4.** (a) The amplitude of the dimensionless surface AC signal voltage  $\tilde{v}(r\sqrt{\omega\alpha(N_A, Q_{ox})})$  vs.  $r$ . (b) The magnitude and (c) the phase of the dimensionless admittance  $\tilde{Y}(R\sqrt{\omega\alpha(N_A, Q_{ox})})$  vs.  $\omega$ . Here,  $\alpha = C_{d,out}R_s$  is dependent on  $N_A$  and  $Q_{ox}$ .

and a dimensionless admittance  $\tilde{Y}(R\sqrt{\omega\alpha(N_A, Q_{ox})})$  as

$$\tilde{Y}(R\sqrt{\omega\alpha(N_A, Q_{ox})}) = \frac{K_1(j^{\frac{1}{2}}R\sqrt{\omega\alpha(N_A, Q_{ox})})}{K_0(j^{\frac{1}{2}}R\sqrt{\omega\alpha(N_A, Q_{ox})})}j^{\frac{1}{2}}. \quad (6)$$

The value of  $|\tilde{v}(r\sqrt{\omega\alpha(N_A, Q_{ox})})|$  vs.  $r$  is plotted in Fig. 4(a). In Fig. 4(a), one can observe that the amplitude of the voltage's AC signal roughly decays exponentially with  $r$  when the device parameter and frequency are decided. The voltage's AC signal will decay faster when measuring

under a higher frequency or  $\alpha(N_A, Q_{ox})$  value. The magnitude and phase of  $Y(R\sqrt{\omega\alpha(N_A, Q_{ox})})$  vs.  $\omega$  are calculated and are shown in Fig. 4(b) and (c). The results in Fig. 4 demonstrate the lateral region's AC signal distribution and effective admittance.

Although the above modeling can describe the effect of lateral AC response,  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$  need to be derived from  $N_A$  and  $Q_{ox}$ . Fortunately,  $R_s(N_A, Q_{ox})$  and  $C_{d,out}(N_A, Q_{ox})$  are coupled values with the well-discussed theories in [1]. The depletion capacitance is known as

$$C_{d,out} = \sqrt{\frac{qN_A\epsilon_s}{2\psi_{s,out}}} \quad (7)$$

and sheet resistance as

$$R_s = \frac{1}{\mu_n|Q_i|} = \frac{1}{\mu_n\sqrt{2qN_A\epsilon_s\psi_{s,out}}} \left[ \sqrt{1 + \frac{kT}{q\psi_{s,out}} \frac{n_i^2}{N_A^2} e^{\frac{q\psi_{s,out}}{kT}}} - 1 \right]^{-1}, \quad (8)$$

where  $q$  is elementary charge,  $N_A$  is the doping concentration,  $\epsilon_s$  is the dielectric constant of silicon,  $\psi_{s,out}$  is the surface band bending outside the electrode,  $\mu_n$  is the electron mobility,  $k$  is Boltzmann constant,  $T$  is the temperature, and  $n_i$  is the intrinsic carrier concentration of silicon. It is noticed that the surface band bending is induced by oxide charges but not electrode voltage. Also, we adopt  $\mu_n = 1000 \text{ cm}^2/\text{V}\cdot\text{s}$  in this work. A more accurate  $\mu_n$  may be achievable by considering doping concentration and electric field [24]. Because the part beyond the electrode is an oxide-semiconductor system, as shown in Fig. 5(a), the oxide charges  $Q_{ox}$  will balance with the induced charges  $Q_s$  in the semiconductor. Thus, one can write down

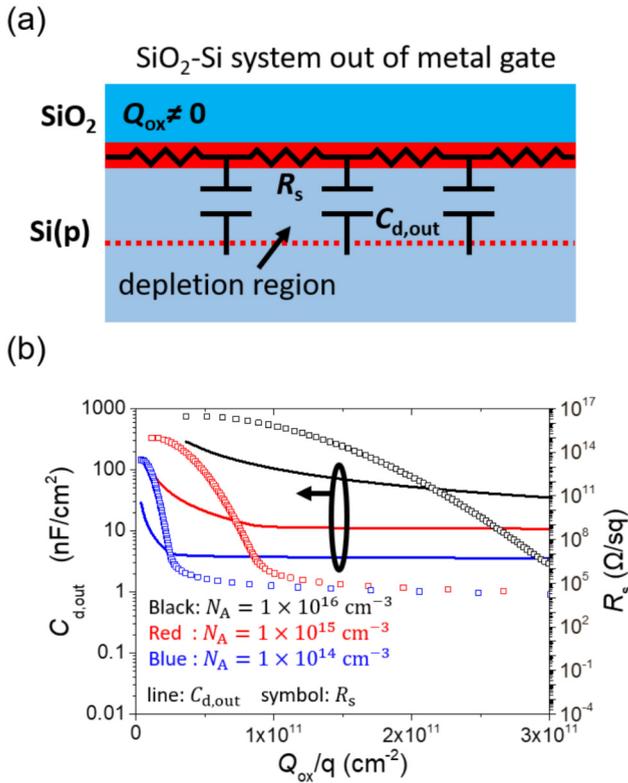
$$Q_{ox} = -Q_s = \sqrt{2qN_A\epsilon_s\psi_{s,out} \left( 1 + \frac{kT}{q\psi_{s,out}} \frac{n_i^2}{N_A^2} e^{\frac{q\psi_{s,out}}{kT}} \right)}. \quad (9)$$

From eq. (9), it is found that  $Q_{ox}$  and  $N_A$  can determine  $\psi_{s,out}$ .  $C_{d,out}$  and  $R_s$  can be found by inserting  $\psi_{s,out}$  into eqs. (7) and (8). Fig. 5(b) is a plot of  $C_{d,out}$ ,  $R_s$  vs.  $Q_{ox}/q$  with different doping concentrations  $N_A$ .

#### D. ROLE OF FREQUENCY ON LATERAL COUPLING

From Fig. 4(b) and (c), it is observed that  $|\tilde{Y}|$  approaches 1 and  $\angle\tilde{Y}$  approaches  $45^\circ$  when  $R\sqrt{\omega\alpha(N_A, Q_{ox})}$  is large enough. For a specific device with fixed  $R$  and  $\alpha(N_A, Q_{ox})$ , if  $\omega$  is large enough, the approximation of  $|\tilde{Y}| \approx 1$  and  $\angle\tilde{Y} \approx 45^\circ$  can be obtained. Under the situation,  $G_{Leff,p}$  and  $C_{Leff,p}$  can be derived from eqs. (3) and (4) as

$$G_{Leff,p} = \pi R \sqrt{\frac{2\omega C_{d,out}(N_A, Q_{ox})}{R_s(N_A, Q_{ox})}}, \quad (10)$$



**FIGURE 5.** (a) Structure of oxide-semiconductor system. (b) Calculated depletion capacitance per unit area  $C_{d,out}$  and sheet resistance  $R_s$  for various effective oxide charge  $Q_{ox}$  and doping concentration  $N_A$ .

and

$$C_{Leff,p} = \pi R \sqrt{\frac{2C_{d,out}(N_A, Q_{ox})}{\omega R_s(N_A, Q_{ox})}}. \quad (11)$$

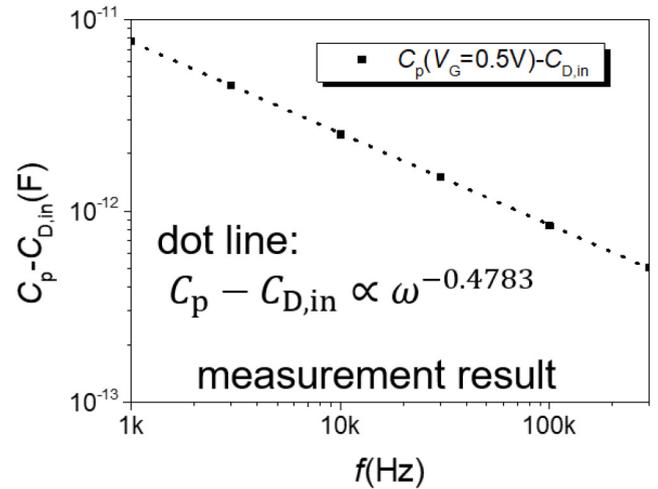
With eq. (11) and the equivalent circuits in Fig. 3, one can observe the relation of

$$C_p - C_{D,in} = C_{Leff,p} \propto \omega^{-0.5}. \quad (12)$$

The tendency of the capacitance contributed by lateral area can be represented by eq. (12). The decreasing of capacitance under higher frequency also reflects the nature of the low-pass filter form by  $dG_L(r)$  and  $dC_L(r)$  in Fig. 3. The log-log plot of  $C_p - C_{D,in}$  vs. frequency from the experiment is shown in Fig. 6. A fitting curve of  $C_p - C_{D,in} \propto \omega^{-0.4783}$  is shown. The result is close to the theory in eq. (12).

### E. EXTRACTION OF AC SIGNAL DECAY LENGTH

The AC signal decay length with the well-defined  $C_{d,out}(N_A, Q_{ox})$  and  $R_s(N_A, Q_{ox})$  is of interest. When a device with radius  $R$  is measured by an AC signal, we consider the AC voltage distribution in Fig. 4(a) at the part of  $r \geq R$ . It is noticed that the silicon surface's AC voltage outside the electrode will decay exponentially with  $r$  if the value of  $r\sqrt{\omega\alpha(N_A, Q_{ox})}$  is large enough. The AC signal



**FIGURE 6.** Extracted  $C_p - C_{D,in}$  vs. frequency from the measurement. The data are well fitted with  $C_p - C_{D,in} \propto \omega^{-0.4783}$ .

decay length  $l_{ac}$  is

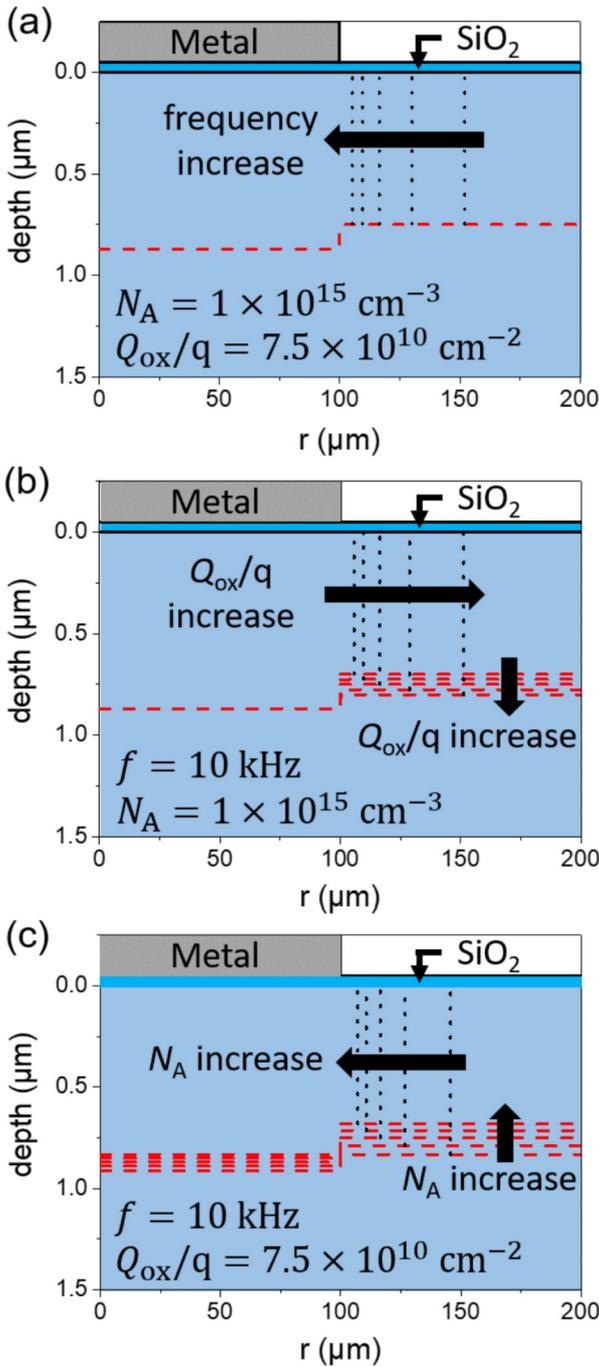
$$l_{ac} = \sqrt{\frac{2}{\omega\alpha(N_A, Q_{ox})}}. \quad (13)$$

The AC signal decay length, which indicates the lateral control distance starting from the edge of the devices, will vary with frequency,  $Q_{ox}$ , and  $N_A$ . In Fig. 7, a circle device with a radius of 100  $\mu\text{m}$  was modeled. The red dash lines are the edges of the depletion region, and the black dot lines are the effective AC signal response boundaries, where the amplitude of the AC signal decays to  $e^{-1}$  of AC signal at device's edge. The lateral AC response regions with various frequencies,  $Q_{ox}$ , and  $N_A$  are plotted in Fig. 7(a), (b), and (c), respectively. For the situation as considered in Fig. 7(a) with  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and  $Q_{ox}/q = 7.5 \times 10^{10} \text{ cm}^{-2}$ , the AC signal decay length starting from device's edge will vary from 52 to 5  $\mu\text{m}$  when the AC signal increases from 1 to 100 kHz. The calculated decay length is comparable to the device dimension.

### F. COMPARISON BETWEEN MODELED AND TCAD-SIMULATED RESULTS

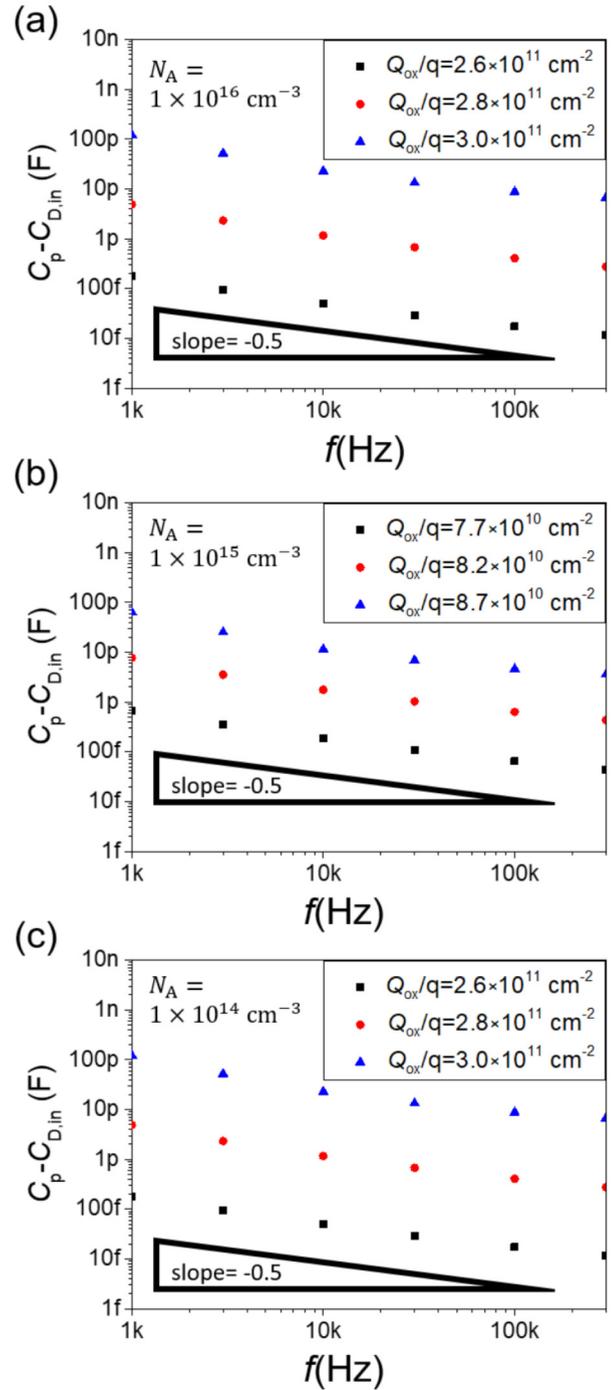
To confirm the universality of our modeling, TCAD simulations under three different doping concentrations of  $N_A = 1 \times 10^{16}$ ,  $1 \times 10^{15}$ , and  $1 \times 10^{14} \text{ cm}^{-3}$  were first explored. The simulated  $C_p - C_{D,in}$  at frequency 1 to 300 kHz is plotted in Fig. 8. For each doping concentration, three different  $Q_{ox}/q$  are selected for simulation. A tendency of  $C_p - C_{D,in} \propto \omega^{-0.5}$  was found in Fig. 8.

Subsequently, the capacitance values of a MIS devices starting from  $R$ ,  $N_A$ ,  $Q_{ox}$ , and frequency are studied. Eqs. (7) to (9) were used to calculate  $R_s(N_A, Q_{ox})$  and  $C_{d,out}(N_A, Q_{ox})$  as before. The capacitance values can be calculated by inserting  $R$ ,  $R_s(N_A, Q_{ox})$ ,  $C_{d,out}(N_A, Q_{ox})$ , and frequency into the proposed analytical model. Solid lines in Fig. 9 show the modeling results of  $C_G$  v.s.  $Q_{ox}/q$  for five



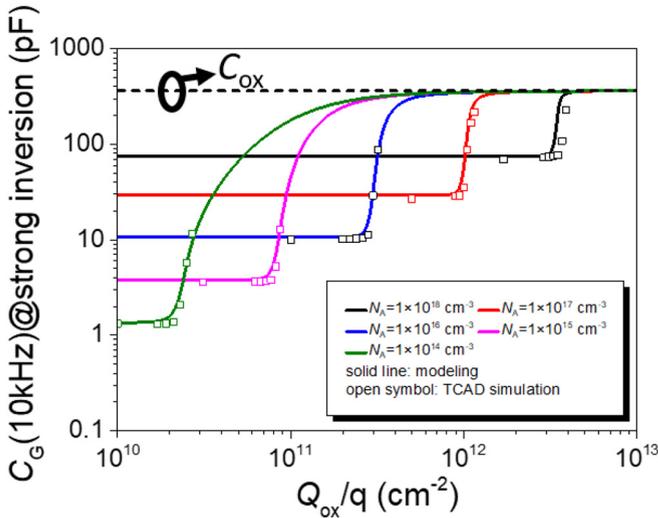
**FIGURE 7.** Modeling of effective AC response edges. The red dash lines are the edges of the depletion region, and the black dot lines are the effective AC signal response boundaries. The boundary is defined as the place where the amplitude of the AC signal was decayed to  $e^{-1}$  from device's edge. Dependencies of AC response edges on (a) frequency from 1 to 100 kHz with fixed  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and  $Q_{ox}/q = 7.5 \times 10^{10} \text{ cm}^{-2}$ , (b)  $Q_{ox}/q$  from  $7 \times 10^{10}$  to  $8 \times 10^{10} \text{ cm}^{-2}$  with fixed frequency 10 kHz and  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and (c)  $N_A$  from  $9 \times 10^{14}$  to  $1.1 \times 10^{15} \text{ cm}^{-3}$  with fixed frequency 10 kHz and  $Q_{ox}/q = 7.5 \times 10^{10} \text{ cm}^{-2}$ .

different doping concentrations at 10 kHz. The TCAD simulation results are also attached as open symbols. In Fig. 9, one can observe that the proposed modeling can calculate

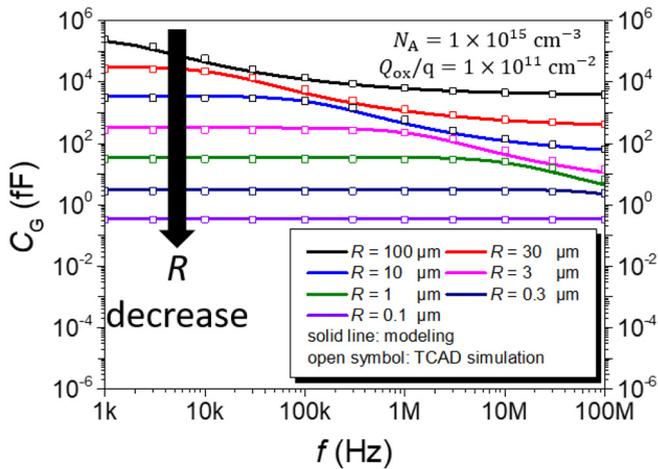


**FIGURE 8.** TCAD simulated  $C_p - C_{D,in}$  at frequency from 1 to 300 kHz for substrate doping concentrations of  $N_A =$  (a)  $1 \times 10^{16}$ , (b)  $1 \times 10^{15}$  and (c)  $1 \times 10^{14} \text{ cm}^{-3}$ .

almost the same results with TCAD simulation under moderate doping concentration. However, the modeling calculates capacitance values higher than the simulation under heavy doping concentration. The deviation stems from the strong surface field and high doping concentration. In the simulation, a strong surface field will make the effect of quantum confinement significant, and high doping concentration will



**FIGURE 9.** TCAD simulated (open symbol) and proposed modeling (solid line)  $C_G$  v.s.  $Q_{ox}/q$  at frequency 10 kHz under strong inversion for five different  $N_A$ 's.



**FIGURE 10.** TCAD simulated (open symbol) and proposed modeling (solid line)  $C_G$  v.s. frequency at  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and oxide charge  $Q_{ox}/q = 1 \times 10^{11} \text{ cm}^{-2}$  under strong inversion. Devices' radii from 100  $\mu\text{m}$  to 100 nm are considered.

lead to severe degradation of carrier mobility because of concentration-dependent mobility. Results in Fig. 9 indicate that our modeling can calculate the capacitance value at light to moderate doping concentrations and predict the trend under heavy doping concentration when considering the impact of the existing oxide charges.

In our modeling, the device dimension  $R$  is also considered. We compare the modeling and simulation under different  $R$  in Fig. 10. A moderate doping concentration of  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and oxide charge  $Q_{ox}/q = 1 \times 10^{11} \text{ cm}^{-2}$  is adopted. Fig. 10 shows that our modeling still works well under the sub-micron region. For the sub-micron devices, one can imagine  $C_p \gg C_{ox}$  because the lateral coupling region is much larger than the devices' area. The serially

connected  $C_p$  and  $C_{ox}$  becomes close to  $C_{ox}$  even at high frequency.

**G. EFFECT OF OXIDE THICKNESS**

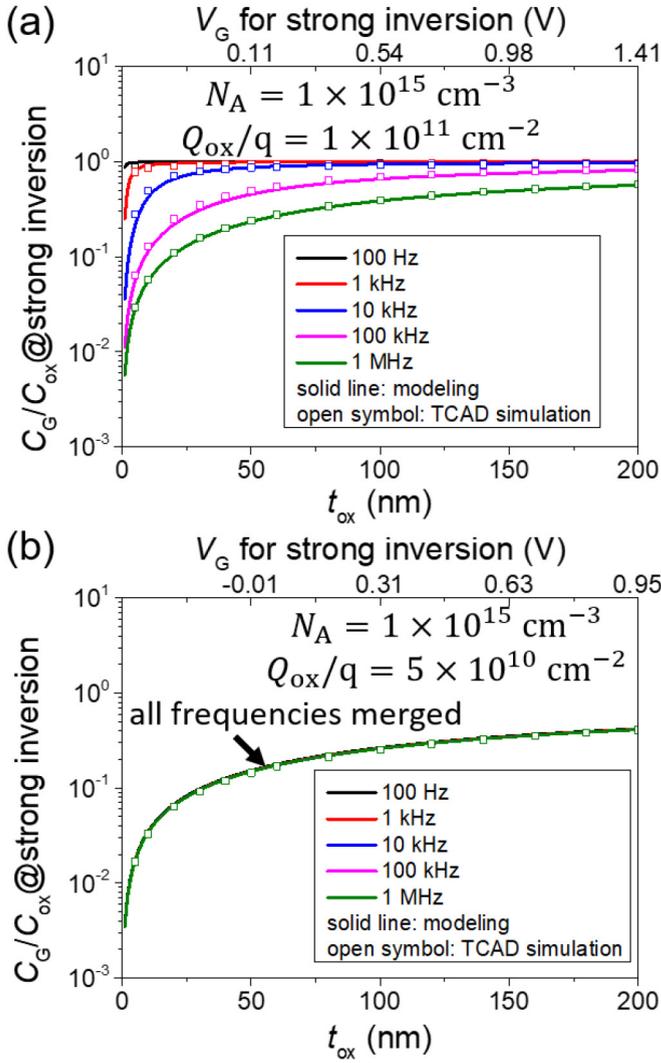
When discussing the effect of oxide charges, former works study oxide thickness over 100 nm [5], [6]. However, oxide thicknesses for recent works drop to a few nanometers. The capacitance frequency dispersion caused by the oxide charges for MIS with different oxide thicknesses is therefore of interest.  $C_G/C_{ox}$  v.s.  $t_{ox}$  under different frequencies and  $Q_{ox}$  according to the proposed model are discussed. Devices with different oxide thicknesses under the same lateral coupling area,  $C_{Leff,p}$ ,  $G_{Leff,p}$ ,  $C_p$ , and  $G_p$  at specific  $Q_{ox}$ ,  $N_A$ , and frequency are considered. However, the final measured  $C_G$  will include the series-connected  $C_{ox}$  as shown on the last equivalent circuit of Fig. 3. The total normalized capacitance  $C_G/C_{ox}$  can be expressed as

$$\frac{C_G}{C_{ox}} = \frac{G_p^2 + \omega^2 C_p (C_p + C_{ox})}{G_p^2 + \omega^2 (C_p + C_{ox})^2} \tag{14}$$

Fig. 11 shows the calculated  $C_G/C_{ox}$  v.s.  $t_{ox}$  for five frequencies at  $Q_{ox}/q = 1 \times 10^{11}$  and  $5 \times 10^{10} \text{ cm}^{-2}$  under strong inversion. The TCAD simulation results are also shown for comparison. The situation of considerable oxide charges causing strong inversion at the silicon surface is first shown in Fig. 11(a). The AC signal lateral extends to a large region at low frequency, i.e., 100 or 1k Hz, and leads to a significant  $C_p$ . The numerator and denominator for eq. (14) are close to  $G_p^2 + \omega^2 C_p^2$  when  $C_p \gg C_{ox}$ . In this situation,  $C_G/C_{ox}$  is close to 1. However, the lateral extended region and  $C_p$  decrease when the frequency increases. For MIS with thick oxide layer,  $C_p$  is still higher than  $C_{ox}$ , and  $C_G/C_{ox}$  keeps close to 1. On the contrary,  $C_{ox}$  of MIS with thin oxide layer is larger than  $C_p$  at high frequency and causes a severe decreasing in  $C_G/C_{ox}$ . From Fig. 11(a), we can observe that  $C_G/C_{ox}$  of MIS with oxide thickness in a few nanometers decreases for about two orders when the frequency increases. In Fig. 11(b) with fewer oxide charges, the AC signal is hard to extend laterally because of fewer induced minority carriers. In this situation, the impact of oxide charges is little, and  $C_G/C_{ox}$  is close to  $C_{D,in}/(C_{D,in} + C_{ox})$ , which is in consistent with the theory of classical high-frequency capacitance [1]. In summary, there is a significant frequency dispersion for MIS with thin oxide layer when the number of oxide charges is non-negligible.

**IV. CONCLUSION**

The phenomenon of oxide charge effect in MIS devices is studied quantitatively by means of modeling, experimental device characterization, and TCAD simulation. The oxide-charge-induced minority carriers outside the electrode will respond to the AC signal and disturb the measured impedance. The capacitance and conductance contributed by



**FIGURE 11.** Theoretical and simulated  $C_G/C_{ox}$  under strong inversion vs.  $t_{ox}$  for substrate doping concentration  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  with oxide charges of (a)  $Q_{ox}/q = 1 \times 10^{11} \text{ cm}^{-2}$  and (b)  $Q_{ox}/q = 5 \times 10^{10} \text{ cm}^{-2}$  at different frequencies. The  $V_G$  for strong inversion of each  $t_{ox}$  is also shown.

the lateral extending area were analytically studied. When the influence of oxide charges is taken into account, a relation of  $C - C_D \propto \omega^{-0.5}$  is proposed. This relation is also observed in the experimental and the TCAD simulation. Lateral AC response distance and oxide charges are also extracted theoretically. From the modeling, the AC signal can laterally extend to  $52 \mu\text{m}$  at 1 kHz under the conditions of  $N_A = 1 \times 10^{15} \text{ cm}^{-3}$  and  $Q_{ox}/q = 7.5 \times 10^{10} \text{ cm}^{-2}$ . The distance is comparable to the device dimension and may perturb the measured capacitance to a considerable level. The capacitance value can be directly calculated from the physical conditions of the devices according to the proposed model. The calculated results agree with the TCAD simulation. It is also shown that frequency dispersion for MIS with a thin oxide layer is severe when the number of oxide charges is non-negligible.

## APPENDIX DERIVATION OF AC VOLTAGE AND CURRENT SIGNAL

The sheet resistance  $R_s(N_A, Q_{ox})$  and capacitance  $C_{d,out}(N_A, Q_{ox})$  in Fig. 1(a) can be transformed into  $dG_L(r)$  and  $dC_L(r)$  in the upper part of Fig. 3. Because  $R_s(N_A, Q_{ox})$  and  $C_{d,out}(N_A, Q_{ox})$  surround the electrode in cylindrical coordinates,  $dG_L(r)$  and  $dC_L(r)$  can be expressed as

$$dG_L(r) = \frac{2\pi r}{R_s(N_A, Q_{ox})} dr, \quad (15)$$

and

$$dC_L(r) = 2\pi r C_{d,out}(N_A, Q_{ox}) dr, \quad (16)$$

where  $r$  is the radius of cylindrical coordinates with origin at the center of the electrode as plotted in Fig. 1. One can write down the differential equations of current and voltage for AC signal, i.e.,  $i(r, t)$  and  $v(r, t)$  in Fig. 3, from  $dG_L(r)$  and  $dC_L(r)$  as

$$i(r, t) = -dG_L(r) dv(r, t) = -\frac{2\pi r}{R_s(N_A, Q_{ox})} \frac{\partial v(r, t)}{\partial r}, \quad (17)$$

and

$$\frac{\partial v(r, t)}{\partial t} = -\frac{di(r, t)}{dC_L(r)} = -\frac{1}{2\pi r C_{d,out}(N_A, Q_{ox})} \frac{\partial i(r, t)}{\partial r}, \quad (18)$$

where  $t$  is time. Under a specific measuring frequency, the solution to  $i(r, t)$  and  $v(r, t)$  can be performed by phasor form as

$$i(r, t) = i_r(r) e^{j\omega t}, \quad (19)$$

and

$$v(r, t) = v_r(r) e^{j\omega t}, \quad (20)$$

where  $\omega$  is the angular frequency.  $i_r(r)$  and  $v_r(r)$  are current and voltage amplitudes of AC signal depending on the radial distance. By inserting eqs. (19) and (20) into the coupled differential equation eqs. (17) and (18) one can get

$$r^2 v_r''(r) + r v_r'(r) - j\omega C_{d,out}(N_A, Q_{ox}) R_s(N_A, Q_{ox}) r^2 v_r(r) = 0. \quad (21)$$

One may define the product of  $C_{d,out}$  and  $R_s$  as  $\alpha$  by

$$\alpha(N_A, Q_{ox}) = C_{d,out}(N_A, Q_{ox}) R_s(N_A, Q_{ox}). \quad (22)$$

From eq. (21) one can solve that

$$v_r(r) = C_1 K_0 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha(N_A, Q_{ox})} \right). \quad (23)$$

By inserting eq. (23) back in to eq. (17), one can derive

$$i_r(r) = C_1 2\pi r \sqrt{\frac{\omega C_{d,out}(N_A, Q_{ox})}{R_s(N_A, Q_{ox})}} K_1 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha(N_A, Q_{ox})} \right) j^{\frac{1}{2}}, \quad (24)$$

where  $C_1$  is a constant,  $K_0$  and  $K_1$  are modified Bessel function of the second kind with orders 0 and 1, respectively.

With considering the phasor part  $e^{j\omega t}$ ,  $i(r, t)$  and  $v(r, t)$  can be expressed as

$$v(r) = C_1 K_0 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha (N_A, Q_{ox})} \right) e^{j\omega t}, \quad r \geq R, \quad (25)$$

and

$$i(r) = C_1 2\pi r \sqrt{\frac{\omega C_{d,out}(N_A, Q_{ox})}{R_s(N_A, Q_{ox})}} K_1 \left( j^{\frac{1}{2}} r \sqrt{\omega \alpha (N_A, Q_{ox})} \right) j^{\frac{1}{2}} e^{j\omega t}, \quad r \geq R, \quad (26)$$

where  $R$  is the radius of the device. Eqs. (25) and (26) describe the distribution of the AC signal outside the electrode. The AC signal inside the electrode is fully controlled by the electrode and serves as the boundary condition.

## REFERENCES

- [1] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. Hoboken, NJ, USA: Wiley, 1982.
- [2] E. H. Nicollian and A. Goetzberger, "The Si-SiO<sub>2</sub> interface—Electrical properties as determined by the metal-insulator-silicon conductance technique," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1055–1133, Jul./Aug. 1967.
- [3] S. R. Hofstein, K. H. Zaininger, and G. Warfield, "Frequency response of the surface inversion layer in silicon," *Proc. IEEE*, vol. 52, no. 8, pp. 971–972, Aug. 1964.
- [4] C.-T. Sah, R. N. Noyce, and W. Shockley, "Carrier generation and recombination in P-N junctions and P-N junction characteristics," *Proc. IRE*, vol. 45, no. 9, pp. 1228–1243, Sep. 1957.
- [5] S. R. Hofstein and G. Warfield, "Physical limitations on the frequency response of a semiconductor surface inversion layer," *Solid-State Electron.*, vol. 8, no. 3, pp. 321–341, 1965.
- [6] E. H. Nicollian and A. Goetzberger, "Lateral AC current flow model for metal-insulator-semiconductor capacitors," *IEEE Trans. Electron Devices*, vol. ED-12, no. 3, pp. 108–117, Mar. 1965.
- [7] R. F. Pierret, "Frequency variation of the MOS-transistor  $V_D = 0$  admittance," *Solid-State Electron.*, vol. 11, no. 2, pp. 253–260, 1968.
- [8] F. M. Fowkes and D. W. Hess, "Control of fixed charge at Si-SiO<sub>2</sub> interface by oxidation–reduction treatments," *Appl. Phys. Lett.*, vol. 22, no. 8, pp. 377–379, 1973.
- [9] H. P. Vyas, G. D. Kirchner, and S. J. Lee, "Fixed charge density ( $Q_{ss}$ ) at the Si-SiO<sub>2</sub> interface for thin oxides," *J. Electrochem. Soc.*, vol. 129, no. 8, pp. 1757–1760, 1982.
- [10] A. I. Akinwande and J. D. Plummer, "Quantitative modeling of Si/SiO<sub>2</sub> interface fixed charge: I. Experimental results," *J. Electrochem. Soc.*, vol. 134, no. 10, pp. 2565–2573, 1987.
- [11] T. Hori, H. Iwasaki, and K. Tsuji, "Electrical and physical properties of ultrathin reoxidized nitrided oxides prepared by rapid thermal processing," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 340–350, Feb. 1989.
- [12] S. Monaghan et al., "Capacitance and conductance for an MOS system in inversion, with oxide capacitance and minority carrier lifetime extractions," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4176–4185, Dec. 2014.
- [13] W. Huang, T. Khan, and T. P. Chow, "Comparison of MOS capacitors on n- and p-type GaN," *J. Electron. Mater.*, vol. 35, no. 4, pp. 726–732, 2006.
- [14] Q. Xie et al., "Germanium surface passivation and atomic layer deposition of high- $k$  dielectrics—Tutorial review on Ge-based MOS capacitors," *Semicond. Sci. Technol.*, vol. 27, no. 7, 2012, Art. no. 74012.
- [15] C. Chellic et al., "Minority carrier lifetime in MOCVD-grown C- and Zn-doped InGaAs," in *Proc. 11th Int. Conf. Indium Phosphide Related Mater. (IPRM)*, 1999, pp. 127–130.
- [16] M.-H. Yang and J.-G. Hwu, "Influence of neighboring coupling on metal-insulator-semiconductor (MIS) deep-depletion tunneling current via Schottky barrier height modulation mechanism," *J. Appl. Phys.*, vol. 121, no. 15, 2017, Art. no. 154504.
- [17] O. Özdemir, İ. Atilgan, and B. Katircioğlu, "Abnormal frequency dispersion of the admittance associated with a chromium/plasma deposited a-SiNx:H/p-Si structure," *J. Non-Cryst. Solids*, vol. 353, no. 29, pp. 2751–2757, 2007.
- [18] J.-P. Colinge et al., "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, pp. 225–229, Feb. 2010.
- [19] L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer, "Simulation of junctionless Si nanowire transistors with 3 nm gate length," *Appl. Phys. Lett.*, vol. 97, Aug. 2010, Art. no. 62105.
- [20] V. Thirunavukkarasu, Y.-R. Jhan, Y.-B. Liu, and Y.-C. Wu, "Performance of inversion, accumulation, and junctionless mode n-Type and p-Type bulk silicon FinFETs with 3-nm gate length," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 645–647, Jul. 2015.
- [21] V. Thirunavukkarasu et al., "Gate-all-around junctionless silicon transistors with atomically thin nanosheet channel (0.65 nm) and record sub-threshold slope (43 mV/dec)," *Appl. Phys. Lett.*, vol. 110, Jan. 2017, Art. no. 32101.
- [22] F. Mo et al., "Low-voltage operating ferroelectric FET with ultrathin IGZO channel for high-density memory application," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 717–723, 2020.
- [23] W. Kern, "The evolution of silicon wafer cleaning technology," *J. Electrochem. Soc.*, vol. 137, no. 6, pp. 1887–1892, 1990.
- [24] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.

**KUNG-CHU CHEN** was born in Chiayi, Taiwan, in 1997. He received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2019. He is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

**KUAN-WUN LIN** (Graduate Student Member, IEEE) was born in Changhua, Taiwan, in 1996. He received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2018, where he is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering.

**SUNG-WEI HUANG** was born in Taiwan in 1996. He received the B.S. degree in physics and electrical engineering from National Taiwan University, Taipei, Taiwan, in 2020, where he is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering.

**JIAN-YU LIN** was born in Taipei, Taiwan, in 1997. He received the B.S. degree in electrical engineering and the M.S. degree in electronics engineering from National Taiwan University, Taipei, in 2019 and 2021, respectively. He is currently pursuing the Ph.D. degree with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, USA.

**JENN-GWO HWU** (Senior Member, IEEE) received the B.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1977, and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1979 and 1985, respectively. He joined the Faculty with NTU in 1981, where he is currently a Distinguished Professor with the Department of Electrical Engineering and the Graduate Institute of Electronics Engineering. His research work is mainly on ultra-thin gate oxide and its related Si MOS devices.