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Pelgrom-Based Predictive Model to Estimate Metal Grain Granularity and Line Edge Roughness in Advanced Multigate MOSFETs

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ABSTRACT The impact of different variability sources on the transistor performance increases as devices are scaled-down, being the metal grain granularity (MGG) and the line edge roughness (LER) some of the major contributors to this increase. Variability studies require the simulation of large samples of different device configurations to have statistical significance, increasing the computational cost. A novel Pelgrom-based predictive (PBP) model that estimates the impact of MGG and LER through the study of the threshold voltage standard deviation (σV_{Th}), is proposed. This technique is computationally efficient since once the threshold voltage mismatch is calculated, σV_{Th} can be predicted for different gate lengths (L_g), cross-sections, and intrinsic variability parameters, without further simulations. The validity of the PBP model is demonstrated for three state-of-the-art architectures (FinFETs, nanowire FETs, and nanosheet FETs) with different L_g, cross-sections, and drain biases (V_D). The relative errors between the predicted and simulated data are lower than 10%, in the 92% of the cases.

INDEX TERMS FinFET, line edge roughness, metal grain granularity, nanosheet, nanowire, Pelgrom, prediction model, variability.

I. INTRODUCTION

Next generations of advanced transistors require an improvement in the gate control, together with the reduction of variability effects [1]. Some of the most relevant sources of variability are the line edge roughness (LER) [2], [3], [4], produced by lithographic processes; the metal grain granularity (MGG) [4], [5], [6], caused by the metal gate deposition; or the random dopant fluctuations (RDF) [7], that are due to the presence of dopants in the channel.

To accurately analyze the impact of different variability sources on these state-of-the-art architectures it is necessary: i) to use three-dimensional simulation approaches that incorporate the effects of quantum-mechanical confinement, and ii) to simulate large ensembles of different device configurations to obtain statistical significance. These two factors notably increase the computational cost of these variability studies. Therefore, complementary techniques to predict variability were developed to lower the computational time, such as those based on machine learning (ML) [2], [8], [9], [10], [11], [12], the fluctuation sensitivity map (FSM) [13], the impedance field method [14], or the statistical model reported in [15].

In classical planar MOSFETs, the impact of the variability on the devices was estimated by the Pelgrom's Law [16], which states that the threshold voltage standard deviation (σV_{Th}) is proportional to the inverse square root of the effective metal gate area (A_g) and has been applied to different sources of variability [4], [5], [17]. This law can be extended to advanced tri-gate or gate-all-around (GAA) architectures by defining the A_g as the product between the gate length

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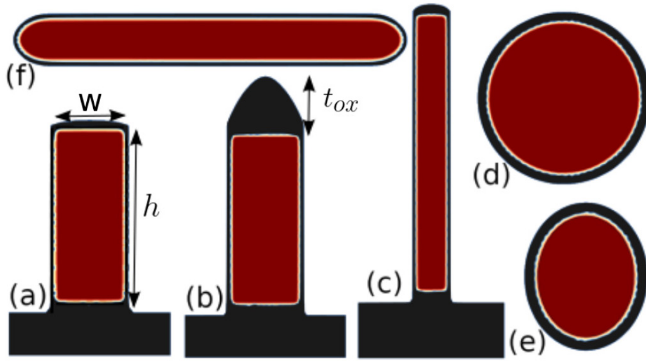

FIGURE 1. Cross-section of the three architectures used in this work. FinFETs: (a) from Wang et al. [19], and Leung and Chui [20], (b) from Seoane et al. [21], Indalecio et al. [22], and (c) from Seoane et al. [23]. NW FETs: (d) from Lü and Dai [24], Sung et al. [6], and (e) from Nagy et al. [25] and Elmessary et al. [3]. NS FETs: (f) from Nagy et al. [26] and this study.

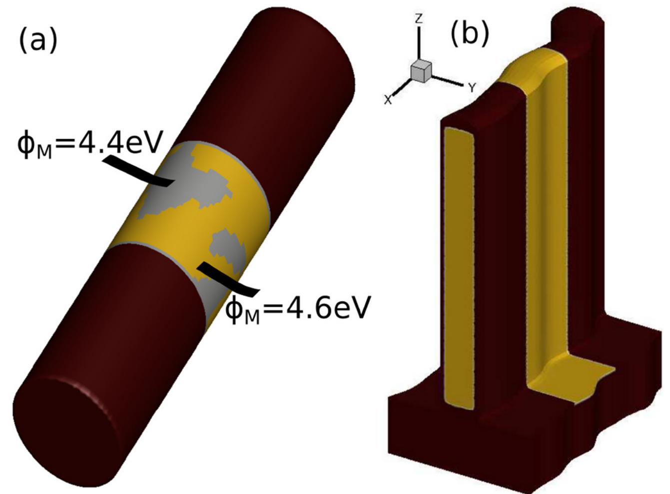

FIGURE 2. Scheme of (a) a gate-all-around (GAA) nanowire (NW) FET with a titanium nitride (TiN) metal gate affected by metal grain granularity (MGG) and (b) a FinFET affected by line edge roughness (LER) induced variability.

(L_g) and the effective gate perimeter (W^*):

$$\sigma V_{Th} = \frac{A_v}{\sqrt{A_g}} = \frac{A_v}{\sqrt{L_g W^*}}, \quad (1)$$

where A_v is the threshold voltage matching coefficient, which is determined by the contributions of all possible sources of transistor variations [18].

In this work, we present a novel Pelgrom-based predictive (PBP) model as a simple, fast, and reliable tool to estimate the impact of variability on advanced semiconductor devices. This model has been developed by analyzing the dependence of A_v with the intrinsic parameters for each variability source. We have successfully applied the PBP model to predict the σV_{Th} due to MGG and LER on three state-of-the-art architectures: FinFET, GAA nanowire (NW) FET and GAA nanosheet (NS) FET.

The structure of this paper is organized as follows. Section II includes the description of the benchmark devices and the simulation methods used in this work. In Section III and Section IV, we develop the PBP model for MGG and LER, respectively, comparing the predicted results with those extracted from literature. Finally, Section V summarizes the main conclusions of this paper.

II. BENCHMARK DEVICES AND SIMULATION METHODOLOGY

In this section, we initially present the benchmark devices used in this work. We study three semiconductor advanced architectures: FinFETs, NW FETs, and NS FETs, see 2D cross-sectional schemes in Fig. 1. Most of the FinFETs [21], [22], NW FETs [3], [6], [25], and NS FETs [26] are either directly based on experimental devices (FinFET [27], NW FET [28], NS FET [29]) or are scaled down versions of them. The FinFET used in [23] (Fig. 1(c)) is a tri-gate version of the NS FET from [29], based on current IRDS predictions [1]. Note that, the FinFETs from Figs. 1(a)-1(b) have similar semiconductor width/height ratio, $w/h \sim 0.4$, and differ on the top oxide height (t_{ox}), whereas the FinFET from Fig. 1(c) has a completely different ratio, $w/h \sim 0.1$. Also, the NW FETs have either circular ($w = h$, see Fig. 1(d)) or elliptical ($w \neq h$, see Fig. 1(e)) cross-sections. The NS FETs from this work (Fig. 1(f)) have a ratio of $w/h \sim 10.0$ based on [29].

All devices of this work have a titanium nitride (TiN) metal gate. TiN is a commonly used metal in the gate deposition due to several factors: its excellent thermal stability for the annealing process [30], its compatibility with silicon dioxide (SiO_2), and its low capacitance for ultralow-power circuit [31]. TiN has two possible metal grain orientations with work-functions (ϕ_M) of 4.4/4.6 eV, and occurrence probabilities of 40/60%, respectively [32]. The MGG profiles are generated using Poisson-Voronoi diagrams depending on the average grain size (GS) in most of the analyzed works [3], [6], [21], [22], [23], [25], [26]. Fig. 2(a) shows a scheme of a NW FET affected by MGG variability.

The LER is applied in TCAD studies using the Fourier transform of the Gaussian spectra [22], [33]. The spectra depends on two parameters, the correlation length (Λ) and the root mean square height (Δ). The Λ is a parameter that indicates how the deformation propagates to neighboring points of the surface. The Δ is the height of the deformation in the direction of the normal vector of a surface. The deformation is applied in the perpendicular direction (Y-axis) to the transport direction (X-axis), as can be seen in Fig. 2(b) for a FinFET affected by LER. The profiles studied in this work correspond to random uncorrelated LER. The Λ is reported to vary between 5 and 40 nm [34], which is consistent with SEM (scanning electron microscope) studies from EUV (extreme ultraviolet) lithography reported by [33], [35].

For completeness, when data are not available in literature, we carried out simulations using VENDES [36], an in-house-built simulation toolbox that reproduces the physics via 3D quantum corrected (QC) drift-diffusion (DD) transport

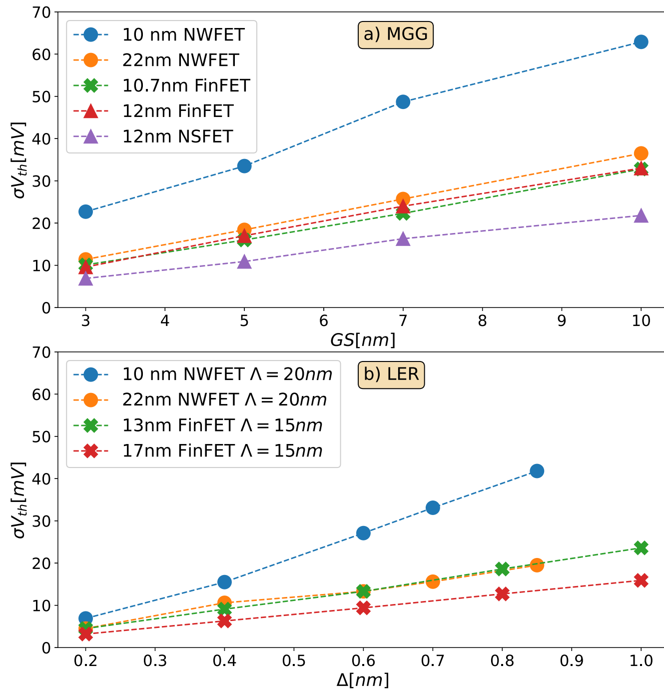

FIGURE 3. Threshold voltage standard deviation σV_{Th} versus: (a) the grain size (*GS*) for MGG variability, and (b) the root mean square (Δ) for LER variability. With these figures we validate the linearity assumption for the *GS* and Δ.

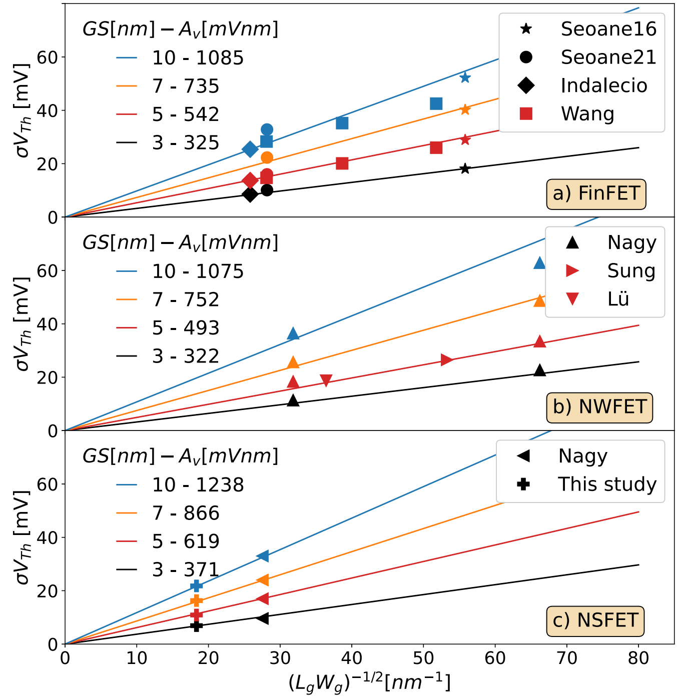

FIGURE 4. Pelgrom plots for the threshold voltage standard deviation (σV_{Th}) due to MGG variability at different grain sizes (GS), for: (a) FinFETs, (b) NW FETs, and (c) NS FETs. The analyzed data has been extracted from Seoane16 [21], Seoane21 [23], Indalecio et al. [22], Wang et al. [19], Nagy et al. [25], Lü and Dai [24], Sung et al. [6], Nagy et al. [26], or from simulations specifically done for this study. Note how the devices accurately follow the Pelgrom's Law and the lineal increase of the matching factor (A_v) with the GS.

method. For each simulation, the threshold voltage (V_{Th}) has been extracted using the MLFoMpy post-processing tool [37], applying the constant current criteria [38]. This value is set as the drain current that corresponds to the V_{Th} extracted by the lineal extrapolation method from the ideal undeformed device I-V characteristics.

III. PBP MODEL FOR METAL GRAIN GRANULARITY

MGG appears because of the random orientations of the metal grains produced in the gate deposition process [39]. The average size of these grains (GS) depends on the annealing temperature [32]. In this section, we consider that the MGG is the only source of variability that contributes to A_v. σV_{Th} increases linearly with the GS, as shown in Fig. 3(a), and as also previously demonstrated in [40], therefore:

$$A_v = \theta_{mgg} \cdot GS, \tag{2}$$

being θ_{mgg} the threshold voltage mismatch for the MGG variability. Also, as the MGG is a gate induced variability, in the Pelgrom's Law (1), W^* is the effective gate perimeter (W_g). The MGG induced variability for a particular device architecture can be predicted with the PBP model as follows:

$$\sigma V_{Th} = \frac{\theta_{mgg}}{\sqrt{L_g W_g}} \cdot GS. \tag{3}$$

MGG does not depend on the drain bias (V_D) as can be seen on [21], [25], and θ_{mgg} will depend on the device architecture and the metal used in the deposition process. Next, we are going to validate the model, by analyzing literature data for the benchmark devices.

Fig. 4 shows the Pelgrom plots for σV_{Th} due to MGG variability for each architecture: Fig. 4(a) FinFETs, Fig. 4(b) NW FETs, and Fig. 4(c) NS FETs. The results for different GS are presented, as well as their corresponding A_v and θ_{mgg} values. The simulations due to MGG reported in [6], [19], [21], [22], [23], [25], [26] together with this study simulations, were performed through QC DD methodology, but Lü and Dai [24] carried out classical DD simulations.

There is a linear relationship between σV_{Th} and $(LW_g)^{-1/2}$, following the PBP model for MGG (3). It is expected that the larger the gate area, the smaller the influence of the metal grains. Therefore, from a macroscopic point of view, when $(LW_g)^{-1/2} \rightarrow 0$ the gate will behave as a gate with a uniform ϕ_M value, and $\sigma V_{Th} \rightarrow 0$.

The slope of the Pelgrom plots (A_v) increases linearly with the GS for the three architectures (see Fig. 4) validating (2). Note that, all devices with the same architecture and metal on the gate, even having different shapes (see Fig. 1) and dimensions ($L_g W_g$), share a common θ_{mgg}. The W_g corresponds to the perimeter of gate surrounding the semiconductor for all devices presented in Fig. 1, except for the Fig. 1(b)-type FinFETs since, as demonstrated in [41] the grains located on the top of the gate do not impact on σV_{Th}.

TABLE 1. Predicted (σV^P_{Th}) vs. simulated (σV^S_{Th}) threshold voltage standard deviations at different grain sizes (GS) for each architecture due to metal grain granularity (MGG) induced variability. The relative error between the predicted and simulated data (σ_r), the gate length (L_g), the effective gate perimeter (W_g), and the V_{Th} mismatch for MGG variability θ_{mgg} are also shown. [*] corresponds to simulations done specifically for this work.

	GS [nm]	σV^P_{Th} [mV]	σV^S_{Th} [mV]	$\theta_{mgg} = 108\ mV$ σ_r	$L_g \times W_g$ [nm^2]	Ref.
FinFET	3	18.2	18.1	+0.6%	10.7×30.0	[21]
		9.2	10.1	-9.2%	12.0×105.0	[23]
		8.4	8.6	-2.3%	25.0×60.0	[22]
	5	30.3	28.9	+4.8%	10.7×30.0	[21]
		28.1	26.0	+8.1%	10.0×37.3	[19]
		21.0	20.1	+4.3%	14.0×47.8	[19]
		15.2	14.7	+3.3%	20.0×63.3	[19]
		15.3	16.0	-4.6%	12.0×105.0	[23]
		14.0	13.7	+2.2%	25.0×60.0	[22]
	7	42.4	40.2	+5.5%	10.7×30.0	[21]
		21.4	22.3	-4.0%	12.0×105.0	[23]
	8	22.4	21.8	+2.8%	25.0×60.0	[22]
	10	60.6	52.2	**+16.1%**	10.7×30.0	[21]
		56.1	42.5	**+32.0%**	10.0×37.3	[19]
		41.9	35.2	**+16.0%**	14.0×47.8	[19]
		29.1	28.3	+2.7%	20.0×63.3	[19]
		30.6	32.8	-6.7%	12.0×105.0	[23]
		28.0	25.4	+10.2%	25.0×60.0	[22]

	GS [nm]	σV^P_{Th} [mV]	σV^S_{Th} [mV]	$\theta_{mgg} = 107\ mV$ σ_r	$L_g \times W_g$ [nm^2]	Ref.
NW FET	3	21.4	22.7	-5.7%	10.0×22.8	[25]
		10.3	11.4	-9.6%	22.0×44.9	[25]
	5	35.6	33.5	+6.3%	10.0×22.8	[25]
		28.7	26.5	+8.3%	10.0×35.2	[6]
		19.6	18.7	+4.8%	20.0×37.7	[24]
		17.1	18.4	-7.1%	22.0×44.9	[25]
	7	49.8	48.7	+2.3%	10.0×22.8	[25]
		23.9	25.7	-7.0%	22.0×44.9	[25]
	10	71.2	62.9	**+13.2%**	10.0×22.8	[25]
		34.2	36.5	-6.3%	22.0×44.9	[25]

	GS [nm]	σV^P_{Th} [mV]	σV^S_{Th} [mV]	$\theta_{mgg} = 124\ mV$ σ_r	$L_g \times W_g$ [nm^2]	Ref.
NS FET	3	10.2	9.6	+6.3%	12.0×110.0	[26]
		6.8	6.9	-1.4%	18.0×165.3	[*]
	5	17.0	17.0	0.0%	12.0×110.0	[26]
		11.3	10.9	+3.7%	18.0×165.3	[*]
	7	23.9	24.0	-0.4%	12.0×110.0	[26]
		15.9	16.3	-2.5%	18.0×165.3	[*]
	10	34.1	33.0	+3.3%	12.0×110.0	[26]
		22.7	21.8	+4.1%	18.0×165.3	[*]

Therefore, to take into account only the grains located on the sides, for the Fig. 1(b)-type FinFET we define the gate effective perimeter as $W_g = 2h$. Note that, the $\theta_{mgg}/\sqrt{L_g W_g}$ ratio provides the sensitivity of a certain device to MGG variability.

In Table 1, we show a comparison of the threshold voltage standard deviation predicted by the PBP model (σV^P_{Th}), against the σV_{Th} coming from simulation studies (σV^S_{Th}) available in literature. Also, the GS, the relative error between predicted and simulated results (σ_r), the effective gate area ($L_g \times W_g$), and θ_{mgg} are shown. In Table 1, [*] indicates data simulated specifically for this study. Note that, as mentioned above, for a particular device architecture and metal on the gate, θ_{mgg} does not change, and once is determined (via the simulation of the MGG variability for two ensembles of devices with different $L_g W_g$ values) the impact of the MGG for any GS and device dimensions (L_g, W_g, w/h, t_{ox}) can be estimated using the PBP model according to (3). The larger prediction inaccuracies are due to the saturation of the standard deviations in devices with small A_g and large GS. This effect occurs because there are a few metal grains on the gate (e.g., for GS 10 nm, there are only 4 grains on the 10.7 nm×30.0 nm FinFET gate), transforming the normal V_{Th} distribution [22] into a bimodal distribution with peaks around the extreme ϕ_M values (4.4/4.6 eV), and breaking the linearity assumed by the PBP model. Avoiding the extreme cases previously mentioned (marked in bold in Table 1), all the predictions have a relative error of 10% or lower, highlighting that 91% of errors are 8% or smaller.

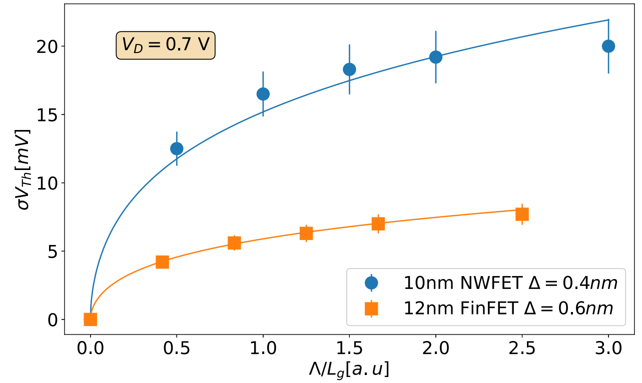

FIGURE 5. Threshold voltage standard deviation σV_{Th} versus the ratio between the correlation length and the gate length (Λ/L_g) for two architectures: (a) FinFETs [21], [22], and (b) NW FETs [3]. The root mean square (Δ) of each architecture is also shown. The solid lines represent the fit of each device to its own $f(\Lambda)$, and the y-error bars correspond to the 10% of each σV_{Th} value. The simulations were carried out at a drain bias (V_D) of 0.7 V. Note the good fit of $f(\Lambda)$ for two devices presented in the plot.

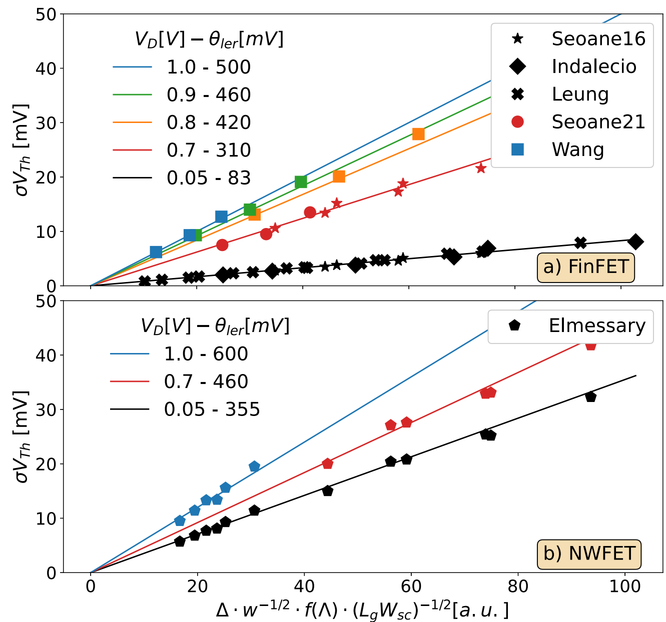

FIGURE 6. Threshold voltage standard deviation (σV_{Th}) versus $\Delta \cdot w^{-1/2} \cdot f(\Lambda) \cdot (L_g W_{SC})^{-1/2}$ plots due to LER variability at different drain biases V_D, for: (a) FinFETs, (b) NW FETs. Data extracted from Seoane16 [21], Seoane21 [23], Indalecio et al. [22], Wang et al. [19], Leung and Chui [20], and Elmessary et al. [3]. Note the excellent fit of the model with simulated data and the increase of θ_{ler} with the V_D.

TABLE 2. PBP model validation for LER. V_D is the drain bias, θ_{ler} the threshold voltage mismatch for LER variability, Λ the correlation length, $L_g \times W_{sc}$ the semiconductor area, and Δ the root mean square height. Also, the predicted (σV_{Th}^P), and the simulated (σV_{Th}^S) threshold voltage standard deviations are shown, together with their relative error (σ_r).

	V_D [V]	θ_{ler} [mV]	Λ [nm]	$L_g \times W_{sc}$ [nm]×[nm]	Δ [nm]	σV_{Th}^P [mV]	σV_{Th}^S [mV]	σ_r[%]	Ref.
FinFET	0.05	83	50	25.0×72.0	1.00	2.8	2.7	+3.7	[22]
					2.00	5.6	5.3	+5.7	
					3.00	8.4	8.1	+3.7	
			20	10.7×35.0	0.60	3.7	3.5	+5.7	[21]
					0.80	4.9	5.1	-3.9	
					1.00	6.1	6.0	+1.7	
				25.0×72.0	1.00	2.1	2	+5.0	[22]
					2.00	4.1	3.8	+7.9	
					3.00	6.3	6.9	-8.7	
			15	13.0×12.8	0.20	1.5	1.5	0.0	[20]
					0.40	3.1	3.2	-3.1	
					0.60	4.6	4.7	-2.1	
					0.80	6.1	6.3	-3.2	
					1.00	7.7	7.9	-2.5	
			15	17.0×16.0	0.20	1.1	1.1	0.0	[20]
					0.40	2.3	2.3	0.0	
					0.60	3.4	3.4	0.0	
					0.80	4.6	4.7	-2.1	
					1.00	5.7	5.9	-3.4	
			15	22.0×19.2	0.20	0.8	0.8	0.0	[20]
					0.40	1.7	1.7	0.0	
					0.60	2.5	2.5	0.0	
					0.80	3.4	3.3	+3.0	
					1.00	4.2	4.1	+2.4	
			10	10.7×35.0	0.60	2.9	2.8	+3.6	[21]
					0.80	3.9	3.8	+2.6	
					1.00	4.8	4.6	+4.2	
	0.70	310	20	10.7×35.0	0.60	13.7	13.4	+2.2	[21]
					0.80	18.3	18.8	-2.7	
					1.00	22.8	21.6	+5.6	
				12.0×105.0	0.60	7.7	7.5	+2.7	[23]
					0.80	10.3	9.5	+8.4	
					1.00	12.8	13.5	-5.2	
			10	10.7×35.0	0.60	10.8	10.6	+1.9	[21]
					0.80	14.4	15.2	-5.3	
					1.00	18.0	17.3	+4.0	
	0.80	420	30	10.0×37.3	0.33	13.0	13.1	-0.8	[19]
					0.50	19.7	20.1	-2.0	
					0.66	26.0	27.9	-6.8	
	0.90	460	30	14.0×47.8	0.33	9.1	9.3	+2.1	[19]
					0.50	13.8	14.0	+1.4	
					0.66	18.2	19.1	-4.7	
	1.00	500	30	20.0×63.3	0.33	6.2	6.2	0.0	[19]
					0.50	9.3	9.3	0.0	
					0.66	12.3	12.7	+3.1	

	V_D [V]	θ_{ler} [mV]	Λ [nm]	$L_g \times W_{sc}$ [nm]×	Δ [nm]	σV_{Th}^P [mV]	σV_{Th}^S [mV]	σ_r[%]	Ref.
NW FET	0.05	355	20	10.0×20.3	0.60	19.9	20.4	-2.5	[3]
					0.70	26.6	25.2	+5.6	
					0.85	33.2	32.3	+2.8	
				22.0×40.2	0.60	7.7	7.7	0.0	[3]
					0.70	9.0	9.3	-3.2	
					0.85	10.9	11.4	-4.4	
			10	10.0×20.3	0.60	15.7	15.0	+4.6	[3]
					0.70	21.0	20.8	+1.0	
					0.85	26.2	25.4	+3.1	
				22.0×40.2	0.60	5.9	5.7	+3.5	[3]
					0.70	6.9	6.8	+1.5	
					0.85	8.4	8.1	+3.7	
	0.70	460	20	10.0×20.3	0.60	25.8	27.1	-4.8	[3]
					0.70	34.4	33.1	+3.9	
					0.85	43.1	41.8	+3.1	
			10	10.0×20.3	0.60	20.4	20.0	+2.0	[3]
					0.70	27.2	27.6	-1.5	
					0.85	34.0	32.9	+3.3	
	1.00	600	20	22.0×40.2	0.60	13.0	13.3	-2.3	[3]
					0.70	15.1	15.6	-3.2	
					0.85	18.4	19.5	-5.6	
			10	22.0×40.2	0.60	10.0	9.5	+5.3	[3]
					0.70	11.7	11.4	+2.6	
					0.85	14.2	13.3	+6.8	

IV. PBP MODEL FOR LINE EDGE ROUGHNESS

The lithographic processes used in the production of nanoelectronic devices result in the appearance of surface roughness, affecting the device performance [33].

In this section, we consider that LER variability will be the sole contributor to A_v. LER induced σV_{Th} variability increases linearly with Δ, as shown in Fig. 3(b) and in the literature [3], [21], [22], [23], [25]. Also, σV_{Th} is inversely proportional to the semiconductor width (w, see Fig. 1), the critical dimension of deformation, since the narrower the device, the larger the expected effect of LER. In addition, σV_{Th} is proportional to a function of the correlation length ($f(\Lambda)$). This $f(\Lambda)$ is empirically defined based on the autocorrelation function that reproduces the surface roughness through the Gaussian spectra. Considering all these factors, the matching factor A_v is as follows:

$$A_v = \theta_{ler} \cdot \frac{\Delta}{\sqrt{w}} \cdot f(\Lambda), \tag{4}$$

with,

$$f(\Lambda) = \sqrt{\Lambda \cdot \left(1 - e^{-\sqrt{L_g/\Lambda}}\right)}, \tag{5}$$

being θ_{ler} the threshold voltage mismatch for the LER variability. Fig. 5 shows how σV_{Th} increases with the Λ/L_g ratio for a 10 nm NWFET with $\Delta = 0.4$ nm and a 12 nm FinFET with $\Delta = 0.6$ nm. The solid lines in Fig. 5 represent the $f(\Lambda)$ (5) that fits the data, and the vertical error bars correspond to the 10% of the σV_{Th} values. Since LER impacts the semiconductor width by narrowing or widening it, in the Pelgrom's Law (1), W^* is the semiconductor perimeter (W_{sc}). With the previous concepts, the PBP model for the LER induced variability is described as follows:

$$\sigma V_{Th} = \theta_{ler} \cdot \frac{\Delta}{\sqrt{w}} \cdot \frac{f(\Lambda)}{\sqrt{L_g W_{sc}}} \tag{6}$$

Unlike for the MGG variability, the V_D has a high impact on the increase of σV_{Th} for LER [3], [21], [25]. Therefore, θ_{ler} will depend on the device architecture and the V_D.

Fig. 6 shows σV_{Th} versus $\Delta f(\Lambda)(w L_g W_{sc})^{-1/2}$ for the FinFETs (top figure), and the NW FETs (bottom figure). Also, the θ_{ler} values are presented at different drain biases (V_D).

Note that, LER variability is not studied for the NS FET since, as seen in [23], the impact on this architecture is negligible ($\sigma V_{Th} \leq 1.0$ mV) because the roughness due to the etching processes is on the non-critical dimension. The simulations due to LER variability reported in [3], [19], [21], [22], [23] were performed with QC DD methodology.

θ_{ler} is determined as the slope of the Fig. 6 plots, increasing with the V_D for the two architectures. For each architecture and V_D, all devices independently on the shape (see Fig. 1(a)-(e)), Λ and Δ share a common θ_{ler}. Once θ_{ler} is determined, the PBP model can be used to predict the impact of the LER for any set of Λ, Δ parameters and device dimensions (L_g, W_{sc}, w). Note that although θ_{ler} has no physical meaning, the $\theta_{ler}/\sqrt{L_g W_{sc}}$ ratio provides an estimation of the sensitivity of a device to LER variability. Table 2 shows the comparison between the predicted (σV_{Th}^P) and simulated (σV_{Th}^S) data, to estimate the accuracy of the PBP model for LER. A wide range of Λ (10 nm to 50 nm), and Δ (0.2 nm to 1.0 nm) values are presented. We observe that for all data the relative errors (σ_r) between the predicted

and simulated σV_{Th} values are below 9%, with 94% of them being below 6%, demonstrating the validity of the estimation provided by the Pelgrom-based predictive model.

V. CONCLUSION

We have presented a novel Pelgrom-based predictive (PBP) model that characterizes the impact of metal grain granularity (MGG) and line edge roughness (LER) induced variabilities on semiconductor device performance. The PBP model was applied to state-of-the-art FinFETs, NW FETs, and NS FETs, with prediction errors of 10% or lower for all data inside the model limits, demonstrating its adaptability to a variety of architectures, dimensions, cross-sectional shapes, and intrinsic variability parameters. Also for MGG, the 91% of the relative errors are 8% or lower and for LER, the 94% of the relative errors are below the 6%. The PBP model only fails to predict the MGG when the gate area ($L_g W_g$) and the grain size (GS) are comparable.

We have demonstrated that the PBP model provides a simple, fast, and reliable estimation of the impact of the major contributors to nanoelectronic transistor variability, with several dimensions, and architectures. This predictive tool could guide the industry and academia in the development of new generation variability-resistant device architectures.

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