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Graphene–Silicon Diode for 2-D Heterostructure Electrical Failure Protection

MUHAMMAD ABID ANWAR, MUNIR ALI, DONG PU, SRIKRISHNA CHANAKYA BODEPUDI, JIANHANG LV^{id},
KHURRAM SHEHZAD, XIAOCHEN WANG, ALI IMRAN, YUDA ZHAO (Member, IEEE), SHURONG DONG^{id},
HUAN HU^{id} (Member, IEEE), BIN YU, AND YANG XU^{id} (Senior Member, IEEE)

School of Micro-Nano Electronics, ZJU-Hangzhou Global Scientific and Technological Innovation Center, ZJU-UIUC Joint Institute,
State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027, China

CORRESPONDING AUTHOR: Y. XU (e-mail: yangxu-isee@zju.edu.cn)

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ABSTRACT Two-dimensional materials have modernized a broad interest in electronic devices. Along with many advantages, their atomic-level thickness makes them sensitive under high electrical stress. This work proposes a protection design using a Graphene/Silicon (Gr/Si) Schottky diode as the protective device, which helps to improve the endurance for unwanted fluctuations in operating voltage of 2D heterostructure-based devices. In this scheme, the 2D heterostructure was configured parallel with the protective device (Gr/Si diode) for electrical measurements. It was found that Gr/Si diode handles a large portion of initial surge current peaks, which significantly increases the durability and lifetime of 2D material-based heterostructure devices. This scheme potentially bridges mature CMOS technology and novel 2D-based heterostructure applications for robust futuristic devices.

INDEX TERMS Protection device, electrical stress, graphene/silicon diode, 2D heterostructure PN diode.

I. INTRODUCTION

Two-dimensional (2D) vertical and lateral heterostructures have attracted much attention due to their fascinating optoelectronic properties and potential applications for various fields [1], [2], [3], [4], [5]. Therefore, numerous research has demonstrated that 2D materials (graphene, MoS₂, WSe₂, and many others) with different work functions permit the fabrication of heterostructure with different functionalities, such as PN diodes, photodetectors, and sensors [1], [6]. However, the impact of time-dependent instabilities in the 2D heterostructure demands special considerations. Electrical stress is one of the most common causes of failure in microelectronic devices, especially in those based on hybrid 2D material-based van der Waals (vdW) heterostructure [7], [8], [9], [10], [11], [12]. Such events generate a high surge current which significantly affects device electrical and optical performance, while permanent damage could result in severe cases. Maintaining operational stability and robustness of devices prone to unwanted and abrupt input changes (current or voltage)

is paramount. For decades, traditional Si-based protection devices have been used to accomplish this [13]. However, due to their fabrication complication and continued to scale down, conventional devices could not meet the demands of advanced levels of protection, encouraging the need for unique device structures.

Here, we explore the dynamic properties of the vertical (Gr/Si) and lateral (MoS₂/WSe₂) heterostructure and proposed protection design. Our proposed model is a simple and promising strategy of connecting the Gr/Si diode parallel to the 2D-PN diode to share its electrical stress, initial surge current peak, excessive heating, and extending the electrical life of 2D-based heterostructure devices. It was found that the initial surge current peak is significantly reduced when the 2D PN diode is connected parallel with Gr/Si diode, which can improve the device operating voltage range. The high carrier mobility of graphene [14], low resistance, parasitic effects [15], high thermal conductivity [16], lower noise, self-powered [17], broadband photodetector [18], [19], large surge current capability, and lower reverse recovery time [15]

prevent overheating during electrical stress and serve as an electrical protection device.

II. EXPERIMENTAL SECTION

The Gr/Si Schottky devices are fabricated on a low-doped n-type Si wafer. The 1st lithography patterns Au/Ti (70/10 nm) electrodes. The Si window is exposed, and the wafer is deep into buffered oxide etchant to remove the oxide layer in the 2nd lithography. Then, graphene is chemically transferred onto the Si window to form a Schottky junction. As a conducting channel, a monolayer CVD graphene was transferred onto the Si window to form the Schottky junction. Before transfer, we etched the graphene grown on the backside of Cu foil by O₂ plasma to avoid Cu residues between the top and back sides of graphene. A layer of polymethyl methacrylate (PMMA) film is smoothly coated on the surface of the top side graphene and backed at 105 °C for 5 minutes. After spin-coated, the PMMA/graphene/Cu is put into the copper sulfate etching solution (5H₂O·CuSO₄ : HCl : H₂O = 15.6 g:50 mL:50 mL) for back copper etching for a minimum of six to eight hours. Graphene film supported by PMMA was picked by a glass slide and washed with deionized water (DI) before being transferred to the target device. Then, PMMA was removed by dichloromethane (DCM) at 50 °C for 3 to 4 minutes and washed in acetone and isopropanol. Finally, the 3rd lithography was performed to pattern graphene, and O₂ plasma was used to remove unwanted graphene on the surface [2]. A metallic Ohmic contact is formed on the backside of the Si substrate.

The 2D-PN heterostructure was fabricated by mechanically exfoliated Nano flakes from bulk crystals onto a Si wafer with a 100-nm thick SiO₂ substrate. A transparent glass slide used as a stamp holds a water-soluble polyvinyl acetate (PVA) sheet on the top side and elastomeric polydimethyl siloxane (PDMS) placed below the pick-up and release processes. A micromanipulator deploys the stamp to the target location and affixes it to the MoS₂ flakes. The stamp was heated at 85 °C for 3 minutes and cooled down to room temperature, and this process increases adhesion between PVA film and MoS₂ flakes. WSe₂ flakes were picked up on the same stamp using the same method. The vdW stack is released on a Si/SiO₂ substrate having pre-fabricated metal electrodes. The PVA and residual polymer were removed using deionized water (DIW) acetone and isopropanol. A semiconductor analyzer (Agilent B1500A) was used for electrical characterization, and a signal generator (Rigol DG1000Z) with a voltage amplifier (Falco Systems WMA-300) was used to perform dynamic characterization.

III. RESULT AND DISCUSSION

The 3D schematic, current-voltage (I-V) characteristics in logarithmic scale (inset: Dynamic measurements circuit), Raman, and SEM of the Gr/Si Schottky diode are presented in Fig. 1(a-c). The electrical properties of the Gr/Si Schottky diode were characterized by thermionic emission theory (T.E).

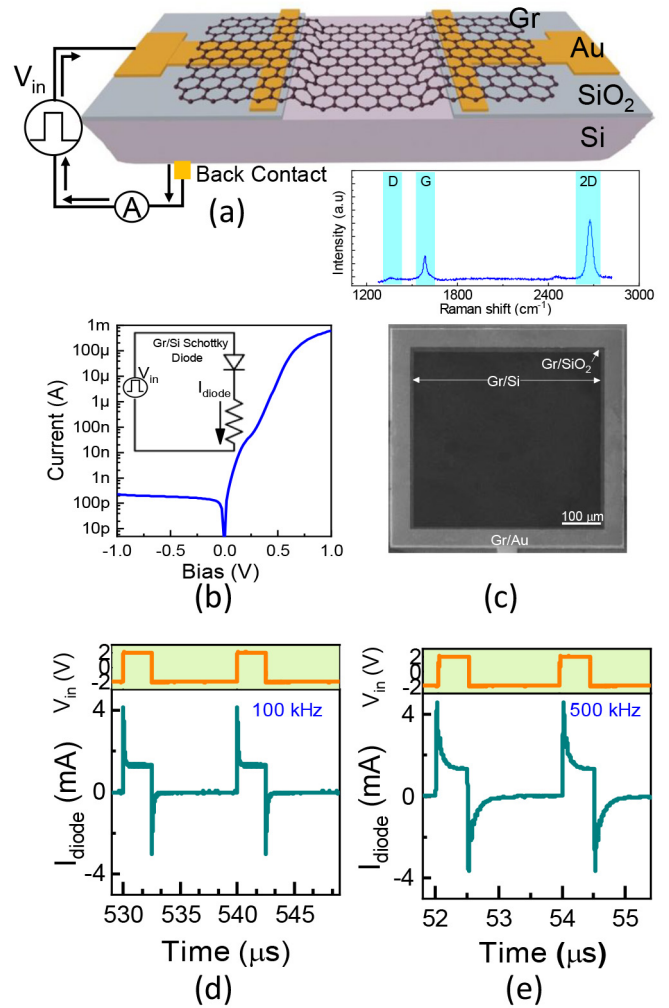


FIGURE 1. (a) 3D schematic of the Gr/Si Schottky device. (b) Current-Voltage (I-V) characteristics of Gr/Si Schottky diode in logarithmic scale (inset: measurements circuit). (c) Raman (top) and SEM (Bottom) image of CVD Gr/Si Schottky diode. (d, e) Temporal response of the Gr/Si Schottky diode at different frequencies (Device size: $0.5 \times 0.5 \text{ mm}^2$).

A linear fitting was performed in the forward bias range to extract the Schottky diode parameters, such as ideality factor (n) and Schottky barrier height (Φ_{SBH}), by using $\ln(\text{current density-voltage})$ characteristics [20]. The I-V characteristics of the Gr/Si Schottky diode showed low dark current with ideality factor ($n = 1.5$), and Schottky barrier height ($\Phi_{\text{SBH}} = 0.6 \text{ eV}$) has been calculated by the Cheung's method [20].

Traditionally, the excess majority of charge carriers cross the junction when the device is switched from reverse to forward mode, significant initial current spike is observed in both regions (forward and reverse) [21], [22], [23]. This initial spike indicates an abrupt current activity after the switching, substantially crowding the junction for a few nanoseconds (ns). The temporal response of the I_{diode} at different operating frequencies is shown in Fig. 1(d, e). This sensitive photodiode device responds to light and generates photo-excited carriers, which causes anomalous photocurrent [24]. The dynamic

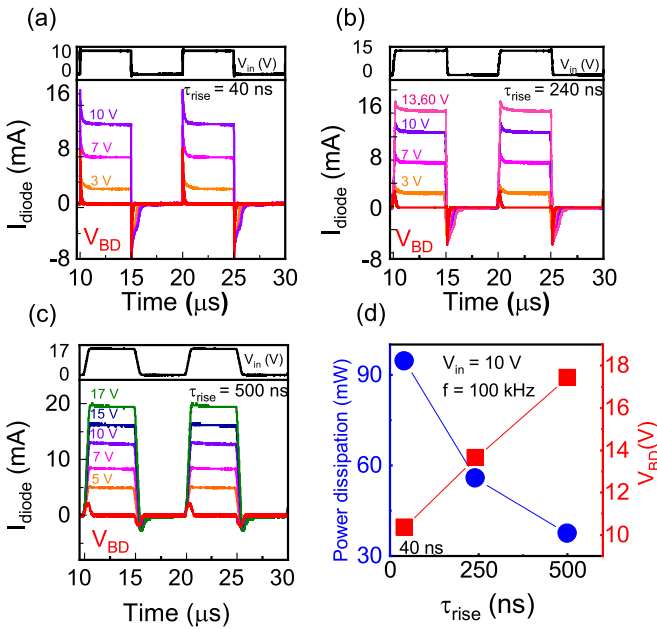


FIGURE 2. The temporal characteristics of the device under different rise times (a) 40 ns, (b) 240 ns, and (c) 500 ns. (d) Power dissipation and breakdown voltage at different rise times.

testing has been carried out in dark mode and at room temperature to eliminate the possibility of any unintentional photocurrent throughout the testing. Probing diode current, I_{diode} only includes charge movement due to input signal voltage variations. Alternatively, a square input pulse signal with ($V_{pp} = 2$ V) is applied to operate the device in forward and reverse mode. The amplitude of initial spikes in the forward and reverse modes at variable frequencies remained unchanged, confirming a clean Gr/Si junction and less contribution of trapped charges which causes irregular spiking at high switching frequency.

The electrical input signal modulates the doping concentration of graphene at the Fermi level [25], [26], [27], with limited charge transfer at the graphene-metal interface because of the low density of the states. The electrons from Si, which were transferred to graphene during forward biasing, give rise to the initial peak current while switching the polarity. These excess electrons in the graphene are directly proportional to the initial peak current, which significantly impacts heating and device stability.

As shown in Fig. 2 (a-c) the device endurance was evaluated with different rising times of 40 ns, 240 ns, and 500 ns by gradually increasing the input voltage (V_{in}) until the device experiences breakdown. The duty cycle and operating frequency of the input signal were fixed at 50% and 100 kHz, respectively. It can be seen that a relatively fast turn-on time (40ns) produces a sharp current spike compared to a rise time of 240 ns and 500 ns, as presented in Fig. 2 (a-c). This initial spike indicates a surge of carriers at the interface due to significant charge crowding (Fig. 2a), which also results in heating. More pronounced heating at faster turn-on times will result in lower breakdown voltage. The

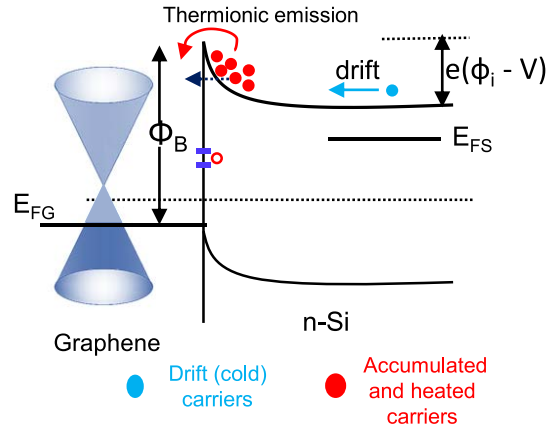


FIGURE 3. The energy band diagram of the Gr/Si Schottky diode under pulsed bias.

breakdown voltage was increased from 10.34V to 17.44V by reducing the rise time of the input signal. Considering that shorter pulse duration (fast rise and fall time), as opposed to the shorter stressing period, may make the discharging less sensitive [28]. When the input signal has a relatively longer rise/fall times, charges find sufficient time for recombination and thus lower initial peaks in the forward and reverse regions. It can be concluded that breakdown voltage and initial peak current depend on the rise time of the input signal. The enhancement in V_{BD} at slower turn-on times is attributed to reduced power dissipation in the device, which can be calculated as follows ($P_{Dissipation} = (E_{ON} + E_{OFF}) f_{Switching}$) [29]. The V_{BD} and power dissipation as a function of rising/falling time are plotted in Fig. 2(d).

The energy band diagram of the Gr/Si Schottky diode is presented in Fig. 3. After the immediate application of the electric field across the semiconductor-graphene junction, the drifted (cold) carriers accumulate at the interface. The accumulation of charge carriers at the interface redistributes the energy within the electrons and the surroundings and generates heated carriers. These carriers with sufficient energy participate in thermionic emission and tunneling, as displayed in Fig. 3.

In the case of pulsed biasing, during the rise time of the electric field, the heated carriers at the interface redistribute their energy with the newly arrived drift (cold) carriers. For a slower rise time of the electric field, the total heating distributes over larger cold carriers arriving at the interface and helps the cooling process. Whereas, in case of a sharper rise in the electric field, carrier energy redistributes within fewer carriers, generating comparatively higher energy carriers that participate in the thermionic emission and tunneling process, resulting in a higher interface current at the beginning of the electric pulse. These momentary charge carriers substantially impact device stability performance and lifetime. This sharp peak in the response current decreases with the continuous supply of drift carriers and electron-phonon interactions that contribute to the forward steady state current (cooling process).

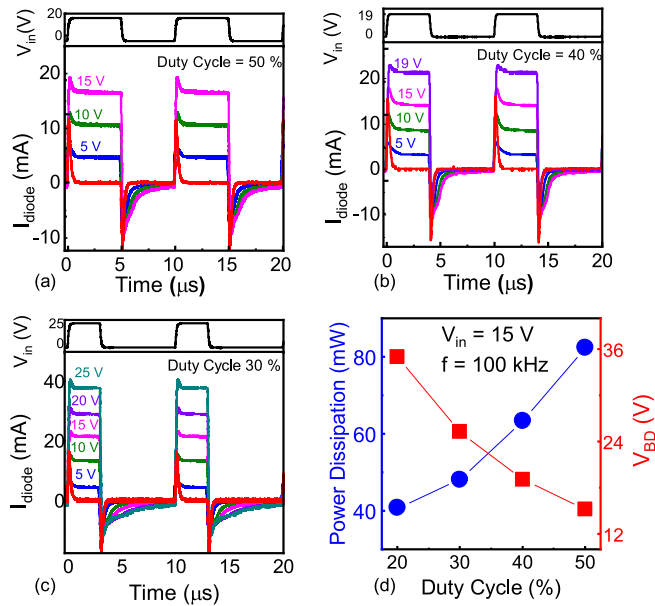


FIGURE 4. Effect on V_{BD} with different duty cycles (a) 50% (b) 40% (c) 30% (at 400 ns rise/fall times). (d) Power dissipation is a function of the duty cycle with fixed input bias voltage and frequency (Device size: $0.5 \times 0.5 \text{ mm}^2$).

Moreover, the device ON-time (or duty cycle) plays an essential role in the Joule heating [30], [31]. The charges from Si, which were accumulated in graphene during forwarding biasing, give rise to the initial peak current while switching the polarity. The amount of accumulated charges at the Gr/Si interface is directly proportional to the duty cycle of the input signal, contributing to charge crowding and influencing the device heating and stability. The device was tested with various duty cycles to understand the dependence of Joule heating. The duty cycle varied from 50%, 40%, and 30%, and the V_{BD} increased from 15.2 V to 25.3 V (see Fig. 4(a-c)).

Power dissipation is a critical factor in assessing device endurance and breakdown characteristics. The power dissipation as a function of different duty cycles and breakdown voltage are shown in Fig. 4(d) at fixed bias voltage and frequency. As the frequency was increased, power dissipation increased significantly due to the higher oscillations at higher frequencies presented in Fig. 5(a). Higher phonon density at higher frequencies raises the lattice temperature. The accumulated charge at the interface is lesser for shorter duty cycles, minimizing the reverse recovery time (τ_{rr}), as shown in Fig. 5(b). The quick recovery in the reverse mode allows the device to operate at higher frequencies.

Fig. 6(a) shows the forward temporal response of the current for the Gr/Si protective diode under different voltage conditions varying between -5 to 35 V with a 20% duty cycle. The reverse bias characteristics of the Gr/Si diode are presented in Fig. 6(b). It is essential to observe that settling times at different $V_{reverse}$ remains the same, which is strong evidence of charge independent of dark current. The only difference between different reverse biasing conditions is the

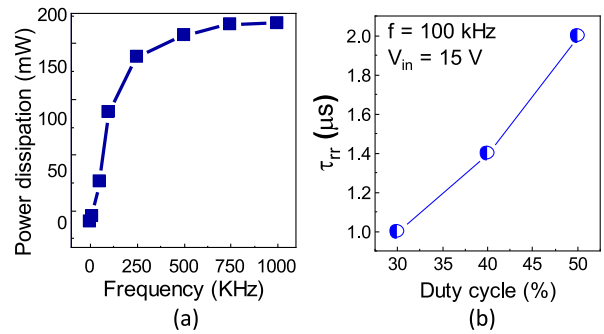


FIGURE 5. (a) Power dissipation increases with the input operating frequency. (b) Reverse recovery time increase with different duty cycles.

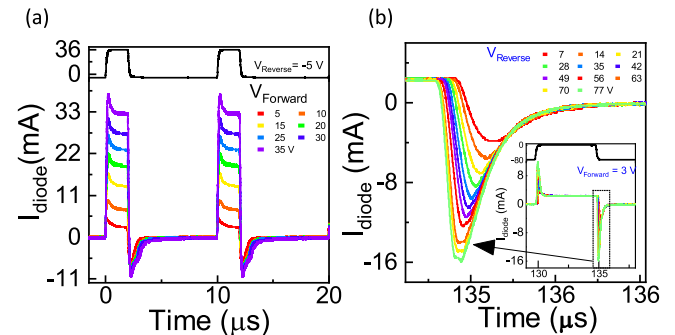


FIGURE 6. Temporal response Gr/Si Schottky diode (a) Forward and (b) reverse endurance measurements with operating frequency = 100kHz (Device size: $0.5 \times 0.5 \text{ mm}^2$).

amplitude of the initial spike, which has a direct relationship with $V_{reverse}$. Our results revealed that Gr/Si Schottky diode has excellent endurance with low dark current, high forward current capability, and high forward/reverse operating voltage which justifies high-amplitude voltage spikes bearing ability as shown in Fig. 6(a, b). The inset of Fig. 6(b) presents an overall temporal response of the spike with gradually increasing the reverse voltage and fixed forward bias.

Sensitive circuits are prone to damage due to abrupt surges, overvoltage threats, and transient signals at the input terminal, which need circuitry to facilitate safe operation. Electrostatic discharges (ESDs) are mixed with input biasing for a brief time and appear as surges or spikes that may exceed the device breakdown thresholds. Hence, the strategy is needed to fabricate a robust enough device or create a safe protection route allowing excessive surge currents and limiting the currents through delicate devices in safe operational ranges. The outstanding physical properties of the Gr/Si Schottky diode offer low dynamic resistance, lower leakage current and reverse recovery, and higher withstand voltage, serving as an electrical protection device.

The Gr/Si protective diode in parallel with a 2D heterostructure ($\text{MoS}_2/\text{WSe}_2$) diode is shown in Fig. 7(a). The Raman spectra of WSe_2 , $\text{WSe}_2/\text{MoS}_2$, and MoS_2 heterostructure and the optical image are shown in Fig. 7(b, c) with the thickness of $\text{WSe}_2/\text{MoS}_2$ ($\sim 30/\sim 15$ nm). The static current-voltage characteristics of the 2D PN diode are presented in Fig. 7(d). The accumulated charges during

forwarding biasing give rise to the initial surge current while switching the polarity. These accumulated charges are directly proportional to the forwarding biasing, which increases the initial overshoot current in both directions (forward and reverse). This initial overshoot current was adversely affecting the lifetime of the device. The higher the forward voltage, the large the accumulated charge at the interface, taking longer to reach the steady state. Our findings showed that with increasing input bias, the initial peak current rises, which contributes to the overall heating of the device and causes device failure. The initial overshoot current peak intensities under different input pulses were observed (Fig. 7(e, f)).

When the Gr/Si diode is connected in parallel with the 2D PN diode, any surges or spikes in the circuit will appear on both devices simultaneously. Due to ultrafast response time and high current absorbing ability, the Gr/Si diode will absorb spikes and protect 2D sensitive devices. We simultaneously monitor the current of the 2D-PN and Schottky diode to observe the amount of current distributed at both devices. The Gr/Si Schottky diode routes excessive current to the circuit ground without letting it reach the sensitive circuit (2D-PN diode). The temporal current through 2D PN and Gr/Si Schottky diode with three configurations are presented in Fig. 7(g-i). In case I, the testing condition shows both devices are connected in parallel configurations (Fig. 7(g)). It is evident from the result that in the presence of electrical stress (V_{in}) in the circuit, Gr/Si silicon Schottky diode reacts more quickly after reaching its threshold voltage and absorbs most of the initial current. In the configuration presented in case II with a voltage clamping source of 3V connected in series with the Schottky diode, Gr/Si Schottky diode does not conduct in either biasing. In that way, Gr/Si diode will wake up only when input biasing or unwanted spikes exceed 3.5V. Until then, the 2D PN will safely perform rectification per its designed parameters (Fig. 7(h)). In case III, when there are overvoltage's in the circuits or spikes in the input, the Gr/Si diode turns on immediately, and a more significant portion of the current will pass through the Gr/Si diode instead of the 2D-PN diode, which helps in reduction of the electrical stress at 2D-PN diode and avoids breakdown as depicted in Fig. 7(i). A keen observation revealed that when the 2D PN diode is measured separately, the initial spike current was more prominent at switching input bias when compared with the cases I-III, which justifies that the Gr/Si diode passes the majority of current through it.

For a broader perspective, future electronics will be based on thin film materials capable of performing multiple tasks. It can be made possible by engineering their geometrical structure, interlayer charge dynamics, and selective excitonic properties to be employed in retinomorphic and neuro-morphic sensing and computing. These developments have emerged artificial neural networks as a baseline for computationally complex real-world problems. We expect a rapid interest in developing such nanoelectronics-based devices with the help of 2D materials, thin film transistors, and

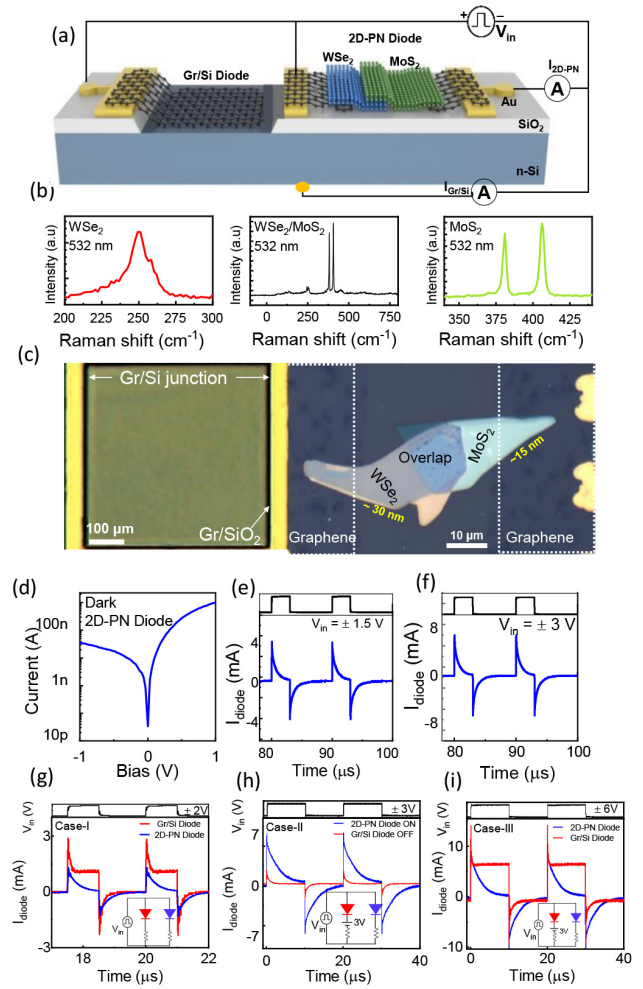


FIGURE 7. (a) Cross-section view of Gr/Si protection diode coupled with 2D-PN diode. (b) Raman spectra of WSe₂, WSe₂/MoS₂ and MoS₂ heterostructure (c) Optical image of the Gr/Si Schottky and 2D-PN diode heterostructure. (d) Static I-V characterization of the 2D-PN diode. (e, f) The temporal characteristics of the 2D-PN diode under different biasing voltages. (g-i) The current temporal response through 2D PN and Gr/Si Schottky diode with three configurations.

TMDCs. Several types of research have investigated the failure mechanism in low-dimensional materials such as MoS₂, WSe₂, black-phosphorus (BP) [3], [5], [6], [7], carbon nanotubes (CNTs) [8], [9], [10], graphene nanoribbons (GNR) and thin film graphene [11], [12], [13], [14].

By providing a safe testing environment foundation and suitable circuitry, we can protect and extend futuristic 2D materials. In this article, we presented one protection scheme that can be further refined according to material-specific structures to extend the lifetime of the 2D materials-based devices.

IV. CONCLUSION

In this study, dynamic characteristics for the failure of the Gr/Si Schottky diode are systematically investigated for its potential in electrical and electrostatic stress applications. Dynamic biasing leads to Joule heating, one of the major causes of electrical breakdown. Such events generate a high surge current which significantly affects device electrical and

optical performance, while permanent damage could result in severe cases. We demonstrated a strategy to protect 2D material-based devices from electrical stress. It has been observed that electrical input spikes are significant reasons for the electrical failure in the 2D heterostructure. The ultra-fast response of the Gr/Si Schottky diode can effectively bypass electrical spikes and avoid the electrical breakdown of the 2D heterostructure when placed in a parallel circuit configuration. Therefore, this study provides an overall picture of the failure mechanisms of Gr-based Schottky diode under dynamic biasing conditions, leading to protection circuits for 2D heterostructures and extending the device lifetime.

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