Received 8 August 2022; revised 17 September 2022; accepted 3 October 2022. Date of publication 10 October 2022;
date of current version 17 October 2022. The review of this article was arranged by Editor K. Joshi.

Digital Object Identifier 10.1109/JEDS.2022.3212697

Characterization of Oxide Trapping in SiC MOSFETs Under Positive Gate Bias

YE LIANG[1,2], YUANLEI ZHANG[1,2] (Graduate Student Member, IEEE), JINGQUN ZHANG[1,2], XIUYUAN HE[1,2], YINCHAO ZHAO[3], MIAO CUI[1,2], HUIQING WEN[1,2] (Senior Member, IEEE), MINGXIANG WANG[4] (Senior Member, IEEE), AND WEN LIU[1,2] (Member, IEEE)

1 School of Advanced Technology, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China
2 Department of Electrical Engineering and Electronics, University of Liverpool, L69 3GJ Liverpool, U.K.
3 School of Intelligent Manufacturing Ecosystem, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China
4 School of Electronic and Information Engineering, Soochow University, Suzhou 215006, China

CORRESPONDING AUTHORS: W. LIU and M. WANG (e-mail: wen.liu@xjtlu.edu.cn; mingxiang_wang@suda.edu.cn)

This work was supported in part by the Suzhou Science and Technology program under Grant SYG201923; in part by the Key Program Special Fund in Xi'an Jiaotong–Liverpool University (XJTLU) under Grant KSF-T-07; and in part by XJTLU Research Development Fund under Grant PGRS1912003 and Grant RDF-20-02-62.

ABSTRACT SiC MOSFETs devices with double-trench dominate the market due to their low on-resistance. However, studies on its temperature-dependent properties are not comprehensive. This work uses fast I-V and static I-V techniques to explore the location of electrons trapped in the device under moderate gate stress. Threshold voltage instability (V_{TH} hysteresis and ΔV_{TH}) and on-resistance degradation (ΔR_{ON}) are used to characterize oxide trapping. Although the observation method is different, it can be found that the V_{TH} instability and R_{ON} degradation increase linearly with logarithmic time over a wide time range from 100 μs to 10^4 s, suggesting that the direct tunneling mechanism dominates the electrons trapping in the oxide near the SiO_2/SiC interface. The interface trap density is 3.8×10^{12} $cm^{-2}\cdot eV^{-1}$. In addition, a negative temperature dependence is shown in the test, and the fitting parameter γ from 0.16 to 0.18 indicated that these traps are concentrated in the oxide layer. These traps' energy level at 0.68 eV below the conduction band was obtained in the recovery phase through the Arrhenius plot.

INDEX TERMS Activation energy, fast I-V technique, MOSFETs, on-resistance degradation, positive-bias stress, silicon carbide, static I-V technique, threshold voltage instability.

I. INTRODUCTION

Silicon carbide (SiC) is considered a promising wide bandgap semiconductor material to supersede silicon for developing high-efficiency, high-power, and high-temperature electron devices [1]. In particular, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to meet the growing demand for electrical power generation, distribution, and switching due to their high breakdown voltage, low conduction, and low switching loss capabilities [2], [3].

Studying the positive gate stress of SiC MOSFETs is crucial to circuit design. For example, SiC MOSFET is usually used as the DC circuit breaker in protection circuits, gated on for prolonged periods. The changed threshold voltage (V_{TH}) under positive gate bias would cause a response time delay of the faulty system [4]. V_{TH} instability is generally characterized by threshold voltage shifts (ΔV_{TH}) and hysteresis (V_{TH} hysteresis). Besides the V_{TH}, the on-state drain-to-source resistance ($R_{DS(ON)}$ or R_{ON}) is an important parameter related to power loss.

Semiconductor manufacturers enthusiastically research device structures and optimize gate oxide to restrict V_{TH} instability and alleviate the R_{ON} degradation [4], [5], [6], [7]. Several papers have investigated the negative or positive temperature dependence of V_{TH} instability and R_{ON} degradation in planar structures [3], [8], [9], [10], yet few studies on the trap level of devices [8]. Meanwhile, very little is known about trench gate structure [7], [11]. Although some articles have observed that trench gate structures had larger V_{TH}

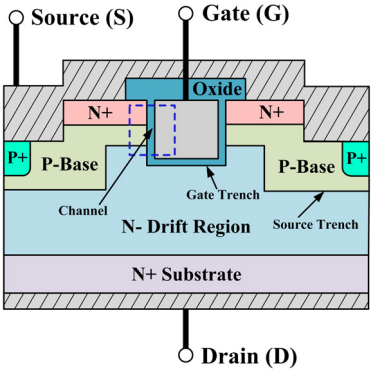

FIGURE 1. The typical device structure of double trench SiC MOSFETs [14].

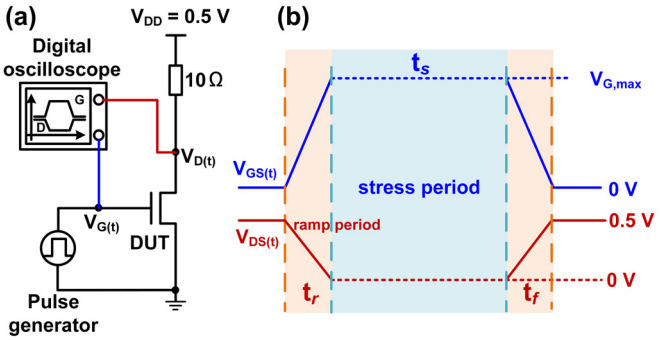

FIGURE 2. (a): Schematic experiment setup for fast I-V measurement. (b): $V_{GS(t)}$ pulse and $V_{DS(t)}$ response waveforms. t_s: stress time and $t_{r/f}$: up/down ramping time.

instability than planar gate structures under the same gate bias [12], [13].

Double trench devices dominate the market due to their low on-resistance. However, there is still a research gap on the temperature-dependent properties of the double trench structure. In this work, fast I-V and static I-V methods are used to investigate the V_{TH} instability and R_{ON} degradation over a wide time range from 100 µs to 10^4 s under moderate stress voltages. The trap level and their distribution are analyzed and calculated. These results may help manufacturers to optimize the gate oxidation process and improve the threshold voltage stability of the device.

The organization of this article is shown below. Section II investigates the V_{TH} hysteresis and R_{ON} degradation with different ramp speeds, gate stress voltages, and stress times using the fast I-V technique. Section III investigates the device degradation under gate stress at high temperatures over a broad time scale using the static I-V technique. Section IV is the conclusion part.

II. FAST I-V EXPERIMENTAL PROCEDURE AND TEST RESULTS

The SiC MOSFETs studied in this work came from leading commercial manufacturers. From its datasheet, the device has a breakdown voltage of 1200 V and $R_{DS(ON)}$ of 105 mΩ, measured at V_{GS} = 18 V and I_D = 7.6 A at room temperature. The simplified structure of SiC MOSFETs with double trench is shown in Fig. 1. According to their technical report, the source trenches can effectively disperse the electric field at the bottom of the gate trench [14].

Fast I-V measurement relied on a paramet er analyzer system involving Agilent DSO-X 2024A digital oscilloscope, Agilent E3647 DC power supply, Rigol DG 2041A pulse generator, and computer control program [15], [16]. A schematic experiment setup for fast I-V measurement is shown in Fig. 2 (a). Changeable square pulses were applied to the gate terminal of the devices under test (DUTs). The load resistance (R_L) of 10 Ω was carefully selected for limiting resonance and a low off-state current. During DUT's switching along the load line, the voltage waveforms of the gate ($V_{GS(t)}$) and drain ($V_{DS(t)}$) terminals were simultaneously recorded by the digital oscilloscope with the sampling rate of 50 M/s, as exhibited in Fig. 2 (b). A small V_{DD} of 0.5 V was selected to eliminate the current collapse and hot-electron effect [16]. It is worth mentioning that before the test, all terminals of the DUTs were grounded for 1 min to achieve a steady state by releasing the charges initially trapped in the MOS interface and oxide bulk. After the up-and-down ramping of each pulse, all terminals of the DUTs were grounded for 10 s to release the trapped charges to restore their initial state.

According to the schematic, time-dependent drain current $I_{D(t)}$ and drain-to-source resistance $R_{DS(t)}$ could be calculated using the following equations:

$$I_{D(t)} = \frac{V_{DD} - V_{DS(t)}}{R_L} \tag{1}$$

$$R_{DS(t)} = \frac{V_{DS(t)} \cdot R_L}{V_{DD} - V_{DS(t)}} \tag{2}$$

The calculated up (solid line)-/down (dotted line) ramp I_D-V_{GS} and R_{DS}-V_{GS} curves are shown in Fig. 3 (a) and (b). In Fig. 3 (a), The V_{TH} hysteresis (pink-dotted-line) is defined as the gate voltage difference read at the up/down ramps when the drain voltage ($V_{DS(t)}$) is 0.3 V [17]. In Fig. 3 (b), R_{ON} is defined as the value of R_{DS} when V_{GS} = 6 V. ΔR_{ON} is defined as the ratio of R_{ON} on the down-ramp to R_{ON} on the up-ramp [17].

It can be seen from Fig. 4 (a) and (b) that the ramping time $t_{r/f}$ greatly influences the extraction of threshold voltage hysteresis and on-resistance. In Fig. 4 (c), the V_{GS} and on-resistances extracted from the up-ramp shift to the left as the ramp speed becomes faster. Furthermore, it was observed that the V_{GS} and on-resistances extracted by the down-ramp shift towards the right direction as the ramp speed become faster. Fig. 4 (d) shows that the V_{TH} hysteresis and ΔR_{ON} increase with faster ramp speed. Moreover, a strong correlation between threshold voltage and on-resistance can be observed [7].

In the ramp region, the slow ramp speed will change the charge state close to the MOS interface. In this case,

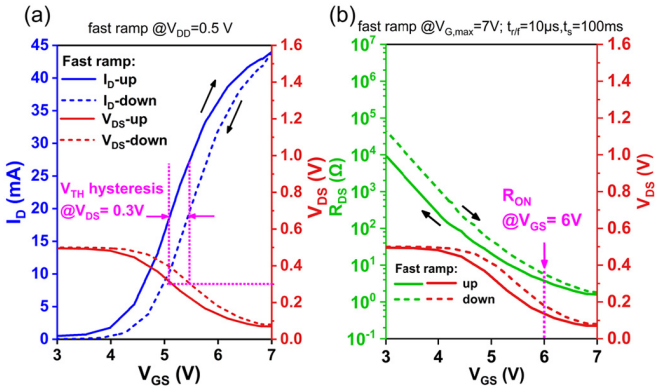

FIGURE 3. (a): calculated I_D-V_{GS} curves at up-/down ramps. The ramp time $t_{r/f}$ is 10 μs. (b): calculated R_{DS}-V_{GS} curves at up-/down ramps.

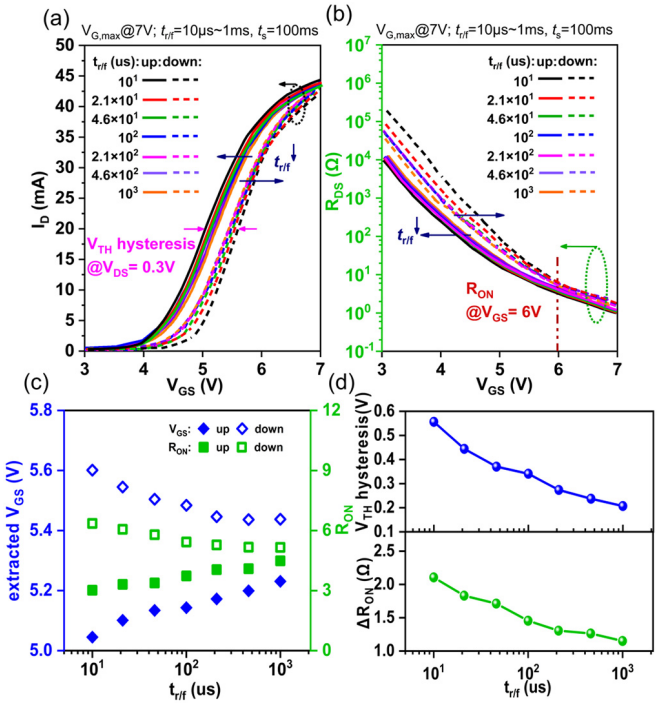

FIGURE 4. (a): I_D-V_{GS} and (b): R_{DS}-V_{GS} curves at different ramping times. (c): V_{GS} and R_{ON} extracted by up-/down-ramp (d): V_{TH} hysteresis and ΔR_{ON} with different ramping times.

the threshold voltage hysteresis is usually underestimated. In other words, faster ramp speed allows for more accurate observation of oxide traps near the interface because less charge state changes during the test [5], [6], [15], [18], and [19].

To achieve acceptable threshold voltage and transconductance, the gate oxide in SiC MOSFETs is usually thinner than its Si counterparts. However, it will lead to more severe degradation in the gate oxide because a higher electric field is applied [4], [18]. The gate stress voltage significantly influences the threshold voltage hysteresis and on-resistance, as shown in Fig. 5. In Fig. 5 (a), the V_{TH} hysteresis is more pronounced at larger stress voltages than at smaller stress

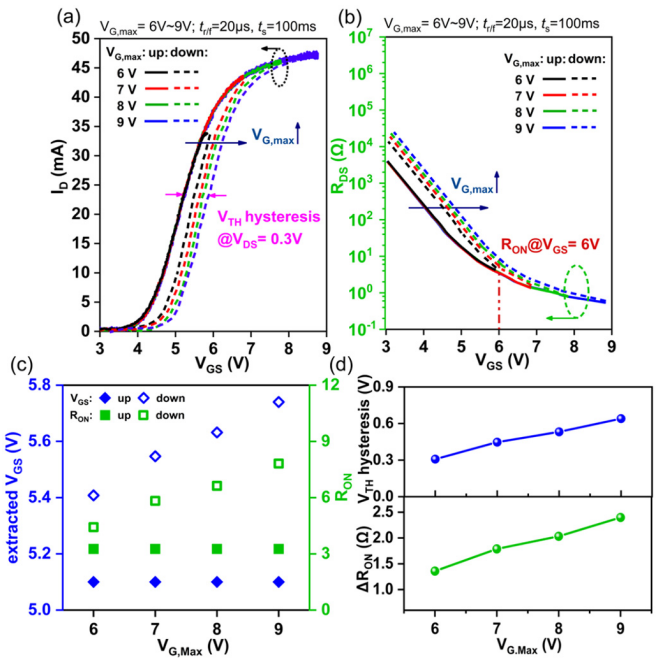

FIGURE 5. (a): I_D-V_{GS} and (b): R_{DS}-V_{GS} curves under different gate stresses. (c): V_{GS} and R_{ON} were extracted by up-/down-ramps under different gate stresses. (d): observed V_{TH} hysteresis and ΔR_{ON} under different gate stresses.

voltages. In Fig. 5 (b), the degeneration of on-resistance is in the same pattern. It is further confirmed in Fig. 5 (c), where extracted V_{GS} and R_{ON} did not change significantly during the up-ramps with increasing gate stress compared with the down-ramps. This is because more oxide defects are filled at higher voltages. Fig. 5 (d) shows the V_{TH} hysteresis and ΔR_{ON} observed under different gate biases using the fast I-V method.

Depending on the results in Fig. 4 and 5, an up-/down-ramp speed of 100 μs and moderate gate stress of 7 V is selected for the following short-term stress test. In Fig. 6, V_{TH} hysteresis, ΔR_{ON}, and maximum transconductance changes ($\Delta G_{m.max}$%) are monitored during the 1 s stress time. The $G_{m.max}$ is defined as the maximum value of $\Delta I_D/\Delta V_{GS}$. The degradation of transconductance $\Delta G_{m.max}$% is defined as the percentage of the $G_{m.max}$ difference read at the up/down ramps divided by the $G_{m.max}$ value of up-ramps.

Fig. 6 (a) and (b) show that V_{TH} hysteresis and R_{ON} degradation increase with stress time. In Fig. 6 (c), the extracted V_{GS}, R_{ON}, and $G_{m,max}$ did not change significantly on the up-ramps but changed greatly with increasing stress time on the down-ramps. Fig. 6 (d) shows that V_{TH} hysteresis and ΔR_{ON} increase linearly with logarithmic time [2], [6], [20], [21], [22], and the transconductance degradation $\Delta G_{m.max}$% also increases with stress time.

Based on the direct tunneling model of charge transfer into MOS devices, it is assumed that the traps are randomly distributed in the oxide. The total charge transferred into the oxide trap follows a logarithmic time dependence [18], [23],

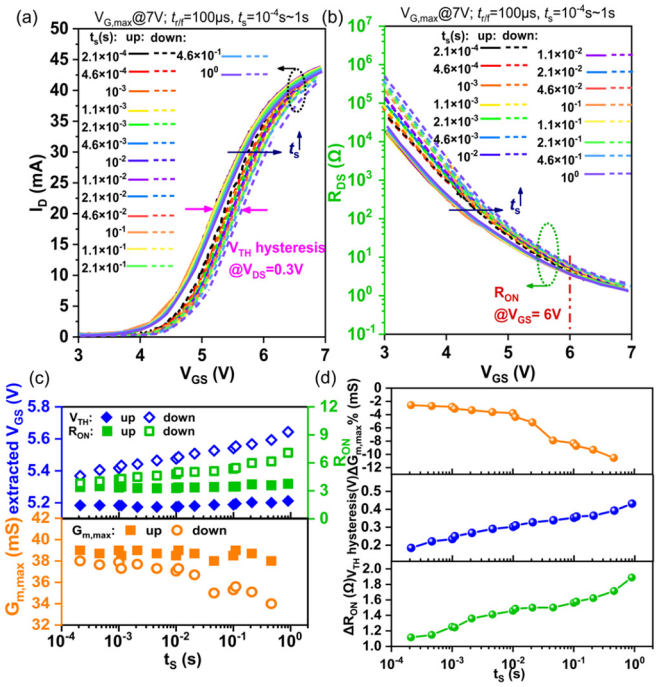

FIGURE 6. (a): I_D-V_{GS} and (b): R_{DS}-V_{GS} curves with increased stress time. (c): $G_{m,max}$, V_{GS}, and R_{ON} extracted by up-/down-ramps with increased stress time. (d): V_{TH} hysteresis, ΔR_{ON}, and $\Delta G_{m,max}$% increased with logarithmic time.

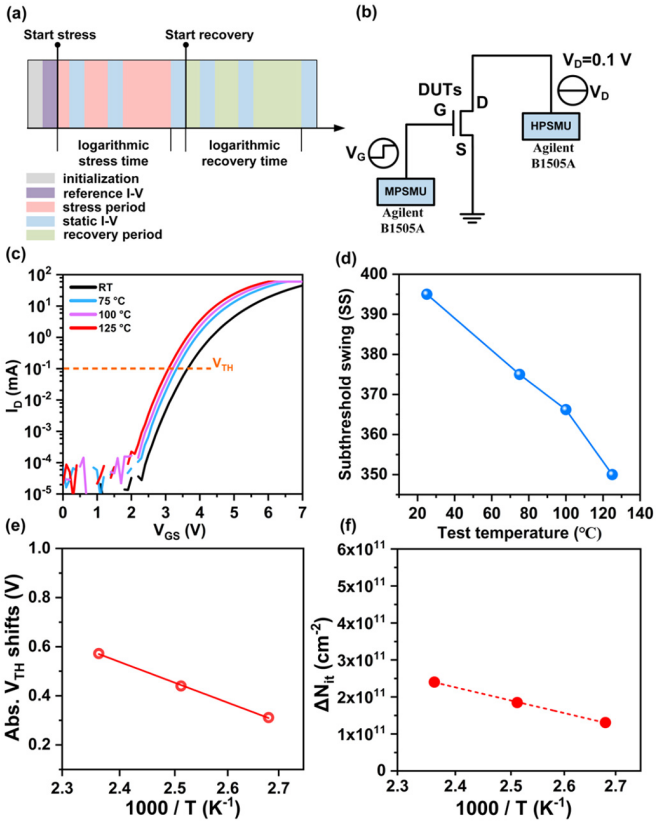

FIGURE 7. (a): measure-stress-measure test procedure. (b): schematic experiment setup for static I-V measurement. (c): transfer characteristics of fresh DUTs at different elevated temperatures. (d): extracted subthreshold swings at different temperatures. (e): V_{TH} shifts in Arrhenius plots at different temperatures. (f): temperature-dependent changes in interface traps per unit area.

as described by the following equation:

$$Q_{NIOT} \cong \frac{eN}{2\beta}\left[In\frac{t}{t_0} + \zeta\right] \tag{3}$$

Where Q_{NIOT} is the charge states in the near-interfacial oxide traps, N is oxide trap density, e is the electronic charge, β is the tunneling parameter, t_0 is the initial tunneling transition time, and ζ is the Euler's constant. It can be seen from the equation that trapped charge states increase linearly concerning the logarithm of stress time, which is consistent with the results shown in Fig. 6 (d).

It is suggested that the V_{TH} hysteresis and ΔR_{ON} are attributed to the direct tunneling of channel electrons into as-grown oxide traps near the interface within 1 s bias time [6], [21]. As shown in Fig. 6 (c) and (d), the decrease in transconductance with stress time is more pronounced since transconductance is related to bulk traps in the oxide layer [24].

It can be predicted that more electrons would be trapped into the deeper oxide defects as stress time increases, causing more significant V_{TH} hysteresis and ΔR_{ON}.

III. STATIC I-V EXPERIMENTAL PROCEDURE AND TEST RESULTS

In the previous section, we discussed the V_{TH} hysteresis and ΔR_{ON} under short-term stress within 1 s; in this section, we will discuss the ΔV_{TH} and ΔR_{ON} under long-term stress within 10^4 s. The static I-V technique uses the measure-stress-measure (MSM) process, as illustrated in Fig. 7 (a). The MSM procedure consists of four steps: initial stabilization, I-V reference curves measurement, multiple stress-sense measurement, and recovery-sense measurement. The schematic experiment setup for static I-V measurement is shown in Fig. 7 (b). Due to the pulse width limitation of the pulse generator in the fast I-V technique, the MPSMU module of Agilent B1505A is used to generate long-term pulse width for stress periods and recovery periods. The maximum current level is limited to 60 mA to protect the parameter analyzer.

At the beginning of the test, four virgin devices were initialized by all terminals being grounded for 1 min. Then the DUTs were heated to elevated temperatures for 1 hour to stabilize the device package temperature. After that, I-V reference curves at elevated environment temperatures were performed with V_{GS} from 0 V to 7 V at V_{DS} = 0.1 V by Agilent B1505A, as displayed in Fig. 7 (c). The V_{TH} is defined as the gate voltage when the drain current reaches 0.1 mA. There are three temperature ranges from room temperature to 75 °C, to 100 °C, to 125 °C. Threshold voltage shifts are defined herein as the difference between the threshold voltage at different temperatures and the room temperature threshold voltage. It can be observed that in

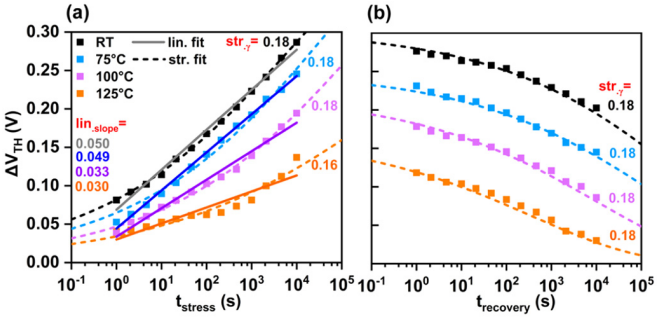

FIGURE 8. Time evolution of ΔV_{TH} measured during (a): stress and (b): recovery at several temperatures. The bias conditions are V_{GS} = 7 V, V_{DS} = 0 V. The data plots are fitted by linear (solid line) and stretched exponential function (dash line).

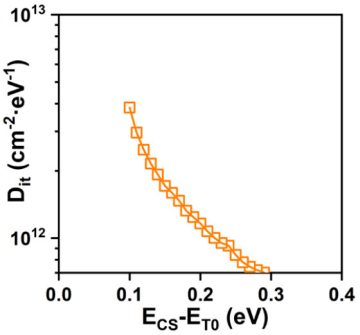

FIGURE 9. Interface trap density of the double-trench device.

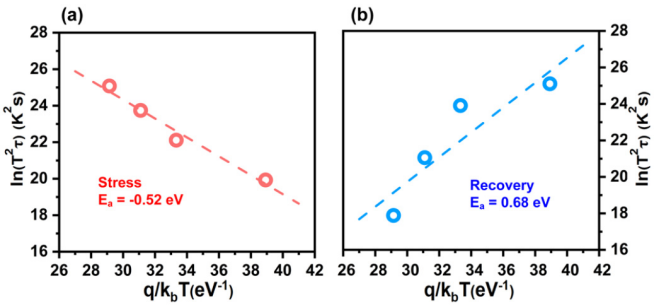

FIGURE 10. Activation energy E_a in the (a): stress phase and (b): recovery phase is obtained by the Arrhenius plot.

Fig. 7 (c) and (e), the V_{TH} shifts increase with higher temperatures consistently with the Arrhenius plot [25], [26]. In Fig. 7 (f), the interface traps per unit area, ΔNit increases from 1.31×10^{11} to 2.41×10^{11} with temperature from 25 °C to 125 °C, which is caused by the massive electron emission from the interface traps [25] and [27]. In Fig. 7 (d), the subthreshold swing decreases at high temperatures due to the alleviated Coulomb scattering effect [3], [26], [28], [29].

In the stress period, 7 V gate bias was applied to the DUTs for 10^4 s with other terminals grounded. The stress process was interrupted at the mean logarithmic time. Transfer characteristic curves were performed in the negative orientation (V_{GS} from 7 V to 0 V at V_{DS} = 0.1 V) to monitor the V_{TH} and R_{ON} [11]. The threshold voltage instability ΔV_{TH} is defined as the difference in V_{TH} before and after stress.

In the recovery period, the gate voltage of 0 V was applied to the DUTs for 10^4 s with other terminals grounded to release electrons that had been trapped in the MOS interface and bulk defects.

To obtain the capture/emission time constant and describe the distribution of defects in the oxide layer, the ΔV_{TH} data in Fig. 8 (a) and (b) are fitted with the stretched exponential functions by using the following Equations (4) and (5), with the high R-square values between 0.95 to 0.99 (dash fitted line) [3], [26], [27].

$$V_{TH\_hys(s)} = V_{TH\_hys(max)}\left[1 - exp\left(\frac{-t_s}{\tau_s}\right)^{\gamma}\right] \quad (4)$$

$$V_{TH\_hys(r)} = V_{TH\_hys(ts,0)}\left[-exp\left(\frac{-t_r}{\tau_r}\right)^{\gamma}\right] \quad (5)$$

$V_{TH\_hys(max)}$ is related to the total trap density, $V_{TH\_hys(ts,0)}$ is the non-recovered V_{TH_hys} value, γ is related to the trap energy distribution, $t_{s/r}$ is stress/recovery time, and τ_s/τ_r is the time constant of stress/recovery periods.

It can be found in Fig. 8 (a) that the time constant τ_s increases from 10^3 to 10^5 as the temperature increases, leading to a negative activation energy of -0.52 eV, extracted in Fig. 10 (a). This may explain why the ΔV_{TH} decreases with the elevated temperature, the same phenomenon observed in [3], [11]. In other words, during the high-temperature stress phase, the de-trapping is even more thermally activated than the trapping, caused by the emission time constant being shorter than their associated capture time [11].

In Fig. 8 (b), after removing the gate bias, we found the de-trapping in the recovery phase is accelerated by high temperatures, with the time constant τ_r dropping from 10^6 s to 10^2 s with increased temperatures, leading to a trap level at 0.68 eV activation energy, extracted by Fig. 10 (b) in the Arrhenius plot.

Moreover, the trap energy distribution shows consistency in the stress and recovery phases, with the parameter γ from 0.16 to 0.18, as shown in Fig. 8 (a) and (b). This indicates that the trap energy distribution is concentrated in the gate oxide [3].

We also found that the ΔV_{TH} increases linearly with logarithmic time (solid fitted line), the same as in Fig. 6 (d). It is suggested that channel electrons are trapped in the oxide defects near the interface [30], [31], [32].

In Fig. 9, the interface trap density D_{it} at room temperature is calculated by I-V subthreshold method [33], [34], [35]. The D_{it} increases exponentially near the conduction band edge. E_{CS} is the potential of the conduction band surface, and E_{t0} is the surface potential related to the trap level. At the $E_{CS} - E_{T0}$ = 0.1 eV, the D_{it} is 3.8×10^{12} cm^{-2}·eV^{-1}.

The time evolution of ΔR_{ON} during the stress and recovery process are shown in Fig. 11 (a) and (b), respectively. It can be found that the ΔR_{ON} decreases with elevated temperature, which is consistent with the ΔV_{TH} tendency in Fig. 8 (a). The ΔR_{ON} also fits well with the stretched

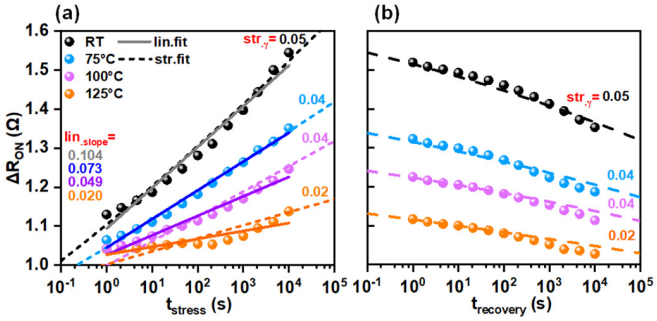

FIGURE 11. Time evolution of ΔR_{ON} was measured during (a): stress and (b): recovery at several temperatures. The data plots are fitted by linear (solid line) and stretched exponential function (dash line).

TABLE 1. Interface trap density of SiC MOSFETs.

Device	Measurement method	Interface trap density Dit ($cm^{-2}{\cdot}eV^{-1}$)	Ref.
Planar	I-V subthreshold characteristics	5.8×10^{12}	[34]
		6.8×10^{12}	
		9.3×10^{12}	
Unknown		about 2×10^{13}	[33]
Unknown		5.4×10^{12}	[35]
Planar	C-V high-frequency characteristics	about 2.5×10^{12}	[36]
		About 10^{13}	[37]
		About 5×10^{11}	[38]
Double trench	I-V subthreshold characteristics	3.8×10^{12}	This work

TABLE 2. Trap level of commercial SiC MOSFETs.

Device	Methods	Bias (V)	T_S(s)	T_R (s)	Trap level (eV)	Ref.
Planar	AC stress (10 kHz)	25	10^{-4}-10^{6}	_____	1.2 (stress)	[8]
Planar	Cyclic gate bias	30	2×10^{0}	_____	0.1 (stress)	[39]
Unk.	DC stress	15-20	10^{1} -10^{5}	_____	1.04~1.14 (stress)	[6]
Unk.	Double ramp	15	5×10^{-6}	10^{-5}-10^{0}	0.3 (recovery)	[40]
Double-trench	DC stress	7	10^{0}-10^{4}	10^{0}-10^{4}	0.68 (recovery)	This work

exponential function, with the parameter γ from 0.02 to 0.05 during both the stress and recovery phases.

IV. CONCLUSION

This work uses fast I-V and static I-V techniques to explore the oxide trapping mechanism under positive gate bias in the double-trench SiC MOSFETs.

By monitoring V_{TH} hysteresis and ΔR_{ON} within 1 s stress time using the fast I-V technique, it was found that these two parameters are affected by ramp speed, bias voltage, and stress time. By monitoring the ΔV_{TH} and ΔR_{ON} within 10^4 stress time using the static I-V technique, it was found that the ΔV_{TH} and ΔR_{ON} decreased with the elevated temperature due to the activated de-trapping effect. Moreover, during the 10^4 recovery time, the trap level at 0.68 eV below the conduction band is obtained, and these recoverable trap sites are concentrated in the oxide layer.

Although the observation method is different, it can be found that the instability of the threshold voltage and on-resistance increases linearly with logarithmic time regardless of the long or short stress time, indicating that direct tunneling dominates the electrons trapping in oxide near the interface. The interface trap density is 3.8×10^{12} $cm^{-2}{\cdot}eV^{-1}$.

Comparisons of D_{it} and E_a between the SiC MOSFETs with different structures are shown in Tables 1 and 2, respectively.

REFERENCES

[1] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, 2015, Art. no. 040103, doi: 10.7567/JJAP.54.040103.
[2] A. Lelis, R. Green, and D. Habersat, "(Invited) effect of threshold-voltage instability on SiC power MOSFET high-temperature reliability," *ECS Trans.*, vol. 41, no. 8, p. 203, 2011, doi: 10.1149/1.3631498.
[3] T. Okunishi et al., "Reliability study on positive bias temperature instability in SiC MOSFETs by fast drain current measurement," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, 2017, Art. no. 4CR01, doi: 10.7567/JJAP.56.04CR01.
[4] B. J. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," *Procedia CIRP*, vol. 59, pp. 280–285, Dec. 2017.
[5] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias temperature instability in commercially-available SiC MOSFETs," *Jpn. J. Appl. Phys.*, vol. 55, no. 4S, 2016, Art. no. 4EA03, doi: 10.7567/JJAP.55.04EA03.
[6] A. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015, doi: 10.1109/TED.2014.2356172.
[7] J. O. Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectron. Rel.*, vols. 88–90, pp. 557–562, Sep. 2018, doi: 10.1016/j.microrel.2018.06.045.
[8] D. B. Habersat, R. Green, and A. J. Lelis, "Temperature-dependent threshold stability of COTS SiC MOSFETs during gate switching," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. WB-4.1-WB-4.4, doi: 10.1109/IRPS.2017.7936413.
[9] D. P. Hamilton et al., "High-temperature electrical and thermal aging performance and application considerations for SiC power DMOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7967–7979, Oct. 2017, doi: 10.1109/TPEL.2016.2636743.
[10] A. Marzoughi, R. Burgos, and D. Boroyevich, "Characterization and comparison of latest generation 900-V and 1.2-kV SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–8.
[11] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Understanding BTI in SiC MOSFETs and its impact on circuit operation," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 144–153, Jun. 2018, doi: 10.1109/TDMR.2018.2813063.
[12] B. Asllani, A. Fayyaz, A. Castellazzi, H. Morel, and D. Planson, "Vth subthreshold hysteresis technology and temperature dependence in commercial 4H-SiC MOSFETs," *Microelectron. Rel.*, vol. 88, pp. 604–609, Jun. 2018, doi: 10.1016/j.microrel.2018.06.047.
[13] G. Consentino, E. Guevara, L. Sanchez, F. Crupi, S. Reggiani, and G. Meneghesso, "Threshold voltage instability in SiC power MOSFETs," in *Proc. PCIM Europe Int. Exhibit. Conf. Power Electron. Intell. Motion Renew. Energy Energy Manag.*, 2019, pp. 1–4.
[14] K. Okumura, N. Hase, K. Ino, T. Nakamura, and M. Tanimura, "Ultra low Ron SiC trench devices," ROHM Corp., Kyoto, Japan, Rep., 2012. [Online]. Available: https://www.rohm.com/documents/11405/851226/120517.pdf

[15] M. Gurfinkel et al., "Characterization of transient gate oxide trapping in SiC MOSFETs using fast I-V techniques," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2004–2012, Aug. 2008, doi: 10.1109/TED.2008.926626.

[16] S. Yang, Y. Lu, H. Wang, S. Liu, C. Liu, and K. J. Chen, "Dynamic gate stress-induced V_{TH} shift and its impact on dynamic RON in GaN MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 157–160, Feb. 2016, doi: 10.1109/LED.2015.2505334.

[17] S. Yang, Y. Lu, S. Liu, H. Wang, C. Liu, and K. J. Chen,, "Impact of Vth shift on Ron in E/D-mode GaN-on-Si power transistors: Role of dynamic stress and gate overdrive," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2016, pp. 263–266, doi: 10.1109/ISPSD.2016.7520828.

[18] U. Karki, N. S. Gonzlez-Santini, and F. Z. Peng, "Effect of gate-oxide degradation on electrical parameters of silicon carbide MOSFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2544–2552, Jun. 2020, doi: 10.1109/TED.2020.2990128.

[19] E. Guevara, V. Herrera-Prez, C. Rocha, and K. Guerrero, "Threshold voltage degradation for n-Channel 4H-SiC power MOSFETs," *J. Low Power Electron. Appl.*, vol. 10, no. 1, p. 3, Jan. 2020, doi: 10.3390/jlpea10010003.

[20] A. J. Lelis et al., "Time dependence of bias-stress-induced SiC MOSFET threshold-voltage instability measurements," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1835–1840, Aug. 2008, doi: 10.1109/TED.2008.926672.

[21] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET threshold-stability issues," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 32–37, May 2018. [Online]. Available: https://doi.org/10.1016/j.mssp.2017.11.028.

[22] A. J. Lelis, T. R. Oldham, H. E. Boesch, and F. B. McLean, "The nature of the trapped hole annealing process," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 1808–1815, Dec. 1989, doi: 10.1109/23.45373.

[23] F. B. Mclean, "A direct tunneling model of charge transfer at the insulator-semiconductor interface in MIS devices," Harry Diamond Labs, Adelphi, MD, USA, Tech. Rep. HDL-TR-176, 1976.

[24] S. J. Rhee et al., "Dynamic positive bias temperature instability characteristics of ultra-thin HfO2 NMOSFET," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2004, pp. 269–272, doi: 10.1109/RELPHY.2004.1315336.

[25] N. Tega, S. Sato, and A. Shima, "Comparison of extremely high-temperature characteristics of planar and three-dimensional SiC MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1382–1384, Sep. 2019, doi: 10.1109/LED.2019.2930712.

[26] S. Potbhare, N. Goldsman, A. Lelis, J. M. McGarrity, F. B. McLean, and D. Habersat, "A physical model of high temperature 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2029–2040, Aug. 2008.

[27] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York, NY, USA: Cambridge Univ. Press, 1998.

[28] L. Yang et al., "Analysis of mobility for 4H-SiC N/P-channel MOSFETs up to 300 °C," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 3936–3941, Aug. 2021, doi: 10.1109/TED.2021.3084908.

[29] S. Yu et al., "Bias-induced threshold voltage instability and interface trap density extraction of 4H-SiC MOSFETs," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 420–424, doi: 10.1109/WiPDA46397.2019.8998931.

[30] L. S'anchez, E. Acurio, F. Crupi, S. Reggiani, and G. Meneghesso, "BTI saturation and universal relaxation in SiC power MOSFETs," *Microelectron. Rel.*, vol. 109, Jun. 2020, Art. no. 113642, doi: 10.1016/j.microrel.2020.113642.

[31] E. Acurio, F. Crupi, P. Magnone, L. Trojman, and F. Iucolano, "Impact of AlN layer sandwiched between the GaN and the Al2O3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs," *Microelectron. Eng.*, vol. 178, pp. 42–47, Jun. 2017, doi: 10.1016/j.mee.2017.04.044.

[32] M. Meneghini et al., "Negative bias-induced threshold voltage instability in GaN-on-Si power HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 474–477, Apr. 2016, doi: 10.1109/LED.2016.2530693.

[33] Y. Zheng, A. Softic, and M. H. White, "Characterization of interface traps in subthreshold regions of implanted 6H- and 4H-SiC MOSFETs," in *Proc. Int. Semicond. Device Res. Symp.*, 2001, pp. 213–215, doi: 10.1109/ISDRS.2001.984478.

[34] S. Yu, M. H. White, and A. K. Agarwal, "Experimental determination of interface trap density and fixed positive oxide charge in commercial 4H-SiC power MOSFETs," *IEEE Access*, vol. 9, pp. 149118–149124, 2021, doi: 10.1109/ACCESS.2021.3124706.

[35] H. Yoshioka and K. Hirata, "Characterization of SiO_2/SiC interface states and channel mobility from MOSFET characteristics including variable-range hopping at cryogenic temperature," *AIP Adv.*, vol. 8, Apr. 2018, Art. no. 45217. [Online]. Available: https://doi.org/10.1063/1.5027695

[36] D. Okamoto, M. Sometani, S. Harada, R. Kosugi, Y. Yonezawa, and H. Yano, "Improved channel mobility in 4H-SiC MOSFETs by boron passivation," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1176–1178, Dec. 2014, doi: 10.1109/LED.2014.2362768.

[37] J. Rozen, A. C. Ahyi, X. Zhu, J. R. Williams, and L. C. Feldman, "Scaling between channel mobility and interface state density in SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3808–3811, Nov. 2011, doi: 10.1109/TED.2011.2164800.

[38] Y. K. Sharma et al., "High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 175–177, Feb. 2013, doi: 10.1109/LED.2012.2232900.

[39] P. Fiorenza, F. Giannazzo, S. Cascino, M. Saggio, and F. Roccaforte, "Identification of two trapping mechanisms responsible of the threshold voltage variation in SiO2/4H-SiC MOSFETs," *Appl. Phys. Lett.*, vol.117, no. 10, Sep. 2020, Art. no. 103502, doi: 10.1063/5.0012399.

[40] M. Cioni et al., "Identification of Interface States responsible for VTH Hysteresis in packaged SiC MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2022, pp. 5B.3–1-5B.3–6, doi: 10.1109/IRPS48227.2022.9764543.

[41] "Narrow-band analyzer," Ph.D. dissertation, Dept. Elect. Eng., Harvard Univ., Cambridge, MA, USA, 1993.