Received 29 August 2022; accepted 3 October 2022. Date of publication 6 October 2022; date of current version 19 October 2022.
The review of this article was arranged by Editor M. T. A. Rahimo.

Digital Object Identifier 10.1109/JEDS.2022.3212368

β-Ga_2O_3 Field Plate Schottky Barrier Diode With Superb Reverse Recovery for High-Efficiency DC–DC Converter

WEI GUO [1] (Student Member, IEEE), GUANGZHONG JIAN [2], WEIBING HAO [1] (Student Member, IEEE), FEIHONG WU [1] (Student Member, IEEE), KAI ZHOU [1] (Student Member, IEEE), JIAHONG DU [1], XUANZE ZHOU [1] (Student Member, IEEE), QIMING HE [1], ZHAOAN YU [2], XIAOLONG ZHAO [1], GUANGWEI XU [1] (Member, IEEE), AND SHIBING LONG [1] (Senior Member, IEEE)

1 School of Microelectronics, University of Science and Technology of China, Hefei 230026, China
2 Key Laboratory of Microelectronics Devices and Integration Technology, Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China

CORRESPONDING AUTHORS: G. XU and S. LONG (e-mail: xugw@ustc.edu.cn; shibinglong@ustc.edu.cnn)

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant 61925110, Grant 61821091, Grant 62004184, Grant 62004186, and Grant 51961145110; in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2020B010174002; in part by the Opening Project of Key Laboratory of Microelectronics Devices and Integration Technology in Institute of Microelectronics of CAS; in part by the Key Laboratory of Nanodevices and Applications in Suzhou Institute of Nano-Tech and Nano-Bionics of CAS; and in part by the Center for Micro and Nanoscale Research and Fabrication of University of Science and Technology of China (USTC).

(Wei Guo and Guangzhong Jian contributed equally to this work.)

ABSTRACT β-Ga_2O_3 Schottky barrier diodes with field plate (FP-SBDs) are fabricated and their SPICE-compatible model are constructed for double-pulse test circuit and DC-DC boost converter simulations. The reverse recovery time (t_{rr}) of the β-Ga_2O_3 SBD is 8.8 ns and its reverse recovery charge (Q_{rr}) is 8.33 nC when switching from a forward current of 1 A to a reverse bias voltage of 100 V with a di/dt of 400 A/μs, which is analogous with the prediction of our model. Device with the radius of 500 μm was fabricated, a current of 2 A can be obtained at the forward voltage of 2 V, meanwhile, the breakdown voltage is 467 V. The Ga_2O_3-based converter module after device packaging with TO-220 reveals a comparative efficiency to that of the SiC-based converter under multiple conditions, and reached up to 95.62% at the input voltage of 200 V. The decent performance of Ga_2O_3 FP-SBD and its DC-DC converter indicates great potential in power application.

INDEX TERMS β-Ga_2O_3, Schottky barrier diode, SPICE-compatible model, double-pulse test circuit, DC-DC converter.

I. INTRODUCTION

Power devices and circuits are the parts that control electrical energy conversion. In order to reduce the power consumption of electrical equipment, it is necessary to reduce the energy conversion loss on power devices. Developing power devices and circuits based on novel ultra-wide bandgap semiconductors can contribute to combating global warming due to a reduction in CO_2 emissions [1].

β-Ga_2O_3 has great potential in power electronic applications due to its large bandgap of approximately 4.8 eV, high critical electric field of 8 MV/cm and Baliga's figure of merit of 3444 [2], [3], [4], which is superior to SiC and GaN significantly. Its effective wide N-type doping range of 10^{16} to 10^{19} cm^{-3} and low-cost substrate growth method have enabled β-Ga_2O_3 to become a promising candidate for the next generation power semiconductors [5], [6], [7], [8], [9], [10].

Numerous studies have focused on β-Ga_2O_3 Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], whose performances have been improved significantly and currently approach those of SiC and GaN power devices [21], [22], [23], [24]. Various techniques have been proposed to further optimize the on-resistance and breakdown voltage of devices, such as field-ring, field-plate, and SU-8 passivation [25], [26], [27].

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

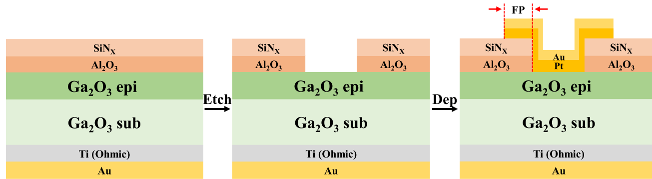

FIGURE 1. Fabrication process flow of the vertical Ga_2O_3 Schottky barrier diode with field-plate (FP-SBD) structure.

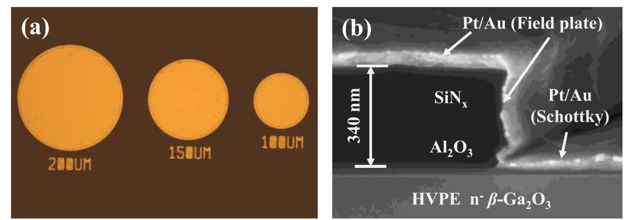

FIGURE 2. (a) Optical top view image of Ga_2O_3 FP-SBDs with different radiuses. (b) Cross-sectional scanning electron microscopy (SEM) image of FP-SBD focusing on the etching dielectric sidewall.

Meanwhile, the performance of Ga_2O_3 SBD is outstanding compared to MOSFET up till now, thus Ga_2O_3 SBD is more mature for circuit application.

Functional circuits based on β-Ga_2O_3 devices are scarce so far. β-Ga_2O_3 SBD was used in rectification circuit to test the rectification characteristics at high frequency [28]. Moreover, β-Ga_2O_3 FETs were used in a boost converter to compare their performance [29]. DC-DC boost converter can be applied to enhance the output voltage for functional circuits and utilized in fields of power transformation, such as home electronics, industrial control and new energy [30], [31], [32], [33], [34]. A converter circuit usually contains SBD and MOSFET, and the whole power efficiency relies on the static and dynamic performance of these devices [35], [36], [37]. Acceptable off-state and reverse recovery characteristics of SBD guarantee stable output waveforms and less overall power loss [38], meanwhile, a WBG (SiC, GaN and Ga_2O_3) SBD has better reverse recovery characteristics due to its unipolar device structure compared to a Si device [39]. However, there is still no study on Ga_2O_3 SBD in DC-DC converters, so the application potential of Ga_2O_3 SBD needs to be further demonstrated.

This work contains a complete process from device to circuit including device fabrication, compact model, SPICE simulation, device package and circuit modularization based on Ga_2O_3 SBD with field plate (FP-SBD). Sections II and III describe the fabrication process and performance of the Ga_2O_3 FP-SBD. The SPICE model for Ga_2O_3 FP-SBD is illustrated in Section IV and the agreement of the simulation result and experiment proves the validity. A double pulse test (DPT) circuit is used to evaluate the switching performance of Ga_2O_3 FP-SBD in Section V, and the simulation results and experimental results are almost consistent. Section VI details the simulation results and physical performance of a DC-DC boost converter utilizing packaged devices. The main conclusions are derived in Section VII.

II. DEVICE FABRICATION

The fabrication process flow of the vertical Ga_2O_3 FP-SBD is shown in Fig. 1. The 610-μm-thick Ga_2O_3 substrate is Sn-doped with a concentration of 7.0×10^{18} cm^{-3} grown by edge-defined film-fed growth (EFG). The 7.6-μm-thick Ga_2O_3 epitaxial layer grown by halide vapor phase epitaxy (HVPE) has a low doping concentration of approximately 1.7×10^{16} cm^{-3}. After organic and acid cleaning, the backside of the Ga_2O_3 substrate is coated with Ti (20 nm)/Au (100 nm) metal stack through e-beam evaporation. Then the Ga_2O_3 substrate undergoes rapid thermal annealing at 470 °C for 1 min in N_2 atmosphere to improve the quality of ohmic contact.

Bilayer Al_2O_3 and SiN_x, which have thicknesses of 20 nm and 320 nm respectively, are deposited in order on the front side. This combination guarantees a high-quality interface between the dielectric and β-Ga_2O_3, while the growth method is economical. The Al_2O_3 is grown by atomic layer deposition (ALD) with trimethylaluminum and H_2O as the precursor. Then top-layer SiN_x with dichlorosilane and NH_3 as the precursor is deposited by plasma-enhanced chemical vapor deposition (PECVD). Wet etching is applied to form metal contact holes with buffered oxide etchant (BOE). The Schottky electrode with a composite of Pt (20 nm) and Au (100 nm) on the front side is formed by a single lithography, magnetron sputtering, and lift-off process. The Schottky electrode extends over the dielectric to act as the field plate (FP), with its length set to be 20 μm. The radiuses of the Schottky contact are designed to be 100, 150, and 200 μm.

Fig. 2(a) shows the optical top view images of FP-SBDs with different radiuses. The raised edge of Schottky contact is just the field plate, and all these lengths are uniformed. Fig. 2(b) is the cross-sectional scanning electron microscopy image of the fabricated FP-SBD. The sidewall of the double-layered dielectric after wet etching is almost vertical.

III. DEVICE PERFORMANCE

The forward conduction characteristics of Ga_2O_3 FP-SBDs with radiuses of 100, 150, and 200 μm are illustrated in Fig. 3. The knee voltage of all devices is 0.8 V in common. The inset of Fig. 3(a) compares the specific on-resistance of different devices, which are 6.45, 8.19 and 10.40 m$\Omega\cdot$cm^2, respectively. The result reveals that the FP-SBD with a smaller radius has lower specific on-resistance. The current flowing from the anode into the β-Ga_2O_3 substrate will have horizontal diffusion current [1]. The linear fitting of the semi-log plot of current density versus voltage in Fig. 3(b) gives the ideality factor of 1.04 and Schottky barrier height of 1.16 eV, which indicates that the forward electron transport is close to the ideal thermionic emission model [40]. The on-off current ratio up to 10^8 is achieved with favorable rectification capability. For all tested devices with different radiuses, the Schottky contact properties are

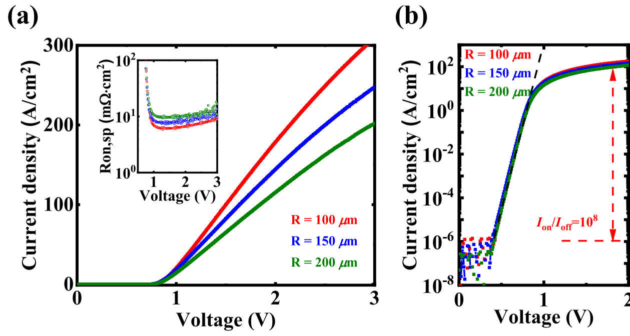

FIGURE 3. Forward conduction characteristics of Ga_2O_3 FP-SBDs with radiuses of 100, 150, and 200 μm. (a) Linear scale plot. The inset shows specific on-resistance of different devices. (b) Semi-log plot and the linear fitting.

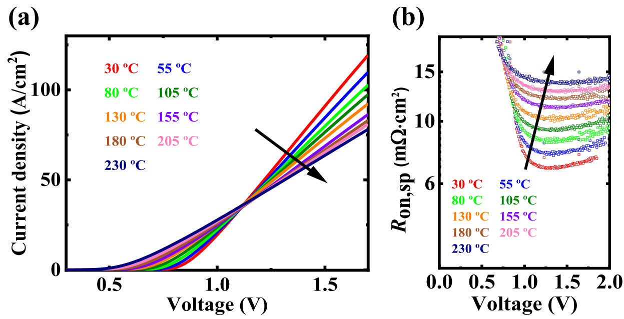

FIGURE 4. Forward conduction characteristics of Ga_2O_3 FP-SBD (radius = 150 μm) with increasing temperatures (along the arrow's direction). (a) Linear scale plot. (b) The specific on-resistance of device at different temperatures.

ideal and uniform as depicted in Fig. 3(b), which shows similar ideality factor and barrier height.

The forward conduction characteristics of FP-SBD (radius = 150 μm) with increasing temperature are shown in Fig. 4(a). The increasing on-state voltages of FP-SBD at a current density of 100 A/cm^2 under increasing temperatures indicate a positive correlation temperature characteristic. Fig. 4(b) also demonstrates a positive temperature coefficient of the specific on-resistance, which can be utilized to parallel different devices to conduct a large current and ensure the uniformity of the current between different devices [41]. Additionally, the knee voltages of devices at increasing temperatures decrease and induce the intersection of different on-state curves at different temperatures.

The capacitance-voltage curves of FP-SBDs with radiuses of 100, 150, and 200 μm are presented in Fig. 5(a). Fig. 5(b) provides a doping concentration of 1.7×10^{16} cm^{-3} in the epitaxy layer, which accounts for the slightly large on-resistance of Ga_2O_3 FP-SBDs.

The field plate structure has weakly impact on the forward conduction characteristics of the Ga_2O_3 SBD, which can be verified by Fig. 6(a). The on-resistance and forward conduction current are nearly the same for the SBDs with and without FP. The breakdown voltage of a Ga_2O_3 SBD without field plate is 215 V for radius of 100 μm. In contrast, the breakdown voltages of Ga_2O_3 FP-SBD exceed

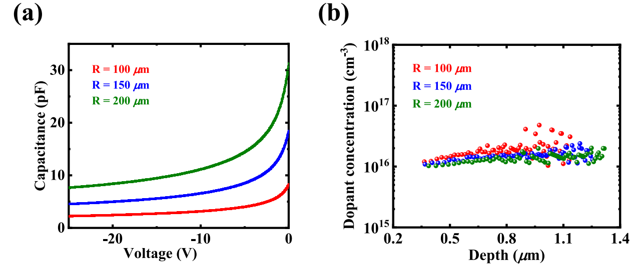

FIGURE 5. (a) Capacitance-voltage characteristics of Ga_2O_3 FP-SBDs with radiuses of 100, 150, and 200 μm. (b) Doping concentration vs depth of Ga_2O_3 FP-SBDs with radiuses of 100, 150, and 200 μm.

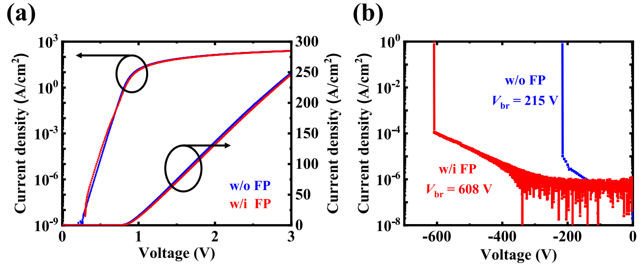

FIGURE 6. (a) Forward conduction characteristics of SBDs with and without field-plate (radius = 100 μm). (b) Reverse blocking properties of the devices.

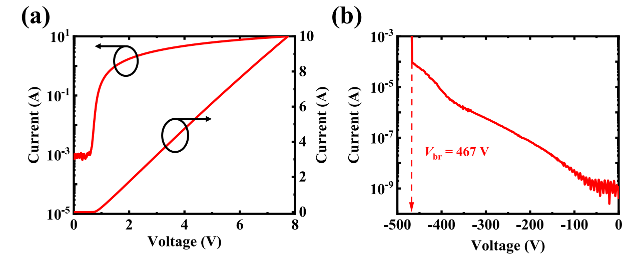

FIGURE 7. (a) Forward conduction characteristics of large area SBD with the radius of 500 μm. (b) Reverse blocking properties of the device.

600 V as shown in Fig. 6(b). The termination of field plate mitigates the electric field crowding at the contact edge and effectively enhances the breakdown voltage. Even so, the performance of the device is underutilized, and better termination structures such as ion implantation, junction termination extension, etc. need to be developed in the future.

In order to satisfy the needs of large current in DC-DC converter, large-area device with the radius of 500 μm was also fabricated. The forward conduction characteristics and reverse blocking properties of the device are shown in Fig. 7, a current of 2 A can be obtained at the forward voltage of 2 V (50-μs pulse width and 1% duty cycle), meanwhile, the breakdown voltage is 467 V, which is relatively superior to other large-area SBDs as shown in Fig. 8 [13], [42], [43], [44], and can be utilized to provide sufficient safety area for the implementation of 350 V-output circuit.

IV. DEVICE MODELING

The device model plays a very important role in simulation, and it can also provide guidance for applications. In this

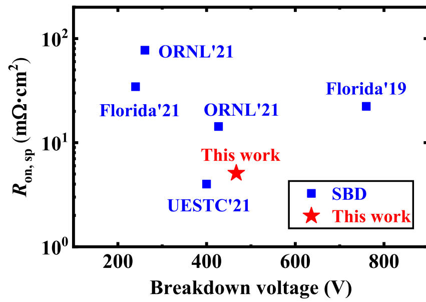

FIGURE 8. R on,sp versus breakdown voltage benchmarking of our fabricated β-Ga_2O_3 SBD with the reported large-area β-Ga_2O_3 SBDs with electrode area above 0.2mm^2.

TABLE 1. SPICE model parameters of Ga_2O_3 SBD.

Parameters	Values	Parameters	Values
C_{j0} (F)	3.5127×10^{-10}	n	1.8860
V_j (V)	0.9	R_S (Ω)	0.6497
M	0.5816	I_S (A)	3.3598×10^{-9}

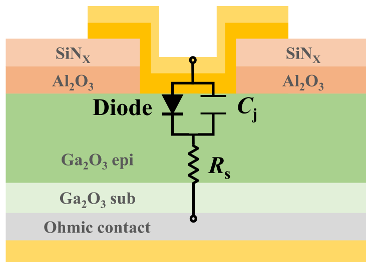

FIGURE 9. Equivalent circuit of Ga_2O_3 SBD.

work, a SPICE model for Ga_2O_3 SBD is constructed from the experimental results with the *I-V* model of

$$I = I_S exp\left[\frac{q(V - IR_S)}{nkT}\right], \quad (1)$$

and the *C-V* model of

$$C = \frac{C_{j0}}{(1 - V/V_j)^M}, \quad (2)$$

where Is is the reverse saturation current, q is the elementary charge, V is the forward voltage, n is the ideality factor, k is the Boltzmann factor, and T is the absolute temperature. C_{j0} is the depletion capacitance at $V = 0$, V_j is the zero-bias build-in potential, and M is the fitting parameter considering the non-ideal effect [45].

Fig. 9 shows the equivalent circuit of the Ga_2O_3 SBD, which contains a diode, a junction capacitance (C_j) in parallel, and a series resistance (R_s) [46], [47], [48]. The diode dominates an exponential growth in the curves of forward current density versus voltage under low voltage, while the resistance dominates the linear growth region at high voltage, as depicted in Fig. 3. The junction capacitance has an effect on the reverse recovery characteristics of the SBD and is frequency dependent.

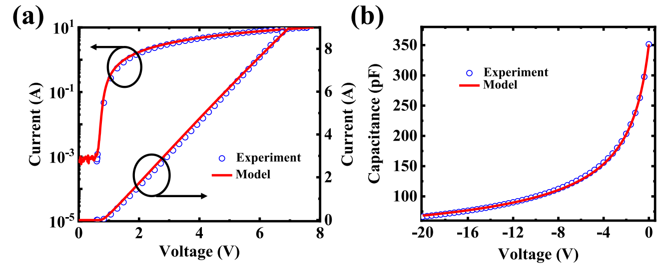

FIGURE 10. Comparison of the (a) *I–V* and (b) *C-V* curves between the experimental and model calculation results.

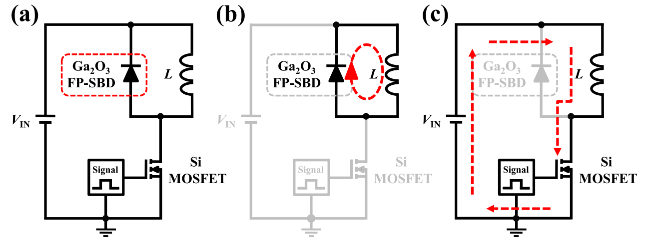

FIGURE 11. (a) Schematic of double-pulse test circuit. (b) Off-state of MOSFET during the switching process. (c) On-state of MOSFET during the switching process.

The Ga_2O_3 SBD used in modeling has a radius of 500 μm, and its corresponding parameters extracted from the experimental results are contained in Table 1. Since the breakdown voltage and the reverse current under breakdown have little effect on the power loss and voltage conversion ratio in our simulation, these parameters are not taken into consideration in device modeling. The simulated forward conduction characteristics and capacitance-voltage characteristics based on this model are consistent with experimental results as depicted in Fig. 10, which proves the validity of our SPICE model. However, the SPICE model is still in its infancy, and more problems such as thermal issues still need to be addressed in the next stage.

V. SWITCHING PERFORMANCE OF DEVICE

A double-pulse test (DPT) circuit was designed to evaluate the switching performance of Ga_2O_3 SBD [39], [49], [50], [51], [52]. The schematic of DPT circuit and its switching process are shown in Fig. 11. The test circuit mainly contains a Si power MOSFET (Infineon, IPD60R360P7ATMA1, 600 V/9 A), a 560 μH inductor for continuous current modulation and our Ga_2O_3 SBD. During the switching process, when the MOSFET is off-state, the current flows from the inductor to the Ga_2O_3 SBD, and the Ga_2O_3 SBD is in forward conduction as shown in Fig. 11(b); when the MOSFET switches from the off-state to the on-state, the inductor is charged by the input power supply, the Ga_2O_3 SBD switches from the on-state to the off-state, and a reverse recovery current occurs during the removal of the charges in the SBD as shown in Fig. 11(c), which is closely

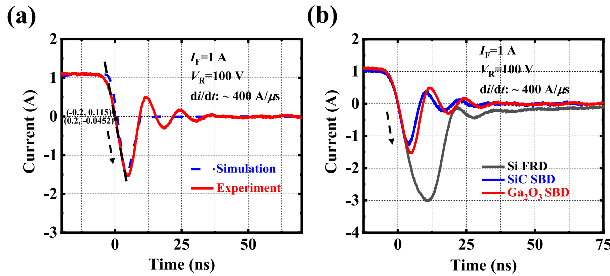

FIGURE 12. (a) Comparison of the reverse recovery properties between the experimental and simulation results with the Ga_2O_3 SBD. (b) The reverse recovery properties of Si FRD, SiC SBD and Ga_2O_3 SBD.

TABLE 2. Parameters of reverse recovery characteristics.

Parameters	Si FRD (STTH1L06)	SiC SBD (CSD01060A)	Ga_2O_3 SBD
I_{rr} (A)	3.01	1.28	1.53
t_{rr} (ns)	20.0	7.8	8.8
Q_{rr} (nC)	37.99	5.93	8.33
R_{on}*Q_{rr} (Ω*nC)	—	2.25	5.41

related to the parasitic capacitance. Through proper selection of the inductor parameter, its current can remain stable with extremely low fluctuations and switches between the MOSFET and SBD.

The reverse recovery characteristic of Ga_2O_3 SBD with the radius of 500 μm was measured when the device switched from a forward current of 1 A to a reverse bias voltage of 100 V with a di/dt of 400 A/μs. Comparison of the reverse recovery properties between the experimental and simulation results with the Ga_2O_3 SBD is shown in Fig. 12(a), the simulation results using our SPICE model are almost consistent with the experimental results. The reverse recovery properties of the Si FRD (Fast Recovery Diode), SiC SBD and Ga_2O_3 SBD are contrasted in Fig. 12(b), and the parameters of the reverse recovery characteristics are shown in Table 2. The on-resistance (R_{on}) of the SiC SBD and Ga_2O_3 SBD are 0.38 Ω and 0.65 Ω, respectively, as for the SiC SBD, the forward voltage is 1.6 V, the total capacitance is 8.5 pF (V_R = 400 V, T_j = 25 °C, f = 1 MHZ). The reverse recovery time (t_{rr}) is defined as the time required to recover to 10% of the peak reverse recovery current (I_{rr}). Experimental results reveal that the reverse recovery characteristic of Ga_2O_3 SBD has an apparent advantage over Si FRD and approaches to SiC SBD.

VI. DC-DC BOOST CONVERTER

The Ga_2O_3 SBD with the radius of 500 μm is implemented into a DC-DC boost converter circuit, which is a step-up design with the output voltage higher than the input voltage, and the circuit configuration of the converter is shown in Fig. 13. The assessed specifications of the converter are summarized in Table 3. In comparison with the Ga_2O_3 SBD, 600 V/1 A SiC SBD (CREE, CSD01060A)

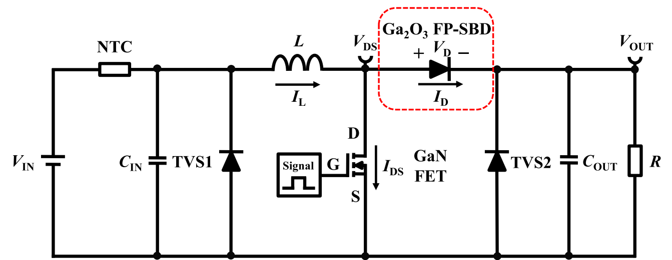

FIGURE 13. Configuration of DC-DC boost converter circuit based on Ga_2O_3 FP-SBD or SiC SBD with NTC and TVS protection.

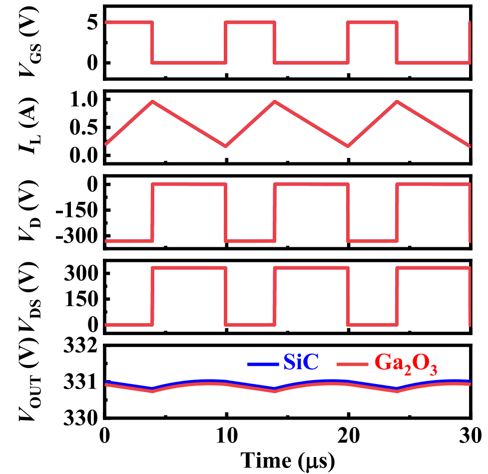

FIGURE 14. Simulation waveforms of the Ga_2O_3- and SiC-based converter for comparison.

and 600 V/1 A Si FRD (ST, STTH1L06) are selected for the proposed DC-DC boost converter. The overall performance is compared between Ga_2O_3-, SiC- and Si-based converters to illustrate the effect of the device on circuit performance.

A 650 V/180 mΩ discrete GaN FET with the part number of TPH3206PSB from Transphorm is used for switching control, and the gate voltage signal (V_{GS}) for the GaN FET is +5 V during the on-state and 0 V during the off-state. The inductor (L) is used to store and provide energy and the magnitude of the current is controlled by the resistance (R). The input voltage (V_{IN}) is selected to be 200 V and the converter is operated at a switching frequency of 100 kHz. Negative temperature coefficient thermistor (NTC) and transient voltage suppression diode (TVS) are implemented in the circuit to provide overcurrent and overvoltage protection. The output capacitance (C_{OUT}) ensures the stability of the output voltage (V_{OUT}). The MOSFET and SBD are turned on alternately to provide stable output.

Fig. 14 shows the comparison of simulation results for the DC-DC boost converters between Ga_2O_3- and SiC-based circuits. The two converters have comparative values including the inductor current (I_L), the diode voltage (V_D) and the MOSFET voltage (V_{DS}). The output voltages of the Ga_2O_3- and SiC-based converter are approximately 330.87 V and 330.94 V, respectively, and their output voltage ripples are

TABLE 3. Specifications of DC-DC boost converter.

Parameters	Values	Parameters	Values
GaN FET	650 V/180 mΩ	$C_{IN@315\,V}$ (μF)	100
SiC SBD	600 V/1 A	$C_{OUT@500\,V}$ (μF)	6.8
Si FRD	600 V/1 A	L (mH)	1
V_{IN} (V)	200	f (kHz)	100
V_{OUT} (V)	331	R (kΩ)	1

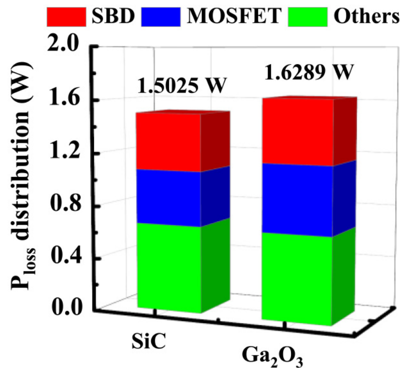

FIGURE 15. Sectional diagrams of power loss distribution in converter simulation.

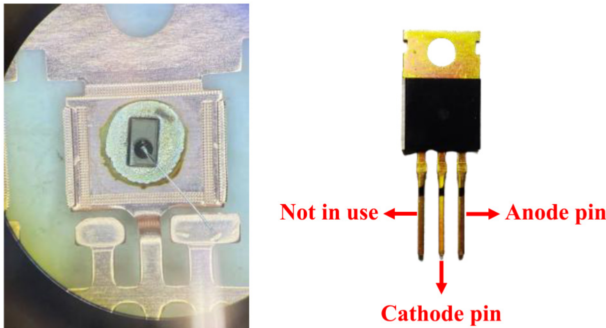

FIGURE 16. Package diagram of the Ga_2O_3 SBD.

TABLE 4. Power loss distribution in converter simulation.

Parameters	SiC converter	Ga_2O_3 converter
P_{IN} (W)	112.3740	112.4340
P_{OUT} (W)	110.8715	110.8051
Total loss (W)	1.5025	1.6289
$P_{loss\text{-}SBD}$ (W)	0.4308	0.4730
$P_{loss\text{-}MOSFET}$ (W)	0.4140	0.5091
$P_{loss\text{-}Others}$ (W)	0.6577	0.6468
Efficiency	98.66%	98.55%

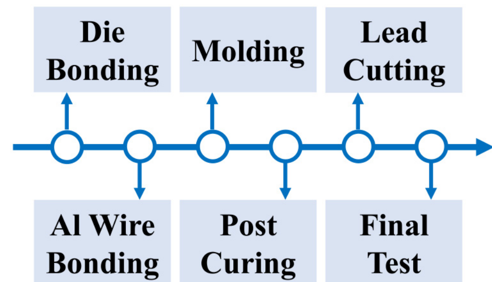

FIGURE 17. Packaging process of the Ga_2O_3 SBDs.

TABLE 5. Experimental results of DC-DC converter.

Parameters	Si converter	SiC converter	Ga_2O_3 converter
V_{IN} (V)	200	200	200
V_{OUT} (V)	329.0	330.8	326.4
P_{IN} (W)	114.46	115.23	113.14
P_{OUT} (W)	108.25	110.64	108.18
Efficiency	94.57%	96.02%	95.62%

less than 0.1%. This minor difference of output voltage is mainly due to the larger on-resistance of the Ga_2O_3 FP-SBD.

The power loss distribution of the Ga_2O_3- and SiC-based converters in the simulation is shown in Table 4 and Fig. 15. The overall loss of the converter is produced by the SBD, MOSFET and other passive devices. The conversion efficiency of the Ga_2O_3-based converter is comparable to that of the SiC-based converter. The slightly lower efficiency of the Ga_2O_3-based converter is mainly due to the larger on-resistance and the slower reverse recovery process of the Ga_2O_3 SBD, which affects the conduction loss and switching loss directly.

The TO-220 package is used for our device to satisfy the needs for application and compare to SiC and Si commercial devices. Fig. 16 shows a photograph of the wire bonding and packaged device, 125 μm Al wire was used to connect the anode of the device and the right package pin, the middle package pin was the cathode pin, and the left pin was not in use. The packaging process is listed in Fig. 17.

The DC-DC boost converter module is shown in Fig. 18, Ga_2O_3 SBD, SiC SBD and Si FRD are tested in the same module. The input signal (V_{GS}) for controlling the MOSFET was generated by an arbitrary function waveform generator (Keysight, 33600A). The input voltage (V_{IN}) was generated by an auto range DC power supply (ITECH, IT6526C), and the output signal (V_{OUT}) was tested through a DC electronic load (ITECH, IT8902E). The voltage and current waveforms were monitored by an oscilloscope (Keysight, MSOX6004A).

Using the parameters shown in Table 3, the experimental waveforms in the DC-DC boost converter based on Si FRD, SiC SBD and Ga_2O_3 SBD are shown in Figs. 19, 20 and 21, respectively. From the diode current (I_D) waveforms, we can

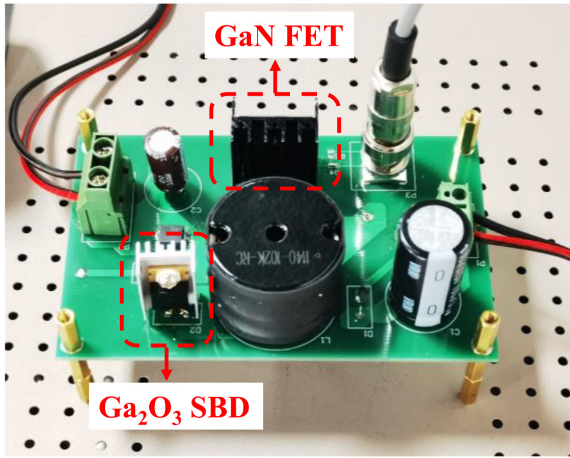

FIGURE 18. Photograph of Ga_2O_3 SBD based DC-DC converter modularized design.

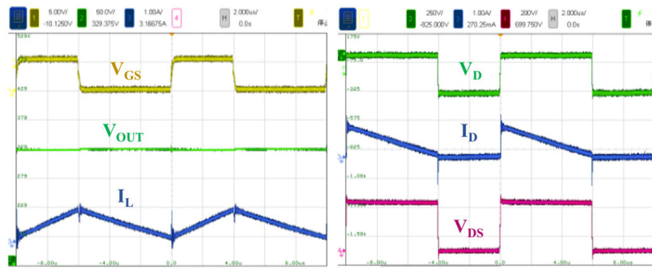

FIGURE 19. Waveforms of V_{GS}, V_{OUT}, I_L, V_D, I_D and V_{DS} in Si FRD-based DC-DC converter.

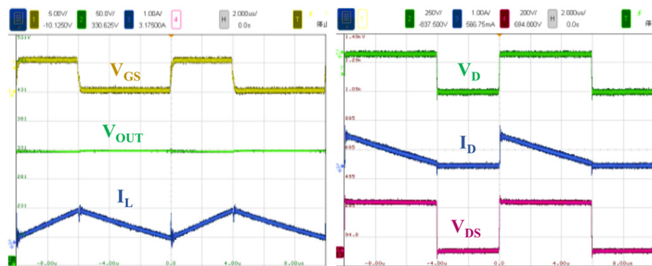

FIGURE 20. Waveforms of V_{GS}, V_{OUT}, I_L, V_D, I_D and V_{DS} in SiC SBD-based DC-DC converter.

obtain that there is a spike of diode current (I_D) in each waveform, and the spike value of the Ga_2O_3 FP-SBD is larger than that of SiC SBD but better than Si FRD due to the reverse recovery characteristic.

The conversion efficiency is computed with the relationship

$$\eta = \frac{V_{OUT}I_{OUT}}{V_{IN}I_{IN}} \times 100\%, \quad (3)$$

where I_{OUT} and I_{IN} are the output and input current, respectively [53].

The experimental results are shown in Table 5, the conversion efficiency of the Si FRD-, SiC SBD- and Ga_2O_3 SBD-based converters are 94.57%, 96.02% and 95.62%, respectively, and the output voltage ripples are approximately

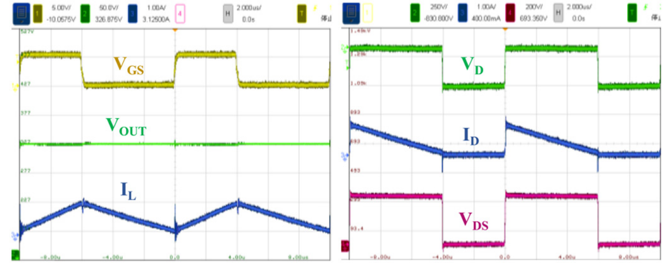

FIGURE 21. Waveforms of V_{GS}, V_{OUT}, I_L, V_D, I_D and V_{DS} in Ga_2O_3 SBD-based DC-DC converter.

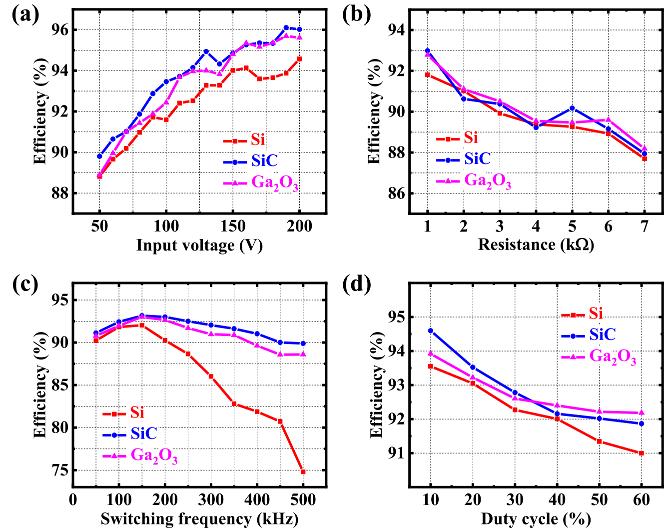

FIGURE 22. Dependence of conversion efficiency on (a) input voltage, (b) load resistance, (c) switching frequency and (d) duty cycle.

0.9%, the efficiency of the Ga_2O_3-based converter is better than that of the Si-based converter and close to that of SiC.

In order to illustrate the performance of the Ga_2O_3 SBD in different situations, the circuit conversion efficiency is measured as a function of four independent variables, including input voltage (V_{IN}), load resistance (R), switching frequency (f) and duty cycle (D). The measured results are shown in Fig. 22.

As depicted in Fig. 22(a), the conversion efficiency increases with increasing input voltage (V_{IN}) from 50 V to 200 V. We can obtain a conversion efficiency reached up to 95.62% at the input voltage of 200 V, while the dependence of the conversion efficiency on the load resistance exhibits the opposite trend in Fig. 22(b), because the power loss is affected by the variation of resistance directly [54]. The efficiency in Fig. 22(b), (c) and (d) was measured with the input voltage of 100 V, as the output voltage would exceed the breakdown voltage of the device in some cases with the input voltage of 200 V. The efficiency decreased with increasing switching frequency in Fig. 22(c), as the switching process of the MOSFET and SBD due to more power losses [55], and the increase in conduction loss mainly affected the efficiency in Fig. 22(d).

From the above demonstrations, the performance of the Ga_2O_3-based converter is superior to that of the Si converter and inferior to that of SiC in multiple conditions. In fact, the research on Ga_2O_3 devices is just in its infancy, and the performance of Ga_2O_3 SBD is almost comparable to SiC SBD, so we can believe that it will be further enhanced with the optimization of our Ga_2O_3 device in the next stage.

VII. CONCLUSION

The β-Ga_2O_3 FP-SBD has approving forward conduction characteristics and possesses a breakdown voltage exceeding 600 V. A SPICE model of Ga_2O_3 FP-SBD is constructed and implemented into DPT circuit and boost converter simulation. The experimental results with a reverse recovery time of 8.8 ns and reverse recovery charge of 8.33 nC when switching from a forward current of 1 A to a reverse bias voltage of 100 V with a di/dt of 400 A/μs are analogous with the DPT simulation results, which reveals the validity of our model. A current of 2 A can be obtained at the forward voltage of 2 V with the large-area device, meanwhile, the breakdown voltage is 467 V. The conversion efficiency of the Ga_2O_3-based converter module after device packaging with TO-220 is comparable to that of the SiC-based converter, and the value grows with increasing input voltage, while with decreasing switching frequency, duty cycle and load resistance. The efficiency value of the Ga_2O_3-based converter is almost consistent with that of the SiC-based converter, and reaches up to 95.62% at the input voltage of 200 V, which indicates the great potential of Ga_2O_3-based devices and circuits. With the reduction of the cost and the improvement of the material quality, power devices and circuits based on Ga_2O_3 material will have promising applications in the foreseeable future.

REFERENCES

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2010.

[2] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Ga_2O_3 Schottky barrier diodes fabricated by using single-crystal Ga_2O_3 (010) substrates," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 493–495, Apr. 2013.

[3] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β- Ga_2O_3 (010) substrates," *Appl. Phys. Lett.*, vol. 100, no. 1, 2012, Art. no. 013504.

[4] M. Higashiwaki et al., "Temperature-dependent capacitance–Voltage and current–Voltage characteristics of Pt/Ga_2O_3 (001) Schottky barrier diodes fabricated on n–Ga_2O_3 drift layers grown by halide vapor phase epitaxy," *Appl. Phys. Lett.*, vol. 108, no. 13, 2016, Art. no. 133503.

[5] A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, "High-quality β- Ga_2O_3 single crystals grown by edge-defined film-fed growth," *Jpn. J. Appl. Phys.*, vol. 55, no. 12, 2016, Art. no. 1202A2.

[6] H. Murakami et al., "Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy," *Appl. Phys. Exp.*, vol. 8, no. 1, 2014, Art. no. 15503.

[7] S. Pearton, F. Ren, M. Tadjer, and J. Kim, "Perspective: Ga_2O_3 for ultra-high power rectifiers and MOSFETS," *J. Appl. Phys.*, vol. 124, no. 22, 2018, Art. no. 220901.

[8] S. J. Pearton et al., "A review of Ga_2O_3 materials, processing, and devices," *Appl. Phys. Rev.*, vol. 5, no. 1, Mar. 2018, Art. no. 11301.

[9] F. Ren, J. C. Yang, C. Fares, and S. J. Pearton, "Device processing and junction formation needs for ultra-high power Ga_2O_3 electronics," *MRS Commun.*, vol. 9, no. 1, pp. 77–87, 2019.

[10] S. B. Reese, T. Remo, J. Green, and A. Zakutayev, "How much will gallium oxide power electronics cost?" *Joule*, vol. 3, no. 4, pp. 903–907, 2019.

[11] K. Konishi et al., "1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes," *Appl. Phys. Lett.*, vol. 110, no. 10, 2017, Art. no. 103506.

[12] H. Zhou et al., "High-performance vertical β-Ga_2O_3 schottky barrier diode with implanted edge termination," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1788–1791, Nov. 2019.

[13] M. Ji et al., "Demonstration of large-size vertical Ga_2O_3 schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 41–44, Jan. 2021.

[14] W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, "Field-plated Ga_2O_3 trench schottky barrier diodes with a $BV^2/R_{on,\ sp}$ up to 0.95 GW/cm^2," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 107–110, Jan. 2020.

[15] Y. Lv et al., "Enhancement-mode β-Ga_2O_3 metal-oxide-semiconductor field-effect transistor with high breakdown voltage over 3000 V realized by oxygen annealing," *Physica Status Solidi (RRL)–Rapid Res. Lett.*, vol. 14, no. 3, 2020, Art. no. 1900586.

[16] H. Dong et al., "Fast switching β-Ga_2O_3 power MOSFET with a trench-gate structure," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1385–1388, Sep. 2019.

[17] Y. Lv et al., "Lateral source field-plated β-Ga_2O_3 MOSFET with recorded breakdown voltage of 2360 V and low specific on-resistance of 560 mΩ cm^2," *Semicond. Sci. Technol.*, vol. 34, no. 11, 2019, Art. no. 11LT02.

[18] J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "2.3 kV field-plated vertical Ga_2O_3 schottky rectifiers and 1 A forward current with 650 V reverse breakdown Ga_2O_3 field-plated schottky barrier diodes," in *Proc. IEEE Device Res. Conf.*, 2018, pp. 1–2.

[19] Q. He et al., "Over 1 GW/cm^2 vertical Ga_2O_3 schottky barrier diodes without edge termination," *IEEE Electron Device Lett.*, vol. 43, no. 2, pp. 264–267, Feb. 2022.

[20] Z. Hu et al., "Field-plated lateral β-Ga_2O_3 Schottky barrier diode with high reverse blocking voltage of more than 3 kV and high DC power figure-of-merit of 500 MW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1564–1567, Oct. 2018.

[21] J. Yang et al., "Dynamic switching characteristics of 1 A forward current β-Ga_2O_3 rectifiers," *IEEE J. Electron Devices Soc.*, vol. 7, no. 1, pp. 57–61, Mar. 2019.

[22] W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, "Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, p. 12.

[23] Y. Zhang et al., "1200 V GaN vertical fin power field-effect transistors," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2017, p. 9.

[24] Z. Hu et al., "1.6 kV vertical Ga_2O_3 FinFETs with source-connected field plates and normally-off operation," in *Proc. Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2019, pp. 483–486.

[25] N. Allen et al., "Vertical Ga_2O_3 Schottky barrier diodes with small-angle beveled field plates: A Baliga's figure-of-merit of 0.6 GW/cm^2," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1399–1402, Sep. 2019.

[26] C. Lin et al., "Vertical Ga_2O_3 Schottky barrier diodes with guard ring formed by nitrogen-ion implantation," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1487–1490, Sep. 2019.

[27] S. Sharma, K. Zeng, S. Saha, and U. Singisetti, "Field-plated lateral Ga_2O_3 MOSFETs with polymer passivation and 8.03 kV breakdown voltage," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 836–839, Jun. 2020.

[28] Q. M. He et al., "Schottky barrier rectifier based on (100) β-Ga_2O_3 and its DC and AC characteristics," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 556–559, Apr. 2018.

[29] B. K. Mahajan, Y.-P. Chen, W. Ahn, N. Zagni, and M. A. Alam, "Design and optimization of β-Ga_2O_3 on (H-BN layered) sapphire for high efficiency power transistors: A device-circuit-package perspective," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018, p. 24.

[30] W. Jun et al., "10-kV SiC MOSFET-based boost converter," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2056–2063, Nov./Dec. 2009.

[31] J. Das et al., "A 96% efficient high-frequency DC–DC converter using E-mode GaN DHFETs on Si," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011.

[32] X. Zhong, X. Wu, W. Zhou, and K. Sheng, "An all-SiC high-frequency boost DC–DC converter operating at 320 °C junction temperature," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5091–5096, Oct. 2014.

[33] J. M. de Andrade, M. A. Salvador, R. F. Coelho, and T. B. Lazzarin, "General method for synthesizing high gain step-up DC-DC converters based on differential connections," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13239–13254, Dec. 2020.

[34] M. S. Nikoo, A. Jafari, N. Perera, and E. Matioli, "Efficient high step-up operation in boost converters based on impulse rectification," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11287–11293, Nov. 2020.

[35] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M. X. Wang, and A. Dentella, "Investigations of 600-V GaN HEMT and GaN diode for power converter applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2441–2452, May 2014.

[36] T. Ibuchi, T. Funaki, S. Ujita, M. Ishida, and T. Ueda, "Conducted noise of GaN Schottky barrier diode in a DC-DC converter," *IEICE Electron. Exp.*, vol. 12, no. 24, Dec. 2015, Art. no. 20150912.

[37] S. Han, S. Yang, R. Li, X. Wu, and K. Sheng, "Current-collapse-free and fast reverse recovery performance in vertical GaN-on-GaN schottky barrier diode," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5012–5018, Jun. 2019.

[38] G. Spiazzi, S. Buso, M. Citron, M. Corradin, and R. Pierobon, "Performance evaluation of a Schottky SiC power diode in a boost PFC application," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1249–1253, Nov. 2003.

[39] L. Efthymiou et al., "Zero reverse recovery in SiC and GaN Schottky diodes: A comparison," in *Proc. Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2016, pp. 71–74.

[40] Q. He et al., "Schottky barrier diode based on β-Ga_2O_3 (100) single crystal substrate and its temperature-dependent electrical characteristics," *Appl. Phys. Lett.*, vol. 110, no. 9, 2017, Art. no. 93503.

[41] J. Yang et al., "Vertical geometry 33.2 A, 4.8 MW cm^2 Ga_2O_3 field-plated Schottky rectifier arrays," *Appl. Phys. Lett.*, vol. 114, no. 23, 2019, Art. no. 232106.

[42] Y. Wei et al., "Experimental study on static and dynamic characteristics of Ga_2O_3 Schottky barrier diodes with compound termination," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10976–10980, Oct. 2021.

[43] J. Yang et al., "Reverse breakdown in large area, field-plated, vertical β-Ga_2O_3 rectifiers," *ECS J. Solid State Sci. Technol.*, vol. 8, no. 7, 2019, Art. no. Q3159.

[44] R. Sharma et al., "Effect of probe geometry during measurement of $>$ 100 A Ga_2O_3 vertical rectifiers," *J. Vacuum Sci. Technol. A*, vol. 39, no. 1, 2021, Art. no. 13406.

[45] K. Zhou et al., "A unified hybrid compact model of β-Ga_2O_3 Schottky barrier diodes for mixer and rectifier applications," *Sci. China Inf. Sci.*, vol. 64, no. 11, pp. 1–2, 2021.

[46] S. Yin, Y. Gu, K. J. Tseng, J. Li, G. Dai, and K. Zhou, "A physics-based compact model of SiC junction barrier Schottky diode for circuit simulation," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3095–3103, Aug. 2018.

[47] C. M. Tan and K.-J. Tseng, "Using power diode models for circuit simulations-A comprehensive review," *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 637–645, Jun. 1999.

[48] R. Kotecha, G. Moreno, B. Mather, and S. Narumanchi, "Modeling needs for power semiconductor devices and power electronics systems," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, p. 12.

[49] Y.-T. Chen et al., "Implementation of a 900 V switching circuit for high breakdown voltage β-Ga_2O_3 Schottky diodes," *ECS J. Solid State Sci. Technol.*, vol. 8, no. 7, pp. Q3229–Q3234, 2019.

[50] X. Lu, X. Zhang, H. Jiang, X. Zou, K. M. Lau, and G. Wang, "Vertical β-Ga_2O_3 Schottky barrier diodes with enhanced breakdown voltage and high switching performance," *Physica Status Solidi*, vol. 217, no. 3, 2020, Art. no. 1900497.

[51] L. Nela, R. Van Erp, G. Kampitsis, H. K. Yildirim, J. Ma, and E. Matioli, "Ultra-compact, high-frequency power integrated circuits based on GaN-on-Si Schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1269–1273, Feb. 2021.

[52] H. Gong et al., "1.37 kV/12 a NiO/-Ga_2O_3 heterojunction diode with nanosecond reverse recovery and rugged surge-current capability," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12213–12217, Nov. 2021.

[53] S. S. Alharbi, S. S. Alharbi, A. M. Al-bayati, and M. Matin, "A comparative performance evaluation of Si IGBT, SiC JFET, and SiC MOSFET power devices for a non-isolated DC-DC boost converter," in *Proc. North Amer. Power Symp. (NAPS)*, 2017, pp. 1–6.

[54] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[55] S. S. Alharbi, A. M. S. Al-bayati, S. S. Alharbi, and M. Matin, "Performance evaluation of a DC-DC boost converter with wide bandgap power devices," in *Proc. IEEE Conf. Technol. Sustainabil. (SusTech)*, 2017, pp. 1–6.