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Application of e-Beam Voltage Contrast Technique for Overlay Improvement and Process Window Control in Multi-Patterning Interconnect Scheme

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ABSTRACT Interconnect development for the new technology node requires coordinated efforts of multiple module teams working to co-optimize patterning and metallization solutions to meet performance and yield, and reliability targets. This paper presents the results of interconnect patterning optimization to improve overlay and process window control using a novel methodology, Design-for-Inspection™ (DFI). Using design-assisted voltage contrast measurement techniques, the method enables in-line test and monitoring of process induced overlay and CD variation of back-end-of line (BEOL) features built with litho-etch-litho-etch (LELE) patterning. While only some of the features of multi-color patterning scheme are chosen to be aligned directly, other combination of metal line and via colors may have uncontrolled misalignment risking open or short failures. The paper shows how the complete metrology coverage of multi-color combinations between dual patterned via and dual patterned metal lines helps driving the improvement of overlay and process margins in 14nm technology. The optimized process margin for via opens enables higher yields and better reliability.

INDEX TERMS Multi-patterning, overlay, misalignment, process window, BEOL, e-Beam, voltage contrast, FinFET.

I. INTRODUCTION

The Moore's Law demands Critical Dimensions (CD) scaling, including BEOL metal lines, to support higher density of devices per chip. One of the consequences of interconnect scaling is the adoption of a multi-patterning scheme for technologies below 20nm generation, until EUV becomes viable at 7nm node and below. Among two approaches – Spacer-Assisted Dual Patterning and Dual Exposure with LELE (Litho-Etch-Litho-Etch), the latter offers more flexibility, especially for bidirectional routing [1]. Also, it is the only available choice for via scaling, which allows printing closely spaced holes.

One of the challenges of multi-exposure patterning within the same layer is maintaining the tight control of the overlay (OVL) between all features of the layers above and the layers below, which depends on the patterning choices and on the implemented alignment scheme.

In-line metrology is adopted at patterning level ("After Develop" and "After Etch" metrology) to provide immediate feedback to manufacturing and enable a rework operation, if possible. Such metrology is very efficient to capture optical misalignment effects, but cannot ensure that the electrical response will also be the same. Wafer bowing and in-film stress may cause additional pattern shifts and cause

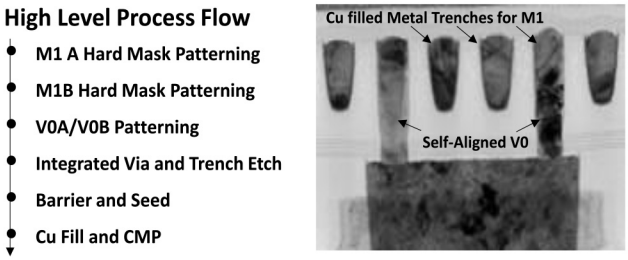

FIGURE 1. Process flow and cross section of M1-V0 structure for interconnect integration with dual patterned metal lines and Self-Aligned Vias used in 14nm BEOL.

Open/Short fails, even if initial optical overlay results showed no problem. We propose a new metrology approach, utilizing PDF Design-for-Inspection methodology to monitor the misalignment electrically in a non-contact way.

II. PROCESS INTEGRATION AND OVERLAY CONTROL

This work is related to some areas of the BEOL development for the 14nm technology and focuses on overlay (OVL) process control for patterning of lower level metal layers [2]. We will discuss a M1-V0 Self-Aligned Via (SAV) process, which uses two LELE patterning sequences for metal lines and vias to meet requirements of 64nm pitch scaling. Figure 1 shows the main process steps for dual-patterning module and a cross-sectional view of a SAV for M1-V0 after full metallization processing.

In LELE patterning approach, the interconnect layout of the chip is split into two sets of lines and two sets of vias per level (using sophisticated decomposition algorithms) which are mapped to separate patterning steps and corresponding masks, which we denote A and B (and sometimes call different "colors") The technology allows any combination of the exposure steps to create a line-via pattern. This is shown in Fig. 2, which shows 4 color combinations as well as potential consequences of mutual misalignment of metal lines and vias.

In SAV integration scheme, the via is patterned after the metal line, and the via is etched only in the region opened in metal line hard mask – as the result, for significantly misaligned vias the final size of the opened and etch via hole may be very small and insufficient to reliably fill with the liner/barrier and copper. This is why the overlay error control plays so critical role in enabling high yield and reliability of interconnects.

During the initial phases of the development, in-line overlay metrology was established to enable process control and patterning optimization. At this initial stage, limited measurements were collected to reduce metrology load and increase the throughput. The implemented alignment scheme is shown in Fig. 3, which shows main vectors of the alignment tree. The overlay was measured for all combinations of the pattern colors, but only some of them were used in the APC feedback loop to enforce a re-work step or cause out-of-control alarms.

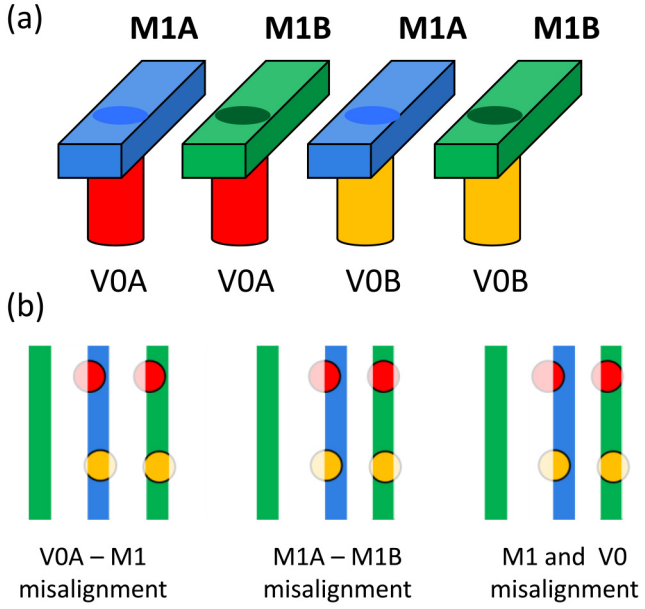

FIGURE 2. (a) Color combinations in dual patterning LELE interconnect scheme and (b) examples of the overlay error effects (metal-to-metal and via-to-metal) causing a risk of potential via open failure in Dual Damascene process with Self-Aligned Vias.

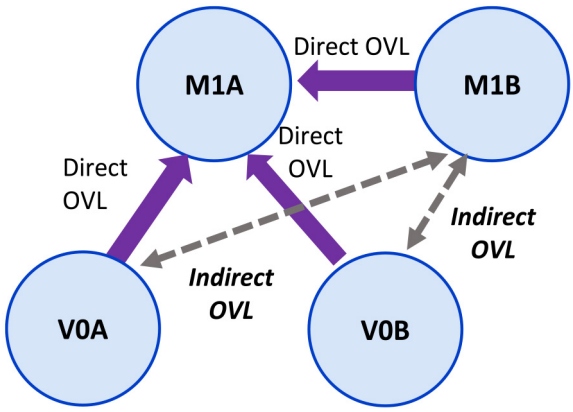

FIGURE 3. Alignment scheme for dual exposure M1 and dual exposure Via0. M1B, V0A, and V0B are all directly aligned to M1A, while V0A and V0B overlay to M1B requires additional alignment control.

III. DESIGN-FOR-INSPECTION™ (DFI) METROLOGY

In order to increase data collection and visibility of a potential downstream impact of overlay errors, we adopted a new electrical metrology technique based on e-Beam Voltage Contrast (VC) inspection.

This technique is called Design-for-Inspection (DFI) and uses the e-Beam VC as a non-contact electrical tester, which performs in-line probing of the dedicated, specially designed micro test structures. The method of detecting the overlay errors is based on similar approach used in electrical measurements and it applies the concept of a series of test structures, each having incrementally increasing built-in misalignment between two subsequent layers (e.g., metal line

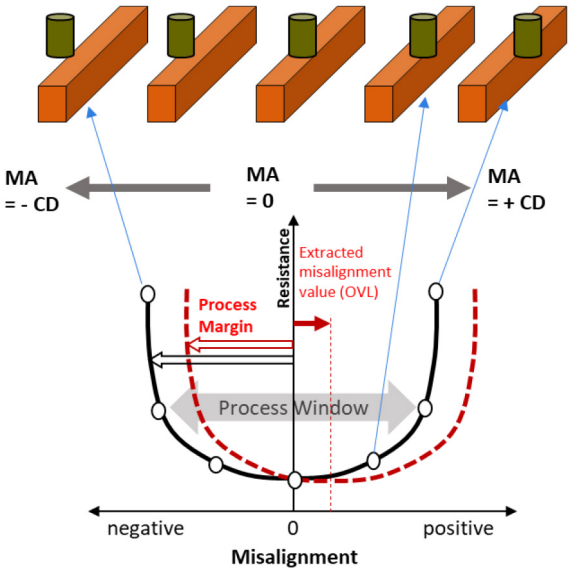

FIGURE 4. **Principle of electrical measurement of the misalignment vector using a set of test structures (for simplicity the vias are shown above the metal lines, although in reality the vias are below the metal lines, despite being printed after the metal lines).**

and via). Misalignment spans the whole width of a feature, including extreme cases where the structure would electrically fail (Fig. 4).

Such structures can be used to characterize the overlay (OVL), process window (PW), and process margin (PM) not only for metal-via pair, but for all critical layers [3], if the proper set of test structures is designed and available.

The e-Beam tool is operating at the conditions (landing energy, current, extraction potentials) which produces a VC signal recorded by the tool detector. The detector, based on the signal from secondary electrons, can distinguish if the metal conductor surface has low (ground) or high (floating) potential [4], and with proper design of the test structure can detect electrical Opens and Shorts.

For the case shown in Fig. 4, the VC response, called here Electrical Response Index (ERI) gives a U-shape Resistance dependence on the intentionally introduced misalignment, "programmed" by design into the set of test structures. The shape and location of the curve minimum allow extraction of the misalignment vector, the process margin and process window for failure-free patterning. In the case of DFI structures, VC gray level signal is used instead of the resistance.

DFI structures offer an advantage of the density, sub-nm level resolution, and high-speed non-contact testing. PDF Solutions' proprietary e-Beam tool (eProbe series [5]) is used to perform high speed VC data collection from large number of DFI cells embedded between IP layout blocks and in the scribe lines between product dies. Unfortunately, the structures are only testable after metal fill and CMP, hence the results cannot be used to react immediately in case of a large misalignment event or process excursion, so a rework cannot be performed as a remedy when the problem is detected.

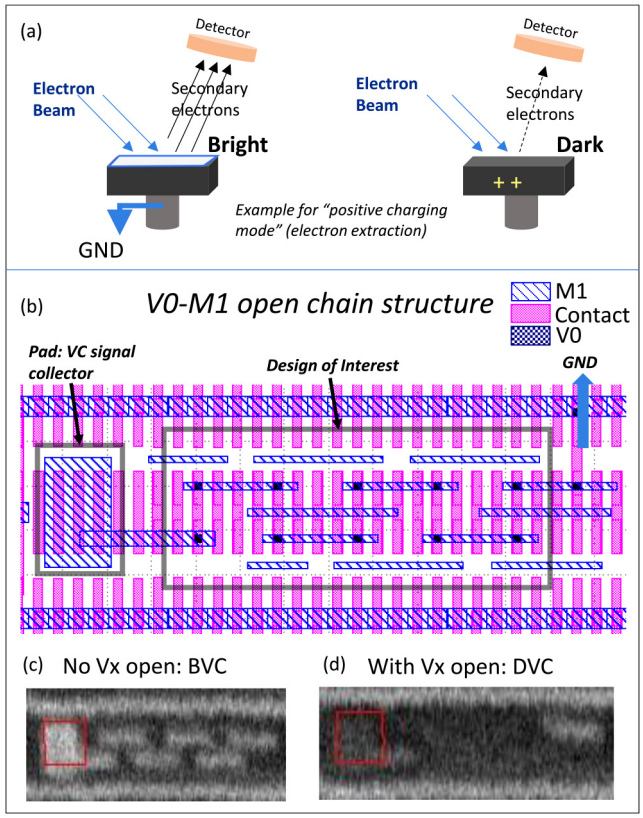

FIGURE 5. **(a) Principle of the BVC and DVC; (b) VC test structure layout for V0-M1 open. Top down SEM images of (c) BVC pad (without V0 open) and (d) DVC pad (with V0 open).**

Fig. 5 shows the principle of the VC, an example of VC test structure for V0-M1 OVL, process margin and process window characterization used in this study.

For VC inspection the eProbe tool operated at a positive charging mode, in which the pad - the VC signal inspection element - is charged positively due to high yield of secondary electron emission. As shown in Fig. 5(a), Bright VC (BVC) is observed when the pad is connected to GND and the electron emission does not impact the potential of the pad. High level of secondary electron emission from the pad provide strong signal recorded by the detector. On the contrary, When the pad is not connected to GND, and is left floating, its surface charges positively due to secondary electron emission, and its electrical potential rises and emission slows down. This results in a dark VC (DVC) signal observed by the detector.

The test structure design is routed as a chain structure, comprised of the metal collector pad, the Design-of-Interest (DOI) and the design construct providing a grounding path (GND). The DOI part represents the area dedicated to the target failure mode, in this case metal-via open (more use case examples can be found in [6]. To perform the test of such structure with e-Beam, only the VC signal from the metal collector pad needs to be collected, as shown in Fig. 5 (b). In such design, a via open event can be detected by

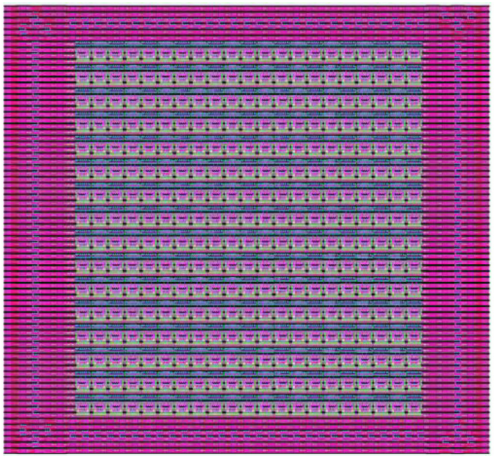

FIGURE 6. Example of a block of DFI test structures grouped together for fast e-Beam inspection scan.

monitoring VC signal of the metal collector pad of the V0-M1 test structure, which, depending on the electrical state, can be either BVC or DVC as shown in Fig. 5 (c and d).

For the current study, the DFI structures with wide range of intentional misalignment (MA) are placed in one analysis block for OVL, PM and PW extraction. Each analysis block usually represents one specific design of experiment (DOE). Blocks with various DOE purposes have different DOI element as a "heart" of the DFI structure design. Sometimes the blocks of different DoE's can be grouped together in a row or a column to enable swath scan mode for faster e-Beam inspection.

Moreover, DFI e-beam system can also operate in a step-and-scan mode for cross-field blocks scanning. The case demonstrated here is designed for specific detection of V0-M1 open, where MA design DOE is achieved by varying relative position of M1 to V0 as illustrated in Fig. 7 (a-c). The normalized VC gray level response is shown in Fig. 7 (d). The ERI used as a metric is plotted here versus an intentional MA value introduced by design in a family of DFI tests structures. The structures are combined in a single inspection block to test the whole set for ERI and detect M1-V0 opens, and then extract the OVL error, process margin, and process window values using a curve fitting.

IV. DFI OVERLAY AND PROCESS MARGIN RESULTS

DFI structures described in Section II were placed on Technology Development Vehicle to support characterization of Overlay errors and help to establish and monitor the process window required for robust yields. A separate set of structures was designed for each of the pattern combinations shown in Fig. 2. Four cases of metal-via combinations yielded OVL error, PW, and PM. M1A-M1B misalignment structures were not designed due to design rule restrictions, the OVL error was extracted indirectly from the results of other structures.

In the multi-exposure patterning, M1A was set as anchor point for V0A and V0B Overlay, and was used for Advanced

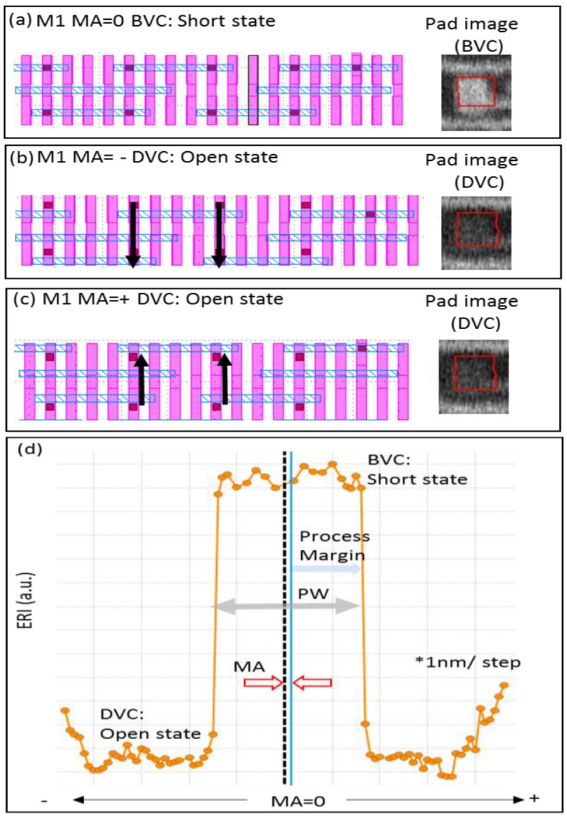

FIGURE 7. Layouts of V0-M1 open (a) with M1 to V0 MA=0 (b) with M1 to V0 MA = - and (c) with M1 to V0 MA =+, and patch images aside are VC images on pad. (d) A curve of normalized VC gray level response to reference for V0 open with respect to designed MA value.

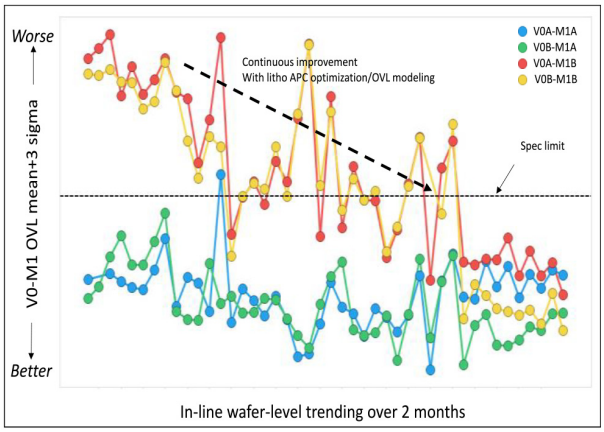

FIGURE 8. Overlay trends for Dual-exposure via to Dual-exposure metal lines. V0A/B better OVL to M1A than to M1B. Time trend shows progress in OVL due to process improvement.

Process Control (APC) feedback and process monitoring. Quality of V0A-M1B and V0B-M1B OVL depends mostly on the alignment of the M1B patterns, and although the OVL error was measured in-line, it was not used for APC. As a consequence, overall OVL performance showed significant differences between V0 to M1A and V0 to M1B patterns.

Fig. 8 illustrates wafer-level trending of the V0-M1 OVL (mean+3 sigma) collected using DFI over a period of

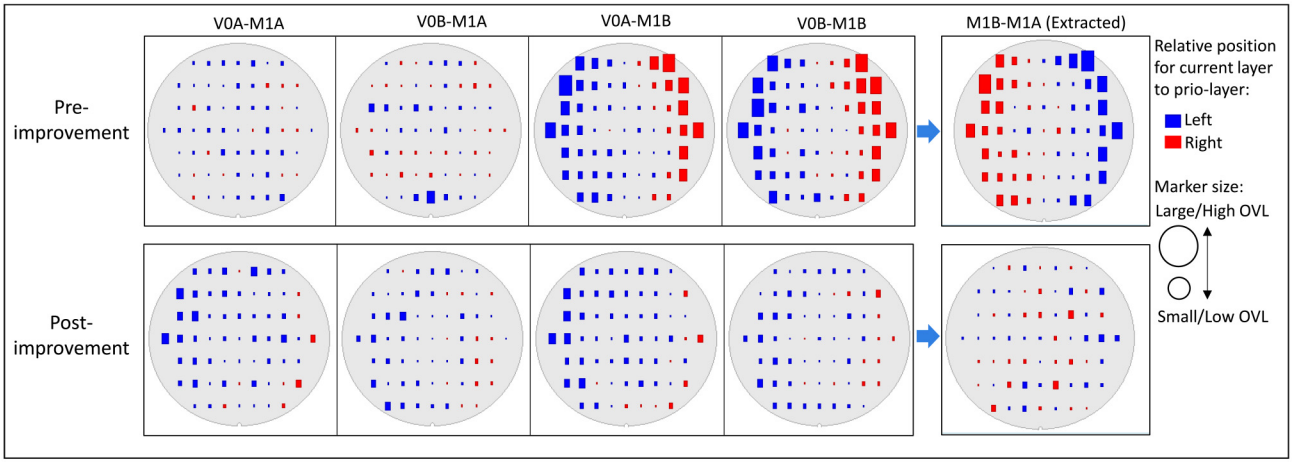

FIGURE 9. **Wafer Maps of misalignment values (OVL) measured with DFI structures. Larger marker size indicates larger OVL error, and the color shows the error sign (the polarity of misalignment direction for corresponding layers, see the legend). V0A and V0B - both Via exposures aligned directly to M1A pattern show good results with small OVL error, while the same V0 patterns show poor alignment to the second M1B exposure pattern. After improving lithographic process, OVL patterns are matched for V0 aligned to both M1A and M1B.**

2 months. Each line marked with a different color represents a different V0-M1 exposure combination for OVL data acquisition. During initial data collection V0A/B-M1B OVL was found to perform much worse than V0A/B-M1A OVL, with no clear OVL delta between V0A-M1 and V0B-M1, regardless of M1 exposure. By comparing OVL performance across 4 different V0-M1 color combinations, M1A-M1B was the top suspected root cause to induce high OVL error for V0A-M1B and V0B-M1B downstream. Although DFI was not measuring M1A-M1B OVL directly, M1A-M1B OVL could be extracted from interpolation of V0-M1A and V0-M1B OVL values. Clearly, the OVL errors in the initial time period were above the specification limit and created high risk of yield loss due to potential V0-M1B open. Corrective actions were introduced by the engineering team for M1A-M1B overlay improvement. After optimizing lithography APC scheme and updating overlay models, significant improvement in V0-M1B OVL was achieved. This result is reflected in the OVL trend shown in the later time period in Fig. 8.

Pre- and post- improvement results are shown in Fig. 9. as wafer maps for directly measured V0-M1 OVL and for extracted M1A-M1B OVL errors. Larger marker size indicates larger OVL error, and the marker colors indicate the error sign - the polarity of misalignment direction for corresponding layers. V0-M1B and M1A-M1B OVL show similar edge elevation pattern, while V0-M1A has rather uniform OVL profile (both V0A and V0B exposures). After optimization of lithographic process and overlay procedures, wafer maps of OVL errors are minimized and matched between both metal exposures V0-M1A and V0-M1B.

In addition to overlay metrology, DFI method can also measure Process Margin (PM), as shown by the arrows in the plot of Fig. 4. Process Margin is defined as a smaller of the two values from the center axis to the two branches of the OVL curve. In our case, the Process Margin is measured by the e-Beam Voltage Contrast. PM variation is affected by

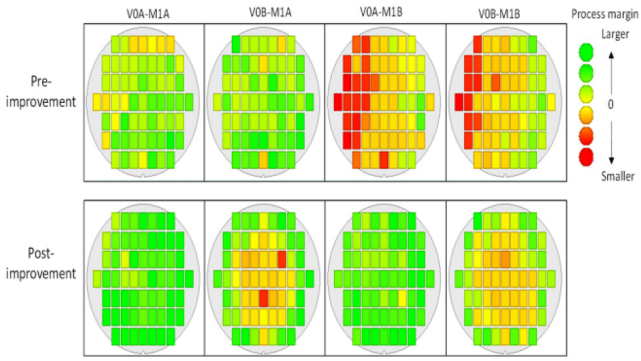

FIGURE 10. **Wafer maps of Process Margin for V0-M1 Opens by die, extracted using DFI structures. The window is very narrow when the alignment is poor, and improves with tighter OVL (RED corresponds to very narrow PM, GREEN is good).**

both M1/V0 CD and their OVL. Analysis of the wafer-level spatial patterns, the regions with high risk of via open and lower yield can be identified in fully built BEOL stack.

Fig. 10 shows wafer maps of process margin across four combination of V0-M1 colors, before and after litho process improvement discussed earlier. Narrow process margin for V0-M1B open is observed at edge of wafer due to poor V0-M1B OVL, and significant enhancement of the process margin is achieved after litho improvement. With DFI methodology, OVL and PM can all feedback to inline methodology to verify process-induced OVL bias post litho step and highlight any risk induced by CD and OVL variations.

V. DFI PROCESS WINDOW CHARACTERIZATION

Besides OVL error and process margin values, the process window (PW) metric, defined as the width of OVL curve in Fig. 4, can also be obtained from the curve fitting. It should be noted that the process window is rather insensitive

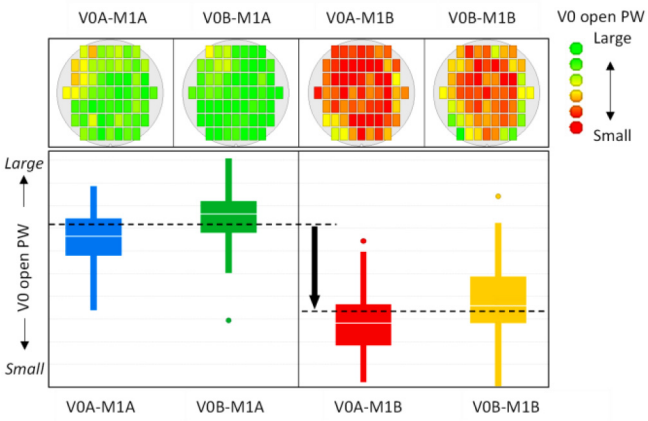

FIGURE 11. **Wafer maps and box plots for process window (distribution of values at die level) for V0-M1 opens.**

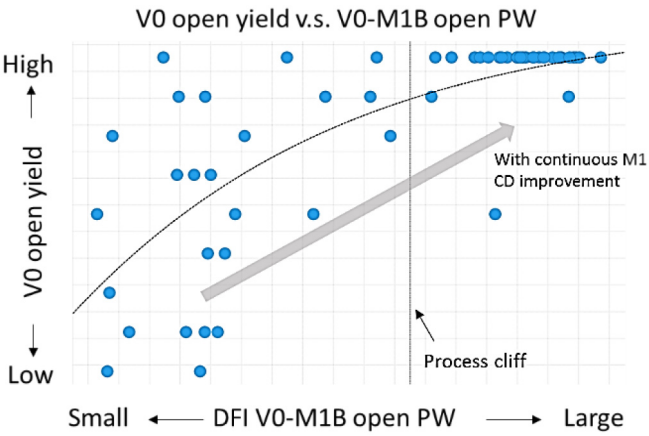

FIGURE 12. **Wafer level yield loss curve of electrical V0 open yield versus PW of DFI V0-M1B open; vertical dashed line represents process cliff for V0-M1B open.**

to the misalignment vector, but strongly dependent on the CDs of the metal line and the via. Therefore, variation of PW highly correlates to CD shifts. Fig. 11 shows process window for V0 opens, with wafer maps and box plots for 4 different color combinations. V0-M1B open PW is found to be consistently lower than V0-M1A one, indicating smaller M1B CD than M1A.

During the early stages of process development, V0 opens were dominated by patterning related M1 opens. In addition, V0 chain failure rates for the structures with M1B metal lines were higher (more failures) than the ones built with M1A lines. To increase the V0 via chain yields and open the process window, M1 target CD was increased. Obviously, there is a trade-off and a delicate balance between Line-Space CD balancing, as with wider lines the space is reduced and the risk of shorts is increasing. Fortunately, with a good Self-Aligned Via process the risk of via-induced metal shorts can be keep in control.

The improvement of V0-M1 open PW due to M1A/M1B CD enlargement provided well needed margins for via open, and increased the yield of electrical structures. As a monitor of V0 health we used electrically tested via chains designed by PDF Solutions and placed on the same Technology Development Vehicle chip. This allowed direct correlation of both metrics. Fig. 12 shows a correlation of an electrical V0 open yield measured at post-process test to V0-M1B process window measured in-line with e-Beam on DFI structures. Data confirms that the improved process (above the process cliff) provides higher V0 yields. Process centering above the cliff and process window control is needed to ensure V0 stable performance. DFI test structures can provide monitor for multiple process metrics to ensure stable V0 yields in all pattern combinations in LELE patterning scheme implemented in our process.

VI. CONCLUSION

This work demonstrated a new methodology of monitoring multi-patterning alignment scheme using e-Beam-based DFI system. M1/V0 OVL, Process Margin and Process Window examples proved applicability to detect OVL issues and support process improvement. In-line monitoring using DFI system was successfully applied to identify root causes of the narrow Process Margin and to drive process improvement. The proposed method can be extended to all BEOL layers and help control OVL and PM performance during New Product Introduction and volume production. Although our current project focused on characterization of multi-patterning overlay issues in 14nm, the methodology is fully applicable to future technology nodes, where multi-patterning is further extended using Spacer-Assisted Quadrupole Patterning, LELE with eUV lithography, or their combinations.

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