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Area-Efficient Power-Rail ESD Clamp Circuit With False-Trigger Immunity in 28nm CMOS Process

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ABSTRACT In this work, a new power-rail electrostatic discharge (ESD) clamp circuit with hybrid trigger mechanism is proposed and implemented in a 28-nm CMOS process. Measurements from silicon chips show that the proposed power clamp circuit is capable of achieving μs-level transient response time with RC time constant of only 10 ns, thus greatly improving area efficiency. Compared to traditional transient circuit with same response time, the proposed one achieves a trigger circuit (TC) area reduction of over 90%. The proposed circuit achieves strong false-trigger immunity under fast power-on conditions. In addition, the circuit also has low standby leakage current of less than 10 nA at different BigFET widths. To verify the proposed circuit, the simulation and test results are analyzed in detail for this paper.

INDEX TERMS Electrostatic discharge (ESD), hybrid-triggered circuit, area-efficient, false-trigger immunity, low leakage current.

I. INTRODUCTION

The rapid development of integrated circuits (ICs) has made it particularly important to improve the performance and reliability of IC products. Electrostatic discharge (ESD) protection has become the main measure to ensure the reliability of IC products [1], [2]. To achieve superior ESD protection performance, power-rail ESD clamp circuits are crucial in the whole chip ESD protection design [3]. Power-rail clamp circuit usually consists of a trigger circuit (TC) and a clamp device (BigFET) [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. The power clamp circuit relies mainly on the channel of the BigFET to discharge ESD current, and it requires a TC to distinguish between ESD stress and normal signals [9]. Depending on the triggering mechanism, traditional triggering circuits can be divided into transient-triggered circuits and static-triggered circuits [4], [5]. Fig. 1(a) shows the traditional transient power-rail ESD clamp circuit with the trigger mechanism of resistor-capacitor (RC) charging delay effect [3]. In the case of an ESD event, the RC charging delay effect maintains the voltage of Node A, V_A, at a logic low, and then the voltage of Node Gate, V_G, is logic high to turn on the ESD clamping MOS transistor (BigFET) to discharge the ESD current. However, in case a fast power-on pulse is encountered with the same transient characteristics as an ESD event, the transient circuit usually suffers from false trigger issues [4], [5], which leads to unnecessary power consumption [4], [5], [6]. In addition, RC time constant is correlated with the layout area, and the RC time constant of 50-100 ns consumes large layout area and cost. Another traditional static power-rail ESD clamp circuit using the voltage-triggered mechanism is shown in Fig. 1(b) [7], [8]. Diode strings are typically used to detect the voltage level of the VDD. When the ESD pulse voltage on VDD is higher than the turn-on voltage of the R-D trigger module, this trigger path is conducted, resulting in a logic low voltage of V_A. Then, the V_G is logic high and turns on the BigFET to discharge ESD current. However, for advanced nanoscale applications with extremely narrow ESD design windows, static circuit consumes too high standby leakage current (I_{leak}) to obtain a low trigger voltage (V_{t1}) that suits these ESD design windows [9]. In addition,

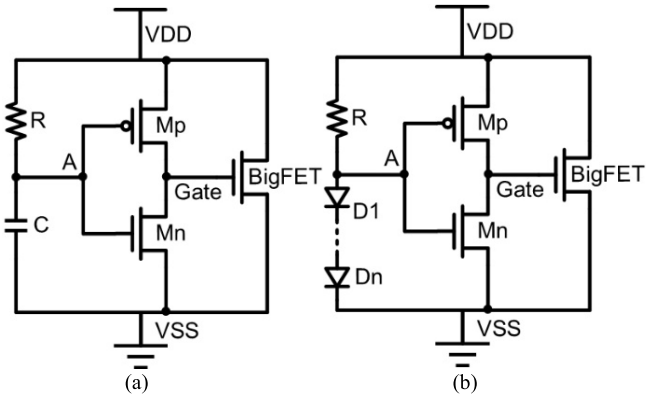

FIGURE 1. **Investigated power-rail ESD clamp circuits: (a) transient-triggered, (b) static-triggered.**

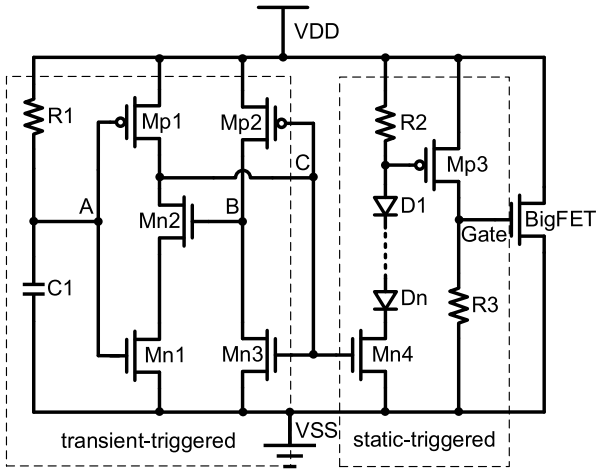

FIGURE 2. **Proposed power-rail ESD clamp circuit with hybrid triggering mechanism.**

static circuits turn on relatively slower compared to transient circuits.

Based on above reports, the traditional transient and static triggering mechanisms for power clamp circuits should be further improved. To solve these issues, some works [4], [16], [17], [18] use multiple time constants—one RC for the detection of the ESD pulses, the second one for controlling the on-time. These circuits typically show compact layout area and immunity to false triggering. In addition, the hybrid triggering method combining static and transient efficiently solves the problems of traditional circuits and provides superior protection performance [6], [7], [8], [9], [10]. While hybrid circuits have great advantages, they still need to be improved in many aspects. Specifically, such as area efficiency and anti-false trigger performance. The sustained weak current path in [6] causes massive unnecessary power consumption. The circuit in [7] shows false triggering in fast power-on pulses with 10-ns rise time. References [9] and [10] with large RC sizes cause the cost to rise and inefficiency of the area.

In this work, a new area-efficient power-rail ESD clamp circuit is proposed. By co-optimizing the two trigger mechanisms, the proposed circuit has strong false-trigger immunity, even in the worst case of fast power-on pulse. In addition, the circuit has low leakage current at different BigFET widths. The proposed circuit with small RC size can achieve transient response times of more than 1 μs, greatly improving area efficiency. In addition, the advantages of the proposed circuit compared to transient, static circuits are verified in this paper. Both simulation and test results based on the 28-nm CMOS process validate the superiority of the proposed circuit.

II. CIRCUIT ANALYSIS AND SIMULATION

Traditional transient-triggered (abbreviated as Transient) and static-triggered (abbreviated as Static) circuits are depicted in Fig. 1 (a) and Fig. 1 (b). The proposed hybrid-triggered circuit is depicted in Fig. 2. The RC time constant of the transient circuit remains the same as that of the proposed one, both being 10 ns. In general, this RC time constant must be over 1 μs to ensure safe clamping behavior in real ESD events [4]. However, large RC time constant will result in large footprint penalty. The proposed circuit can achieve μs-level transient response time with an RC time constant of only 10 ns, greatly improving area efficiency. Therefore, compared to traditional transient circuit with μs-level response time, the proposed one achieves a TC area reduction of over 90%. This advantage of the proposed circuit mainly comes from the timed leakage mechanism of Mn2, which greatly prolongs the transient response time.

The proposed power-rail ESD clamp circuit uses hybrid triggering method to achieve superior ESD protection performance. The proposed circuit achieves sufficient BigFET response time with low RC time constant. This advantage allows the layout area to be greatly reduced, while also obtaining strong anti-false trigger characteristics. Mn1 serves the pull-down path of node C, allowing leakage current of the path only to depend on the size of Mn2, facilitating the flexible adjustment. Mn4 combines the transient trigger part and the static trigger part skillfully. Enabling the static triggered part by turning on Mn4. In addition, Mn4 is off under direct current (DC) conditions, which can ensure that the number of diodes does not affect the I_{leak}. Mp3 is employed to transmit the enable signal of the static triggered part to the BigFET. When static triggered part starts to work, the current flows through R_2 and Mp3 is turned on, setting the node Gate to high level. The comparison of the simulation and test results verifies that the proposed circuit with 2 diodes satisfies the ESD design window of the process used. A proper R_3 design enables the Gate node to be pulled up to a better logic high voltage in ESD events. Once the RC network of the proposed circuit detects an ESD event, transient triggered part starts working. The node B turns low by inversion of the node C. This operation shuts down the pull-down path of the node C by turning off Mn2. The node C is temporarily maintained at high level to transmit the detection signal of transient triggered part to

TABLE 1. Device parameters of the investigated circuits.

Device Name	Parameter Values
$R_{(1.a)}$, $R_{(1.b)}$, R_1, R_2, R_3 (kΩ)	24.6, 24.6, 24.6, 24.6, 18.8
C, C_1 (fF)	408.5
W/L of Mp (Mp1, Mp2, Mp3) (μm/μm)	2.4 / 0.15
W/L of Mn (Mn2, Mn4) (μm /μm)	2.4 / 0.15
W/L of Mn (Mn1, Mn3) (μm /μm)	1.2 / 0.15
W/L of BigFET (μm/μm)	1000/0.15

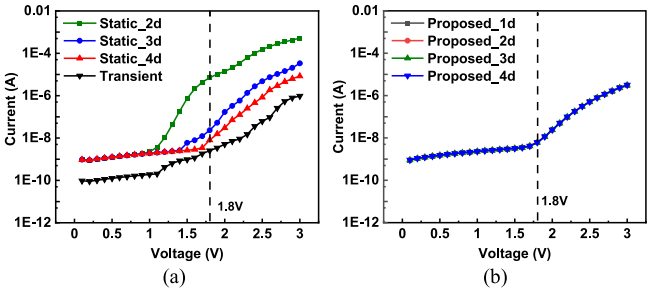

FIGURE 3. DC simulation results of the investigated circuits: (a) traditional circuits, (b) the proposed circuit.

TABLE 2. Comparison of simulation results of Ileak at high temperatures.

Temperature	25 °C	80 °C	125 °C
Transient	2.5 nA	90.5 nA	560.1 nA
Static_2d	5.7 μA	12.8 μA	25.9 μA
Static_3d	91.1 nA	548.3 nA	4.7 μA
Static_4d	8.5 nA	289.1 nA	1.3 μA
Proposed_2d	7.8 nA	129.8 nA	682.6 nA
Proposed_3d	6.9 nA	113.7 nA	663.9 nA
Proposed_4d	6.3 nA	105.5 nA	615.3 nA

static part through Mn4, which realizes the transition from transient triggered mode to static triggered mode. The ESD voltage reaches the turn-on voltage of the static triggered part, then the voltage of node C, V_C, remains logically high. And the voltage of node Gate, V_G, remains in line with the V_C to turn on the BigFET. Over time, when V_C goes low, Mn4 turns off, causing the clamp to turn-off. In addition, when the voltage at VDD is lower than the trigger voltage, it also makes the static triggered part closed, thus turning off the BigFET. With this timed leakage mechanism, the BigFET response time is determined by the leakage current in the pull-down path, which is essentially independent of the time constant of R_1 and C_1. Therefore, the proposed circuit can greatly prolong the transient response time with low RC time constant. The investigated circuits are designed in a 28-nm CMOS process using thick-oxide devices with a normal VDD of 1.8 V. Device parameters of investigated circuits are summarized in Table 1. The investigated circuits include traditional circuits in Fig. 1 and the proposed circuit in Fig. 2.

Except for the listed parameters, all diodes in Fig. 1(b) and Fig. 2 are p+/n-well diodes with the same area of 4 μm^2. The following simulations are performed to verify the above design conclusions.

A. DC SIMULATION RESULTS

Fig. 3 depicts DC simulation results at room temperature. For proposed clamp, BigFET is the major contributor for I_{leak} since it typically employs large sizes to ensure high protection levels. In Fig. 3, a DC voltage sweep from 0 V to 3 V is implemented on the VDD line. The currents obtained by the different circuits are plotted. Static circuits with different numbers of diodes (abbreviated as Static_n-d in the figure) exhibit different DC characteristics than transient circuits. Static trigger circuits with fewer diodes result in higher I_{leak}, which is unacceptable. For static circuits, fewer diodes produce lower V_{t1}, which is beneficial for applications in advanced nanoscale processes where the ESD design window is narrow. The standby leakage current is obtained under normal power supply conditions. At 1.8V normal supply, proposed circuits maintain low I_{leak} with values of 6-7 nA. The I_{leak} of the transient circuit is kept low because the circuit is not sensitive to DC voltage. The I_{leak} of all proposed circuits remain in the low range irrespective of the number of diodes, which confirms the superiority of proposed circuit compared to static one. The proposed circuit has the flexibility to freely adjust the V_{t1} by changing the number of diodes to suit different ESD design windows and application scenarios. The DC simulations at temperatures of 80 °C and 125 °C are also performed and extracted I_{leak} are compared in Table 2. The superior I_{leak} performance of the proposed circuits over that of the static one is fully verified in this table.

B. FAST POWER-UP SIMULATION RESULTS

Fig. 4 depicts fast power-up simulation results of the investigated circuits. A voltage value of 1.8 V with rise time of 10 ns is considered as the worst case for fast power-on pulses. In Fig. 4(a), V_G is plotted for each circuit. The transient circuit is falsely triggered by this pulse with a duration of about 20 ns. While the proposed circuit shows a voltage peak that is not higher than the threshold voltage, BigFET is in the off state, confirming that the circuit has strong immunity against false triggering. In addition, the static triggered part does not turn on during the pulse because 1.8 V is lower than its turn-on voltage. It is worth noting that the transient and proposed circuit have the same RC time constant. The hybrid triggering mechanism of the proposed circuit ensures its robust false-trigger immunity. In addition, the current of proposed circuit is plotted under this fast power-up pulse. The proposed circuit maintains the leakage current at 6 nA after the current peak and achieves low power consumption under fast power-on disturbances. In Fig. 4(b), V_G of the proposed circuit is

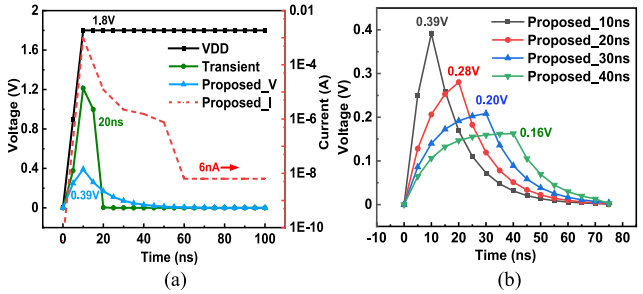

FIGURE 4. Fast power-up simulation results of: (a) all investigated circuits under a rise time of 10 ns, (b) the V_G of proposed circuit under rise time of 10-40 ns pulses.

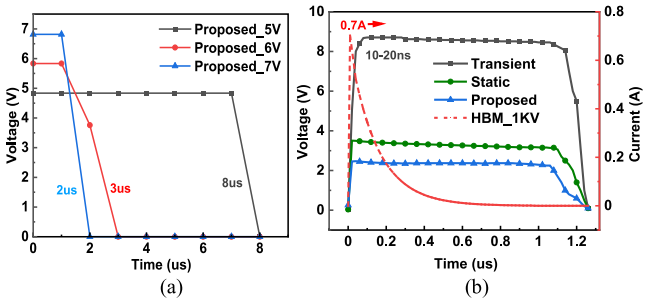

FIGURE 5. Transient simulation results of the investigated circuits: (a) under 5/6/7V transmission line pulsing (TLP) like transient EOS pulses and (b) under a 1 kV HBM like current pulse.

plotted under voltage value of 1.8 V with rise time of 10-40 ns pulses. With longer rise time, the peak of V_G becomes lower, which proves that 10-ns rise time is the worst case for fast power-on pulses. The immunity to false triggering of the proposed circuit has a great advantage over traditional circuits and most existing clamp circuits [4], [6], [7], [10]. The proposed circuit is totally immune to power-up pulses with rise time of 10-40 ns, which is assuring for immunity against normal power-up pulses with rise time over 100 μs [11].

C. TRANSIENT EOS SIMULATION RESULTS

Fig. 5(a) depicts the proposed circuit with V_G plotted under transient pulses of 10-ns rise time and 10-μs duration with amplitudes of 5/6/7 V. With such EOS-like pulses, the proposed circuit can achieve BigFET response time at the ∼ μs level, which is sufficient to discharge ESD current. In addition, with increasing values of voltage, the leakage current in the pull-down path increases, thus the transient response time is shortened. Therefore, the proposed circuit has short response time for overvoltage disturbances under power-on conditions and latch-up effect can be effectively avoided. In actual measurement, the appropriate voltage values are carefully selected for the sake of device reliability. The proposed circuit realizes sufficient response time with small footprint, confirming the superiority of the co-optimization in Fig. 2.

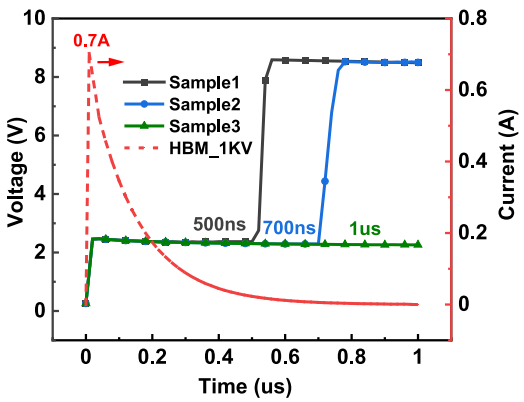

FIGURE 6. Transient simulation results of three samples of proposed circuits with different transient response time under a 1 kV HBM like current pulse.

D. TRANSIENT HBM SIMULATION RESULTS

In Fig. 5(b), a human-body model (HBM)-like current pulse with rise time of 10 ns and peak current of 0.7 A (equivalent to 1 kV HBM level) is simulated on the V_{DD} line, and the resulting clamping voltage (V_{clamp}) is plotted. The transient and proposed circuit have the same RC time constant. The response time of the transient circuit is only 10-20 ns, and the proposed one achieves response time of over 1μs to ensure that ESD current is fully discharged. HBM represents a real ESD event with duration above 1μs [22]. With the proper design of R_3, the proposed circuit can safely discharge current at a lower V_{clamp} than the static one.

The proposed circuit provides prolonged transient response time once triggered. For better adaptation to various application scenarios and preventing the power consumptions due to false triggering, the circuit can also achieve adjustable transient response time. Adjustable transient response time can be achieved by scaling the size of Mn2. The reduced size of Mn2 means lower leakage current, which obtains longer transient response time. As shown in Fig. 6, the three proposed circuit samples obtain transient response time of 500ns, 700ns and 1μs, respectively. The transient response time of the proposed circuit is freely adjustable, giving it greater flexibility and wider range of application scenarios. The adjustment method can be easily implemented in simulations to provide guidance to circuit designers.

E. ROBUSTNESS SIMULATION RESULTS

Fig. 7 shows the effect of process corners variations on design performance. The corners to be simulated must least cover (SS, SF, TT, FS, FF) × (−45°C ∼ 125°C). These simulation results are presented over all process and temperature corners. The proposed circuit is simulated under a 1kV HBM pulse, so voltage corners are not concerned. For transient response time, sample3 and sample4 are taken as examples to demonstrate. Sample3 is the default design and sample4 is the optimized design for PVT variations by adjusting the size of Mn2. In sample3, the proposed circuit

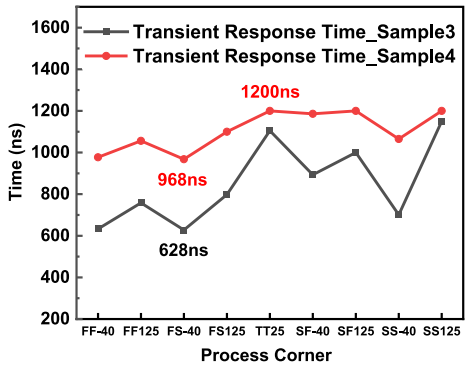

FIGURE 7. Robustness simulation results of the proposed circuits over all process and temperature corners.

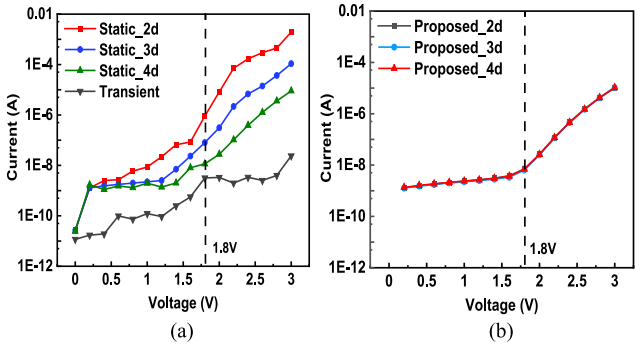

FIGURE 8. DC test results of all investigated circuits: (a) traditional circuits, (b) proposed circuits.

TABLE 3. Comparison of test results of Ileak at high temperatures.

Temperature	25 °C	80 °C	125 °C
Transient	2.6 nA	88.2 nA	674.8 nA
Static_2d	6.8 μA	11.7 μA	25.4 μA
Static_3d	102.3 nA	748.3 nA	5.7 μA
Static_4d	11.5 nA	319.5 nA	1.8 μA
Proposed_2d	7.1 nA	109.3nA	742.6nA
Proposed_3d	6.9 nA	104.2 nA	728.9 nA
Proposed_4d	6.8 nA	98.6 nA	702.3 nA

can maintain transient response time of 628 ns at the worst PVT corner, ensuring that the majority of current discharge is completed under HBM events, and the circuit is still robust at all PVT corners. As mentioned above, the size of Mn2 can be adjusted (in sample4) to ensure that the proposed circuit provides transient response time of nearly 1μs at the worst corner, then the circuit can safely complete ESD current discharge. The maximum transient response time of sample4 is 1.2 μs since the maximum duration of the HBM pulse is limited [22]. In fact, the transient response time of the circuit would be longer under other ESD pulses. As a result, the worst corner for proposed circuit is FS × −40°C. Therefore, the proposed circuit has greater flexibility and robustness at all PVT corners.

III. SILICON DATA VERIFICATION

All investigated circuits are verified in a 28-nm CMOS process. DC, Fast Power-up, HBM and TLP tests are performed to confirm the previous simulation results.

A. DC TEST RESULTS

DC test results are depicted in Fig. 8. These test results are generally consistent with the simulation results in Fig. 3. Both the proposed circuit and transient circuit have an I_{leak} of nA level at 1.8 V, and their I_{leak} are much lower than that of the corresponding static one in Fig. 8(a). The I_{leak} of the proposed circuit is 7 nA at 1.8V normal supply condition. Aside from these test results, DC tests at temperatures of 80 °C and 125 °C are also performed and extracted I_{leak} are compared in Table 3. Table 3 compares the test results of all investigated circuits with I_{leak} at 1.8 V. The superior I_{leak} performance of the proposed circuit over that of the static one is fully verified in this table. Besides, I_{leak} of proposed circuits are basically slightly higher than those of the transient one at the same temperature due to the additional devices in the trigger circuits. Moreover, the proposed circuits with different number of diodes also maintain better consistency at high temperatures compared to the static circuits. Because the proposed circuit is employed to discharge A-level high current, the 700nA-level leakage current at 125°C is acceptable for ESD power clamp circuits. Therefore, the proposed circuit also has superior I_{leak} performance at high temperatures.

B. FAST POWER-UP TEST RESULTS

Fig. 9 depicts the V_{clamp} plot with a 10ns rise time and 1.8 V voltage pulse. The test results are in highly consistent with the simulation results in Fig. 4(a). The false triggering duration of transient circuit is 20-30 ns, while the proposed circuit is free from false triggering. The current of the proposed circuit decreases after a 3.4 mA peak and eventually maintains at the 7-nA level. It is concluded that the proposed circuit is free from leakage issue under fast power-up pulse disturbances.

C. TRANSIENT HBM TEST RESULTS

Fig. 10 depicts the V_{clamp} of the investigated circuits under a 1 kV HBM pulse. The test results in Fig. 10 are in line with the simulation results above. In Fig. 10(a), an overshoot effect can be found in the actual test, where the BigFET turns on and then quickly clamps V_{clamp} to a low voltage for discharge. The overshoot is not a concern for thick-oxide devices at 1.8V power domain.

The proposed circuit discharges more charge and complete the entire discharge process earlier, thus clamping V_{clamp} to 0 V earlier. The proposed circuit safely and efficiently discharges ESD current at a lower V_{clamp} than the static

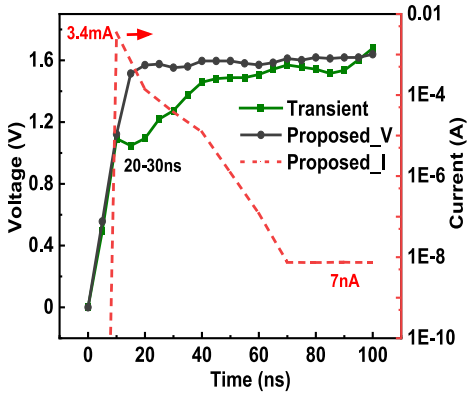

FIGURE 9. Fast power-up test results of all investigated circuits.

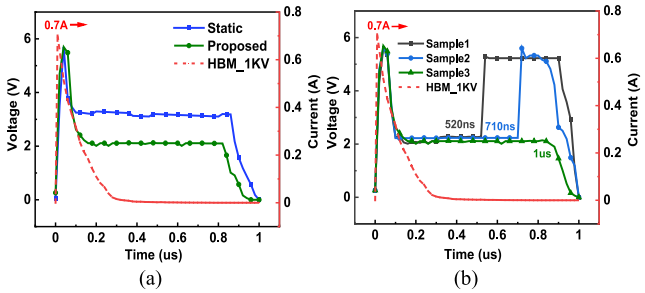

FIGURE 10. Transient test results of the investigated circuits: (a) under a HBM like current pulse, (b) three samples of proposed circuits with different transient response time under the same pulse.

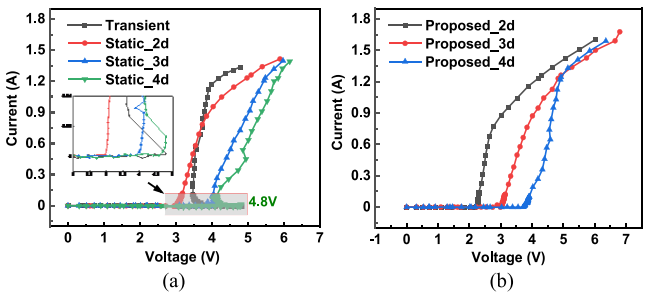

FIGURE 11. TLP test results of all investigated circuits: (a) traditional circuits (b) proposed circuits.

one. The proposed circuit achieves transient response time of μs level with an RC time constant of 10 ns, demonstrating its quite high area efficiency. In agreement with Fig. 6, the three samples of the proposed circuit achieve similar transient response time in the test results.

D. TLP TEST RESULTS

The TLP tests are performed using transient pulses with 10 ns rise time and 100 ns pulse width. Fig. 11 depicts the results of all investigated circuits.

In Fig. 11(a), the traditional transient clamp exhibits a ggNMOS-like TLP I–V curve since the parasitic BJT triggering of BigFET. In the TLP test, static I-V data is usually obtained as time of 70-90 ns. The RC time constant of the transient circuit is only 10 ns, for the time period of

TABLE 4. Summary of TLP test results.

Circuit Type	V_{t1} (V)	V_h (V)
Transient	4.8	3.4
Static_2d	2.9	2.9
Static_3d	3.8	3.8
Static_4d	4.8	4.1
Proposed_2d	2.2	2.2
Proposed_3d	3.0	3.0
Proposed_4d	3.8	3.8

extracting I-V data, Gate is logic low and BigFET turns off. So the current discharge of transient circuit relies entirely on the parasitic BJT trigger, which is not efficient and the modulation effect of RC is removed. Vt1 variations of static clamps with respect to different diode numbers are clear in Fig. 11(a). Due to the weak V_G response in Fig. 1(b), the snapback triggering behavior of the static clamp with four diodes is dominated by the parasitic BJT of the BigFET. The nonlinear TLP I-V curves of the static circuit make it difficult to adjust the triggering behavior of the BigFET.

In Fig. 11(b), the proposed circuit achieves adjustable V_{t1} with low I_{leak}. V_{t1} of each proposed clamp is lower than that of the static one under the same diode number, which is benefited from the properly sized R_3 in Fig. 2. As the TLP voltage increases, the main discharge path gradually transfers from channel discharge to parasitic BJT discharge. It is beneficial to turn on the BJT in high current conditions, which can improve discharge capability and realize higher level of protection. Therefore, at higher TLP voltages, the R_{on} of the BigFET tends to be consistent, independent of the number of diodes. For the proposed circuit, V_{t1} can be adjusted linearly by changing the number of diodes. It is clear that reduced diode-number clamps are suitable for more advanced processes where the ESD design windows are narrower. Table 4 presents the summary of TLP test results. V_{t1} and V_h denote the triggering voltage and holding voltage, respectively. It is worth noting that the proposed circuit has high linearity of V_{t1} control, which is superior to the static circuit. Moreover, the proposed circuit has better ESD design window compatibility with respect to the transient one.

Transient V_{clamp} of different circuits are extracted from TLP test results and compared in Fig. 12. The exhibited clamping voltages correspond to the TLP precharge voltage, V_{pre}, of 5V. The V_{pre} defines the voltage that TLP pulse generator precharges to the transmission line and represents the output energy level of TLP pulse generator. Higher V_{pre} means higher output energy of TLP pulse generator. For Fig. 12, the comparison at the same V_{pre} is fair and objective. The transient clamp exhibits unacceptable performance with its V_{clamp} being the trigger voltage V_{t1}, which is in

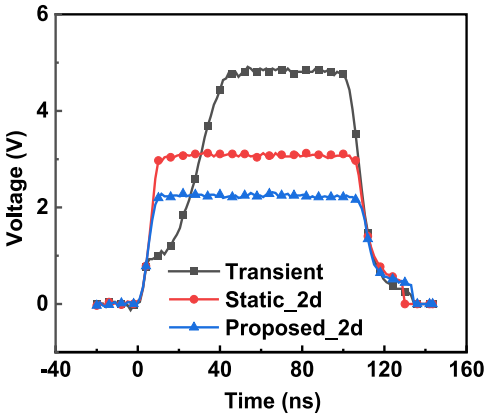

FIGURE 12. Transient V_{clamp} comparisons under the TLP V_{pre} of 5 V.

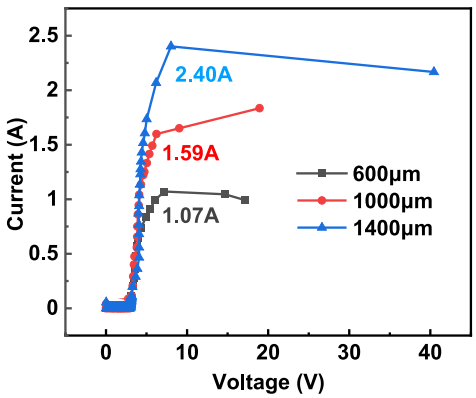

FIGURE 13. TLP test results with different BigFET widths of proposed circuits.

line with the static I-V data in Fig. 11(a). The response time of the transient circuits is only 10-20 ns, which is completely insufficient for the safe discharge of ESD current. The proposed circuit with two diodes achieves the best performance since V_{clamp} of the transient circuit is still too high and the static circuit with two diodes stays basically higher than the proposed one. It should be noted that the tested performance of the proposed circuit in Fig. 12 is also compliant with the ESD design window. The proposed circuit can safely discharge current at a lower V_{clamp}. These results are also in line with the HBM simulation results in Fig. 5(b).

Fig. 13 shows the TLP test results of the proposed circuit with different BigFET widths. As the width increases, Ron becomes lower and I_{t2} becomes higher, which is in agreement with the expectation. Different protection levels are achieved by changing MOS widths, which meets different protection scenarios. The circuit designers can select the appropriate BigFET widths for the application requirements. The trigger circuit parts of the proposed clamp can keep the same structure.

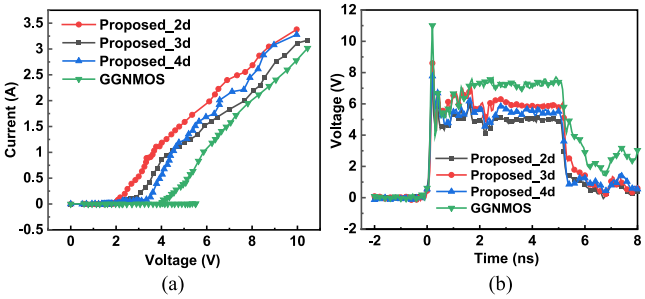

FIGURE 14. VF-TLP test results of proposed circuits and GGNMOS: (a) I–V curves. (b) Transient clamping voltages.

E. VF-TLP TEST RESULTS

Fig. 14 shows very fast TLP (VF-TLP) test results using transient pulses with 100-ps rise time and 5-ns pulse width. Transient clamping voltages under the V_{pre} of 100 V are compared in Fig. 14(b). The same V_{pre} means that VF-TLP pulse generator provides the same energy level. Fig. 14(a) depicts test results of proposed clamps with different number of diodes and ggNMOS. It should be noted that the proposed circuit and ggNMOS maintain the same MOS width. It can be inferred from Fig. 14(a) that the adjustable V_{t1} with low I_{leak} is also valid in CDM events. Above the current of ~3 A in Fig. 14(a), the curves of proposed circuits are undistinguishable from that of ggNMOS, confirming the dominant parasitic BJT discharge mechanism in the high-current stage as has been analyzed above. The trigger voltage for ggNMOS is ~6 V, which is too high for the ESD design window corresponding to this process and is unacceptable. In Fig. 14(b), the proposed circuits show voltage overshoot, which could be caused by the slow turn-on speed of static circuit section. The proposed circuit still achieves fast voltage clamping in 2 ns to ensure safe discharge by optimizing the turn-on speed. Initial overshoots of proposed circuits are lower than that of ggNMOS, which verifies the suppression from R_3 and the parasitic drain to gate capacitor of the BigFET in Fig. 2. After the initial overshoots, the clamping behaviors of proposed circuits with diode-number variations are consistent, confirming the functionality of the TC. In addition, the proposed circuits have lower clamp voltage compared to ggNMOS, ensuring safe discharge of ESD current even under CDM events.

F. PERFORMANCE SUMMARY OF PROPOSED CIRCUIT

Performance summary of the proposed clamps with different BigFET widths are presented in Table 5. Silicon-based test results are the source of data. In this table, the proposed clamp with 2 diodes is chosen as a representative sample.

The leakage current under the normal power supply remains essentially consistent in the low range of less than 10 nA for the three different BigFET widths, even under CDM events. The leakage current is slightly lower in the VF-TLP condition, which could be that tested circuit recovers to initial state more rapidly after each pulse. The VF-TLP

TABLE 5. Performance summary of the proposed clamp with different BigFET width.

BigFET Width (μm)	Leakage current @1.8V	It2@TLP	It2@VF-TLP	HBM Level (kV)	Failure type
600	5nA (TLP); 4nA (VF-TLP)	1.07A	2.50A	2.0	Short-circuit failure
1000	7nA (TLP); 6nA (VF-TLP)	1.59A	3.83A	3.1	Short-circuit failure
1400	8nA (TLP); 8nA (VF-TLP)	2.40A	4.92A	4.2	Short-circuit failure

TABLE 6. Performance comparisons of the proposed clamp with the representative prior arts.

Reference	[4]	[6]	[9]	[10]	This Work
Process	40 nm	65 nm	0.18 μm	BCD Process	28 nm
I_{leak}	28.70 nA	14.83 nA	N/A	31.0 nA	8 nA
TC Area-reduction Ratio	> 20% over the baseline circuit	~47% over the baseline circuit	No Reduction	No Reduction	~ 90% over the baseline circuit
Transient Response Time	μs - level	Continuous Response	100 ns	μs - level	μs - level
Fast Power-on Issue	Immune	Immune (But has sustained leakage issue)	Immune	Immune	Immune
Adjustable V_{t1} with Low I_{leak}	Not Achieved	Achieved	Achieved	Not Achieved	Achieved

has less thermal accumulation in the test circuits due to the shorter pulse widths. Therefore, I_{t2} under VF-TLP test will be higher than that of TLP test [23], [24]. The circuit failures come from short failures, mainly induced by the thermal accumulation of the BigFET [25]. Optimal HBM-level width-scaling characteristics are achieved in this table due to the efficient TC of the proposed circuits. The levels of HBM and I_{t2} represent the degree of ESD protection. The HBM values are measured on HBM test equipment. The proposed circuit provides the complete design guidance for circuit designers. The circuit designers can choose the suitable size to ensure reliable ESD protection according to the requirements of application.

G. PERFORMANCE COMPARISONS WITH PRIOR ARTS

Performance comparisons of the proposed clamp with the representative prior arts are presented in Table 6. Silicon-based test results are the main choice for data collection. Regarding TC area-reduction ratio in Table 6, the baseline circuit for comparison is the traditional transient circuit with the same transient response time. Prior arts also make comparisons based on the baseline circuit. Over 90% area reduction mostly benefits from the extremely low RC time constant of the proposed circuit. The proposed circuit and design parameters are based on wafer-level test conditions with standard ESD pulse specifications. Therefore, based on different test and application scenarios, the RC time constant can be increased. In these scenarios, the increased RC area leads to a smaller TC area-reduction ratio. The proposed circuit remains significant area superiority over traditional circuits. The fast power-on issue is to verify the immunity of the clamp circuits under a fast power-up pulse with 10 ns rise time. The very fast power-up pulse is employed to characterize the performance of the circuit under extreme power-up conditions [7], [9], [19], [20]. Therefore, the proposed circuit would not be triggered to discharge current under these fast power-up conditions, which provides a great advantage for fast startup of core circuits.

By co-optimizing transient and static trigger mechanisms, the proposed hybrid circuit has higher area efficiency than most prior arts. The transient response time of proposed circuit at the μs level is sufficient for ESD current discharge. As well, the circuit proved to have strong false trigger immunity in the worst case of fast power-on pulses. In addition, proposed circuit also has lower leakage current of less than 10 nA than most prior arts. According to the above test results, the proposed circuit has high linearity of V_{t1} control with low I_{leak}. By the comparisons in Table 6, the proposed circuit performs better than prior arts, which provides a better choice for on-chip ESD protection design.

IV. CONCLUSION

The advantages of the proposed circuit compared to transient, static circuits are verified in this paper. Test results in a 28-nm CMOS process have successfully verified that the proposed circuit is capable of performing strong false-trigger immunity under the worst-case fast power-on pulse. The new circuit with 10 ns RC time constant achieves transient response time at the μs level, significantly saving the layout area and cost. Compared to traditional transient circuit with same response time, the proposed one achieves a TC area reduction of over 90%. Besides, the circuit has a low I_{leak} of less than 10nA with different BigFET widths, demonstrating its superior low power performance. Moreover, detailed performance summary of the proposed clamp with different BigFET widths are addressed in this paper, which provides complete design guidance for circuit

designers. Detailed comparisons of the proposed circuit with prior arts verify its superiority. Finally, this circuit provides an excellent solution for on-chip ESD protection.

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