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BEOL Integrated Ferroelectric HfO_2-Based Capacitors for FeRAM: Extrapolation of Reliability Performance to Use Conditions

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ABSTRACT Si doped HfO_2 based ferroelectric capacitors integrated into Back-End-Of-Line (BEOL) 130 nm CMOS technology were investigated in regard to critical reliability parameters for their implementation in non-volatile one-transistor one-capacitor ferroelectric random-access memory applications. The assessed reliability parameters are electric field, capacitor area, and temperature and are evaluated on single and parallel structured capacitors to understand their respective impact on wake-up, fatigue, imprint, and retention.

INDEX TERMS BEOL, ferroelectric, HfO_2, reliability.

I. INTRODUCTION

Ferroelectric HfO_2 based non-volatile memory devices have increasingly gained attention during this past decade due to their high-performance operation and CMOS process compatibility. Comparing one-transistor-one-capacitor ferroelectric random-access memory (1T1C FeRAM), a ferroelectric field-effect transistor, and ferroelectric tunnel junctions, FeRAM has the advantage of improved reliability, as well as low power and disturb-free operation [1]. However, so far, most reliability characteristics have been evaluated on large capacitor structures (>100 μm^2) [2]. Here, for the first-time, wake-up, endurance, retention, and imprint characteristics are evaluated with target sizes, voltages, and temperatures in mind.

II. FABRICATION

Metal-ferroelectric-metal (MFM) capacitors were fabricated as single capacitors or arrays of 1290 capacitors connected in parallel consisting of TiN top and bottom electrodes and a 10 nm thick ferroelectric corresponding to a 1.5 % Si doped HfO_2 (HSO) layer (Fig. 1); similar to formerly reported structures [3]. A thermal budget of 450°C was sufficient to crystallize the ferroelectric layer and obtain high polar phase fractions. The fabricated planar capacitor structures ranged from an area of 7850 down to 0.047 μm^2. Of these, the smallest structure is comparable to a DRAM capacitor array at the 20 nm technology node; as explained ahead. Starting with the assumption that a comparable sense amplifier can be used to sense the charge difference determined by the two possible memory states, the two technologies can be equated by:

$$Q = A_{FeRAM} \cdot 2 \cdot P_r = C \cdot U = A_{DRAM} \cdot \varepsilon_0 \cdot \varepsilon_r \cdot U/d \quad (1)$$

with capacitor area A, remanent polarization P_r, dielectric constant ε_0, ε_r, voltage U, and the thickness of the capacitor dielectric d. For a DRAM capacitor, an aspect ratio of 50:1-100:1 was reported for current technologies below 20 nm [4], resulting in a capacitor area of about 0.24 μm^2 with a capacitance of about 10 fF/cell. Assuming a dielectric layer thickness of 6 nm, ε_r of 40, and an applied voltage of 0.5 V for DRAM and a P_r of about 15 $\mu C/cm^2$ for FeRAM, (1) leads to an area ratio between DRAM and FeRAM of

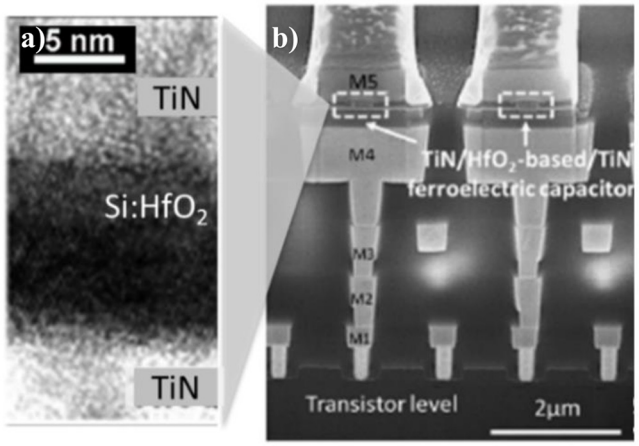

FIGURE 1. **Cross-sectional (a) HRTEM and (b) SEM imaging of an HSO BEOL integrated ferroelectric capacitor.**

$A_{FeRAM}/A_{DRAM} \sim 1/10$. Accordingly, a capacitor area of 0.024 μm^2 would be sufficient for an FeRAM capacitor; which is only half as small as the smallest structure evaluated in this work. Furthermore, it is also worth mentioning that by evaluating the smallest structures in the parallel array configuration in order to improve the signal-to-noise ratio, some properties such as remanent polarization are unaffected as they are normalized to the total area but, other properties such as cycles-to-breakdown and time-to-failure will reflect the earliest fail-event of the entire array.

III. WAKE-UP AND FIELD CYCLING ENDURANCE

Important reliability topics for FeRAM capacitors that determine their electric field cycling stability are wake-up, fatigue, and breakdown. A 100 kHz square cycling signal with a periodic, 50 μs segmented, triangular pulse structured PUND measurement was used to characterize cycling stability.

Significant wake-up was observed in all of the array-structured devices with areas ranging from 0.248 down to 0.047 μm^2. Fig. 2a presents an example of this behavior for a device with a 0.047 μm^2 area. Wake-up effects, also observed as the de-pinching of the P-V hysteresis loop, are mainly attributed to field-induced phase transitions, de-pinning of domains due to charge movement, interface breakdown, or ferroelastic switching [5]; all of which are defects within the ferroelectric layer.

By comparing the different capacitor areas in more detail, we see that, assuming a typical HfO_2 grain size of 30 nm, the aforementioned capacitors would consist of around 350 down to 70 grains with approximately 15% to 33% edge grains, respectively. Accordingly, the number of edge grains would be large enough to influence wake-up and fatigue through edge effects during field cycling. Additionally, relatively higher device structuring defects in the smaller devices due to a smaller surface to edge ratio could also lead to earlier degradation. That said, only an increase in polarization (likely related to an enhanced noise level for smaller devices) was observed for the smaller devices but this did not visibly

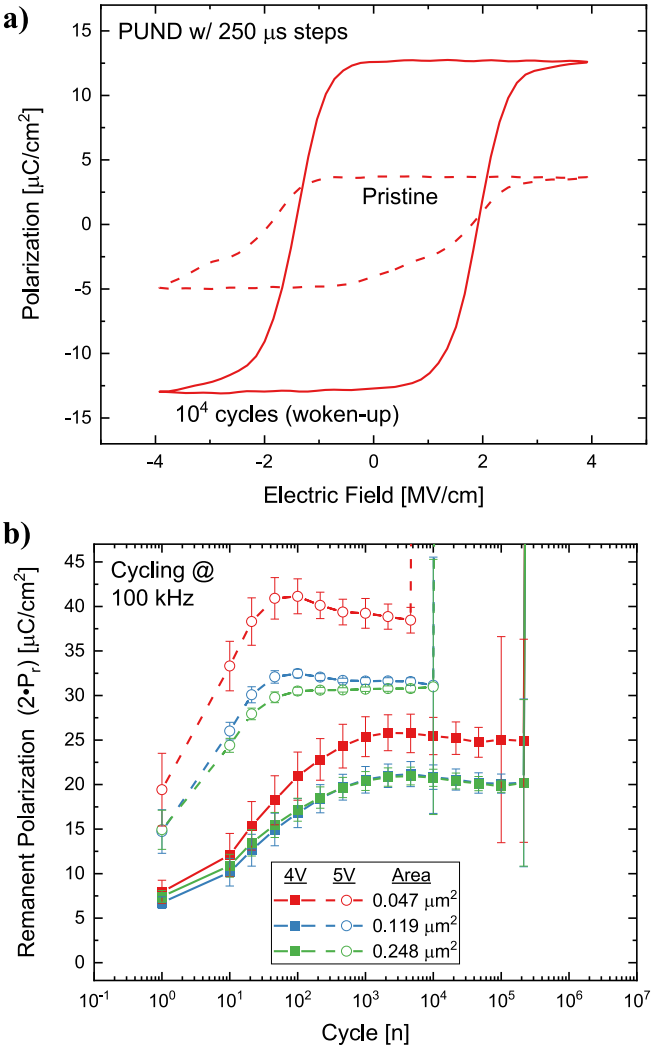

FIGURE 2. **(a) Polarization vs. electric field response of an array of HSO BEOL integrated ferroelectric capacitor with an area of 0.047 μm^2 in a pristine and woken-up (after 10^4 cycles) state. (b) 2· P_r during field cycling for different voltages and capacitor areas for the parallel capacitor arrays.**

impact the device performance (Fig. 2b). Therefore, it can also be said that no significant difference in the wake-up behavior is present for different capacitor areas and, consequently, edge effects can be neglected for wake-up. Similarly, fatigue, that is, the reduction in remanent polarization with field cycling for high number of field cycles, seems to be comparable for different capacitor areas and, since the number of grains per capacitor is still reasonably high, no impact of grain or domain statistics is visible.

In contrast, if defects within the ferroelectric layer do dominate, cycles-to-breakdown (i.e. field cycling endurance) would be improved for smaller devices. Fig. 3a shows the area dependence of the number of cycles to breakdown for three different electric field amplitudes for the single capacitor structures with an area range from 7850 down to 0.3μm^2. It can be seen that a reduced capacitor size by a factor of

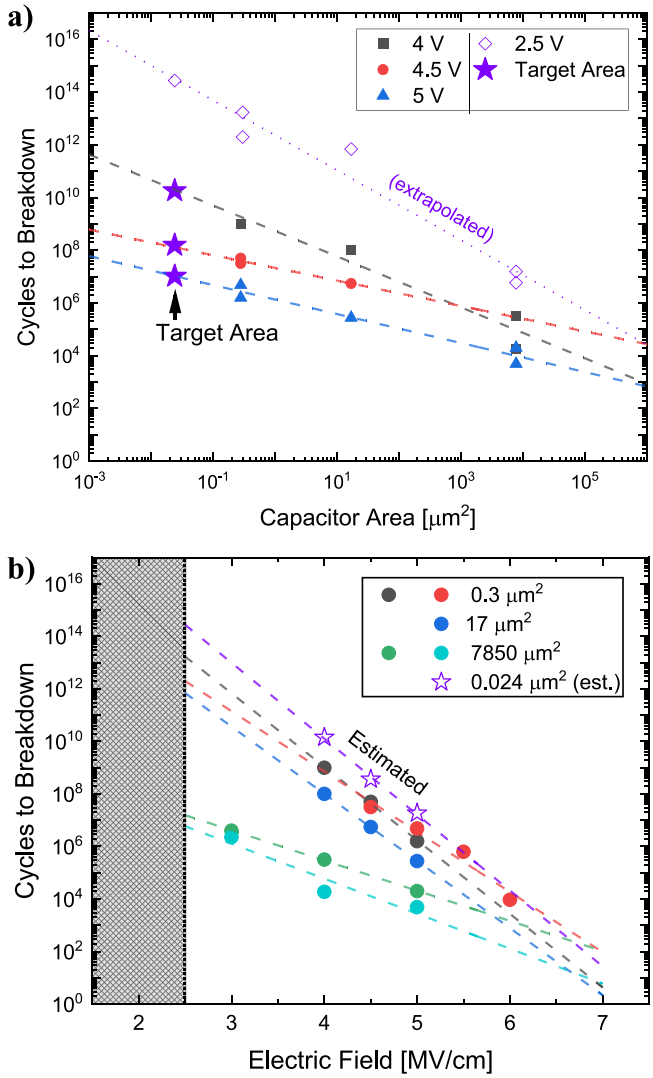

FIGURE 3. **Cycles to breakdown vs. capacitor area and (b) cycles to breakdown vs. electric field cycling amplitude for different single capacitor areas and with an extrapolation to the estimated target capacitor area and electric field amplitude.**

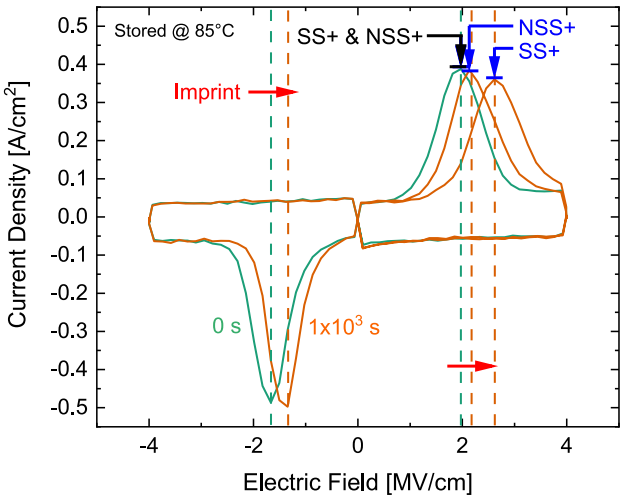

FIGURE 4. **Current density vs. electric field curve displacement after 10^3 s during a retention measurement of an HSO BEOL integrated ferroelectric capacitor.**

five leads to improved field cycling endurance and, therefore, it is expected that bulk regions accelerate breakdown compared to edge zones. This concurs with typical dielectric breakdown [6].

With the obtained cycles-to-breakdown trends from Fig. 3a, one can extrapolate to the target capacitor size of 0.024 μm^2. Furthermore, one can look into a broader electric field cycling range (Fig. 3b) and, with the estimated values for the target capacitor area, extrapolate to an operating electric field of 2.5 MV/cm [7], [8] where a cycles-to-breakdown near 10^{15} is obtained, this at room temperature. In a recursive manner, data extrapolated to 2.5 MV/cm in Fig. 3b are added to Fig. 3a to demonstrate the impact of reducing the maximum applied field on cycling endurance.

The extrapolated value of cycles-to-breakdown for HSO is already significant for meeting field cycling endurance specifications [9]. That said, standard product qualification tests require an evaluation at higher temperatures (e.g. 85°C) determined by the goal application [10]. At higher temperatures, a reduced field cycling endurance (e.g. of at least one decade at 75°C [11]) can be hindered by material improvements such as replacing HSO for $Hf_{0.5}Zr_{0.5}O_2$ as in [12].

Overall, capacitor area scaling down to the target capacitor size is expected to be non-detrimental to electric field cycling reliability.

IV. IMPRINT AND RETENTION

Another main reliability concern for FeRAM capacitors is polarization retention. Typically, three phenomena influence retention loss: thermal depolarization, depolarization by a non-fully compensated depolarization field and imprint. Of these three, imprint, which is a preferential polarization orientation defined by a lower coercive field, has been shown to be the most critical factor of the three [13] and is expected to be caused by charge injection and/or charge/ionic movement during storage of the device [14].

Imprint and retention were evaluated regarding area and temperature dependence. For this analysis, the electric current response to electric field of a ferroelectric capacitor is monitored after different storage times (see Fig. 4). Only the parallel HSO capacitor arrays of 1290 capacitors with individual capacitor areas of 0.248-0.047 μm^2 were analyzed. Three retention states (as described in [15]) for both voltage polarities were evaluated with respect to storage time: same state (SS), new same state (NSS), and opposite state (OS), as seen in Fig. 5a. Each of these states has unique contributions from the three phenomena that influence retention loss, where SS reflects a combination of all three phenomena, NSS reflects primarily depolarization-field induced polarization loss (when compared to SS) and OS reflects primarily

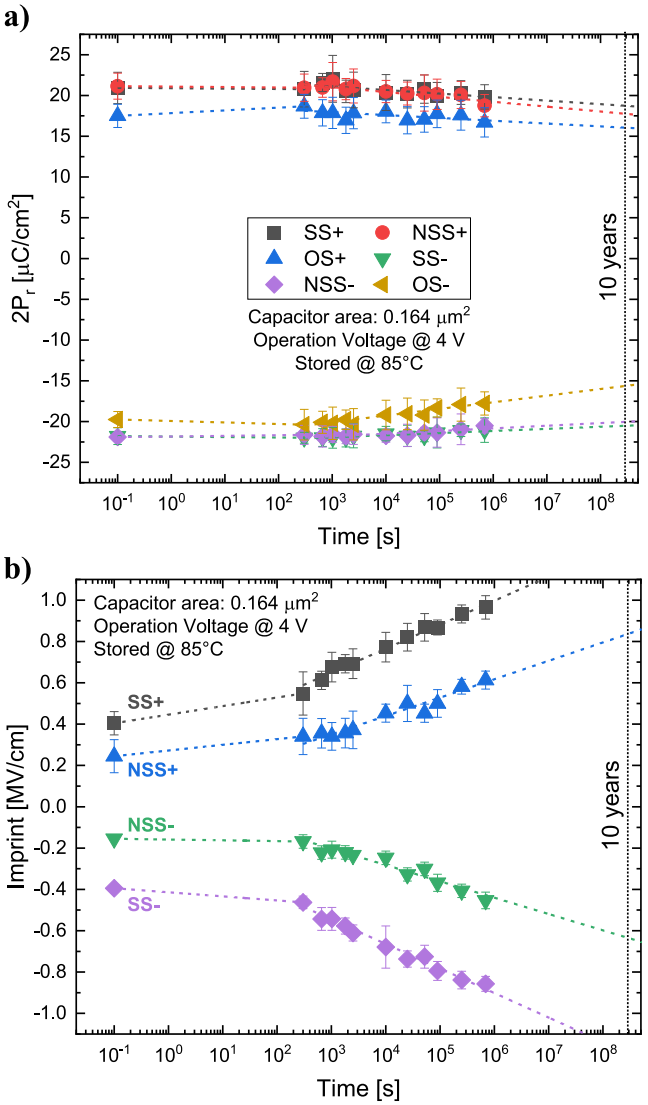

FIGURE 5. **(a) Remanent polarization (2· P_r) vs. time for three types of retention states (SS, NSS, and OS) and (b) imprint vs. time of a retention measurement with the variation between SS and NSS states due to charging.**

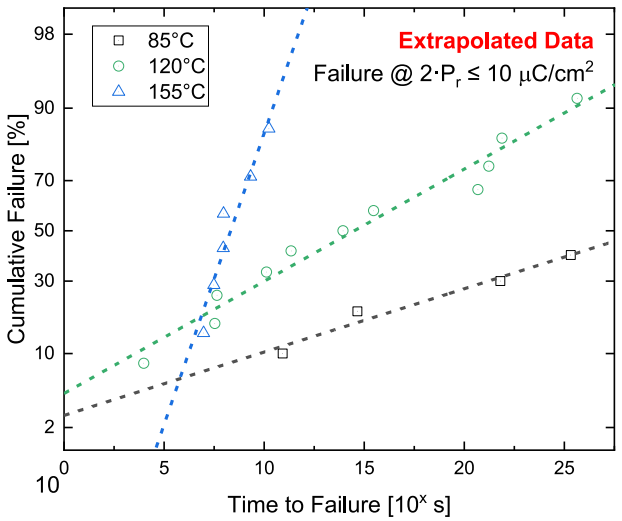

FIGURE 6. **Cumulative failure vs. time-to-failure (TTF) during retention measurements of HSO BEOL integrated ferroelectric capacitors in parallel with different storing temperatures (on a Gaussian probability plot).**

depolarization loss as a result of increased imprint. In some cases, for simplicity, OS is the state considered when not mentioned otherwise. This simplification is justified by the faster degradation of the OS state compared to the other two retention-metrics (see in Fig. 5a) which, in turn, matches the initial assumption regarding the relation of retention to imprint. Typically, about 72 capacitor arrays (6 per process condition) were analyzed in parallel to understand the statistical relevance of the obtained results.

For a non-volatile memory device, it is important to retain the memory state up to 10 years at elevated temperatures (85°C) [9]. Retention measurements were thus performed over several hours or days and then extrapolated to 10 years (Fig. 5). More so than remanent polarization loss (see blue arrows of Fig. 4), an increasing shift of the switching peak through time (see red arrows in Fig. 4) allows for the calculation of the imprint of the capacitor, defined as:

$$Imprint = \frac{E_{c+} + E_{c-}}{2} \tag{2}$$

where E_{c+} and E_{c-} are the coercive fields and considered here as the electric field at which a maximum in measured electrical current is observed for a positive and negative bias respectively. Since the measurement pulse sequences used can present two pulses with identical polarity for which separate coercive fields can be extracted, two imprint values calculated, $SS_{Imprint}$ and $NSS_{Imprint}$, corresponding to their respective retention state (Fig. 5b). Additionally, differences found in the slopes of the extrapolated trends for imprint in Fig. 5b (defined here as the imprint rate) may indicate time-dependent charging effects.

Despite the variations among the different retention states and their respective imprint values, the variation for a single state with respect to the multiple essays performed exhibited a normal Gaussian distribution behavior when extrapolating for time-to-failure (TTF), considered here as reaching a $2{\cdot}P_r$ lower than 10 μC/cm^2 (Fig. 6).

Regarding the different capacitor areas, stable behavior in retention was observed. The retention stability is indicated by a lack of change with respect to TTF or increase in imprint for the different capacitor areas which were evaluated (Fig. 7a). Since retention for this work is mainly being attributed to charge movement, it is noteworthy that smaller structures with more significant edge effects did not appear to degrade device performance. This would match the trend identified in Section III for electric field cycling endurance.

The impact of increased baking temperature on the imprint in the devices during a retention measurement is presented

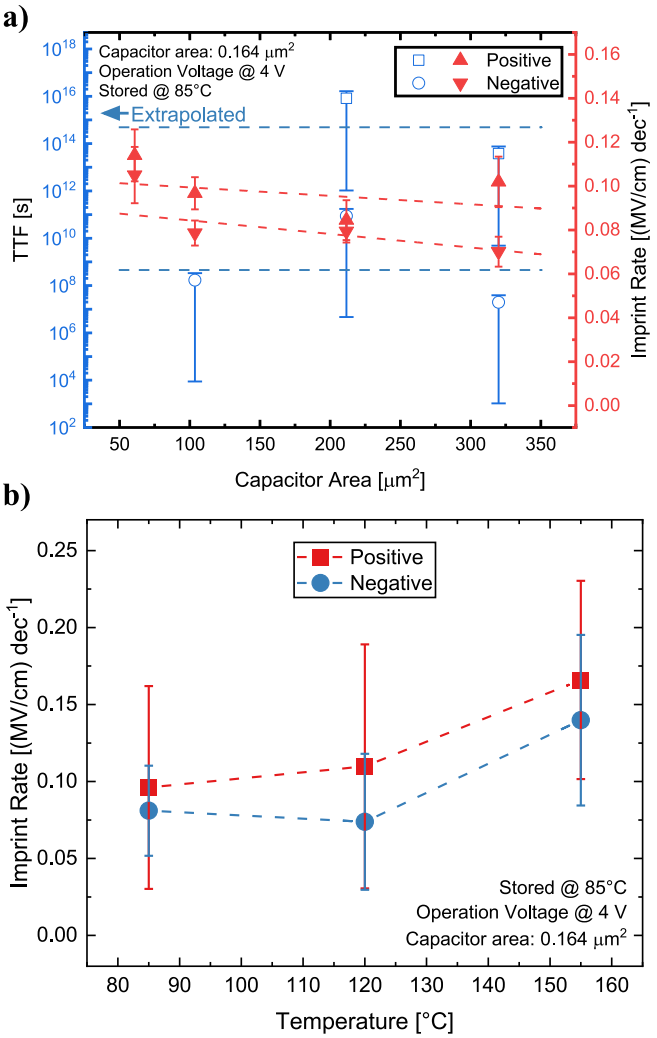

FIGURE 7. **(a) Time-to-failure (TTF, left axis) and imprint rate (right axis) during retention measurements of HSO BEOL integrated ferroelectric capacitors in parallel as a function of the capacitor area and (b) imprint rate as a function of temperature in retention measurements of HSO BEOL integrated ferroelectric capacitors in parallel, comparing positive and negative stored states.**

in Fig. 7b. Increasing the temperature from 85 to 120°C had a lower impact on retention degradation speed than a further increment to 155°C, which is true for both voltage polarities. In addition to imprint, higher baking temperatures also degraded the retained polarization quicker. This impact of incremental baking temperatures on the polarization state may be analyzed by a short-term (<1000 s) and long-term (>1000s) logarithmic fitting as shown previously in [14]. This allows for the determination of two activation energies in accordance to an Arrhenius relation, a ~0.4 eV short-term activation energy and a ~0.3 eV long-term activation energy. These values fall within the range of published results for $PbZrTiO_3$ (PZT) based capacitors, where an initial 0.28 eV activation energy and a 0.11 eV long-term activation energy have been reported [13]. It is worth mentioning that only the relation with respect to temperature,

TABLE 1. **Reliability evaluation of HSO for FeRAM.**

	Wake-Up	Cycles to Break.	Imprint	Retention
Area (↓)	-	↑	-	-
Temperature (↓)			↓	↑
Electric Field (↓)	-	↑		

and not the actual magnitude of degradation, is being compared between the two materials. Nevertheless, the trends indicate similarities in the general mechanisms for retention degradation between HfO_2 and PZT based capacitors, mainly attributable to charge injection from the electrode and charge/ionic movement within the dipole field of the ferroelectric layer.

V. SUMMARY

Key reliability parameters for the necessary validation of HSO for the application of this material as a ferroelectric layer in capacitors for 1T1C FRAM technology were investigated (Table 1) [16]. Lateral scaling of the devices showed no detrimental effect on the wake-up, fatigue, imprint and retention behavior observed for larger devices. This relates closely to the lack of edge effects. In contrast, an improvement in field cycling endurance was observed and is possibly due to the net reduction in defects within the ferroelectric layer merely as a result of having a smaller area and by which the probability of having breakdown event is reduced. Additionally, further scaling toward smaller capacitor sizes is estimated to allow for a field cycling endurance near 10^{15}, which is already significant but can be further improved with a proposed material optimization. Finally, retention behavior was only influenced through temperature and showed a similarity in degradation characteristics with what has been previously reported for PZT.

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