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# A Retina-Inspired Image Sensor Array Based on Randomly-Accessible Active Pixel Sensor

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**ABSTRACT** Human retina is by nature a superior image sensor with a high sensitivity, wide dynamic range as well as low power consumption. In this paper, an image sensor array based on randomly-accessible active pixel design is studied where to mimic retinal photoreceptor, a photodiode-body-biased MOSFET (PD-MOS) with an adjustable gain of 10-420000 (higher than $10^5$), a wide dynamic range of 140 dB and a spectral responsibility of 3-25000A/W from near UV to near IR wavelengths, is proposed. The image sensor array can capture images under light intensity ranging from 10nW/cm$^2$ to 3mW/cm$^2$ and its dynamic range is approximately 110dB.

**INDEX TERMS** Retina, photoreceptor, randomly-accessible active pixel sensor, wide dynamic range, adjustable gain.

## I. INTRODUCTION

Human retina is the best known natural photosensor with high sensitivity and wide dynamic range. Besides, what is less well-known but more important characteristic is that its sensitivity is also tunable for different levels of light exposure since different cells in human retina take different roles in processing photons. For instance, rod cells mainly work in scotopic vision but with a high sensitivity so that the weak light of $10^{-6}$mL can be sensed. While cone cells mainly play a role at photopic conditions with a wide dynamic range of over 180dB [1], [2]. However, such demanding requirements can hardly be met by any conventional CMOS active pixel image sensors (APS), which generally have a dynamic range of approximate 40-70 dB with a non-adjustable photo-electron conversion gain or sensitivity [3], [4], [5], [6], [7], [8], [9]. Additionally, it has been revealed that the response of the primate retina to light is a logarithmic function while the response of the conventional CMOS APS is in a linear fashion. In order to mimic the superior performance of the primate retina, especially the wide dynamic range, a logarithmic response active pixel sensor was proposed [10], [11].

The logarithmic response comes from the sub-threshold operation of the load transistor in connection with the photodiode and as a result a wide dynamic range of greater than 120dB can be obtained. As such, integrating the photo-generated charges during the photoelectric conversion process becomes unnecessary and the pixel reset is no longer needed, thus, reading and addressing the pixel can be random, enabling continuous operation and improving the reading speed.

However, its signal to noise ratio is relatively low when exposed to low-level light and due to its randomly-accessible characteristic, the correlated double sampling technique that is frequently used by the conventional CMOS image sensors to reduce the fixed pattern noise cannot be used in the logarithmic pixel [12], [13], [14], [15].

Since the randomly-accessible active pixel sensor which has been proposed by our group can resolve the issues mentioned above, in this work, an image sensor array chip composed of this new pixel circuit which based on our novel photodiode-body-biased MOSFET (PD-MOS) is studied and the performances of the PD-MOS, pixel circuits and such retinal photoreceptor-like image sensor array are characterized and analyzed in detail.

## II. MODELING, CHARACTERIZATION AND DESIGN

### A. MODELING AND SIMULATION

The PD-MOS in the randomly-accessible pixel was proposed by our group in EDTM 2019 [16]. It is formed by connecting

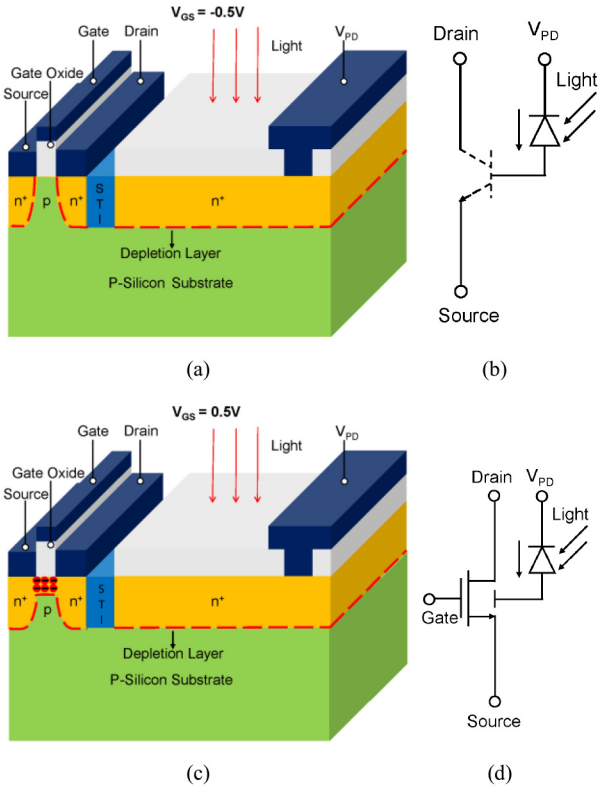



**FIGURE 1. (a) Schematic diagram of PD-MOS working in BJT mode; (b) Equivalent circuit of PD-MOS working in BJT mode; (c) Schematic diagram of PD-MOS working in sub-threshold mode; (d) Equivalent circuit of PD-MOS working in sub-threshold mode.**

the cathode of a photodiode (PD) to the substrate of a N-channel MOSFET via a common lightly-doped p-type substrate, as schematically shown in Fig. 1. When illuminated by the light, electron-hole pairs are created in the PD and separated by the reverse bias and built-in potential. That is, electrons drift to the cathode of the PD and holes are forced to accumulate in the lightly-doped p-type substrate and continue to diffuse to the back channel of MOSFET, inducing a positive body bias which is known as light-induced body bias effect.

In practical applications, the drain terminal of the MOSFET and the cathode of the PD are generally biased with adequate positive voltages. Through regulating the biases between the gate and source terminals ($V_{GS}$) of the MOSFET, PD-MOS can work in two different modes. If $V_{GS}$ is lower than $V_{TH}$, the inversion in the channel of the MOSFET does not occur, the p-n junction between the source and the lightly-doped p-type substrate is weakly forward-biased due to the light-induced body bias effect, and with a higher drain voltage, the p-n junction between the substrate and the drain is reverse-biased. Therefore, in this scenario, the MOSFET acts like a bipolar junction transistor (BJT) which works in the amplifying region and the PD is connected with the base of the BJT which is schematically depicted by Fig. 1(a) and its device equivalent circuit is shown in Fig. 1(b). The output current $I_{DS(BJT)}$, is expressed as follows:

$$I_{DS(BJT)} = (\beta + 1)I_{PH} = (\beta + 1)I_S\left[\exp\left(\frac{V_{BS}}{V_T}\right) - 1\right] \quad (1)$$

where $\beta$ is the amplification factor of the BJT, $I_{PH}$ is light-induced hole current, $V_{BS}$ is the light-induced body bias, $V_T = \frac{kT}{q}$, is the thermal voltage, $k$ is the Boltzmann's constant, $q$ is the electron charge, T is the absolute temperature, and $I_S$ is the reverse-bias saturation current.

Then, from the equations above, the following relation could be obtained:

$$V_{BS} = V_T \ln\left(1 + \frac{I_{PH}}{I_S}\right) \quad (2)$$

where $I_{PH}$ is determined by the rate of the photogenerated holes, $Q_{LH}$, which is associated with the incident photon flux, $\Phi_\lambda$, the photosensitive area of PD, $A_{PD}$, the reflectivity of PD, r, the absorption coefficient of PD for light, $\alpha$, the depletion depth of PD, $d$ and the internal quantum efficiency of PD, $\eta$. The expression is as follows [15]:

$$I_{PH} = \frac{dQ_{LH}}{dt} = q\eta\Phi_\lambda A_{PD}(1 - r)\left(1 - e^{-\alpha d}\right) \quad (3)$$

When $V_{GS}$ increases till the weak inversion occurs, but it is still lower than the threshold voltage of the MOSFET, the PD-MOS works in the sub-threshold mode. Here, according to the equation (4), the light-induced body bias effect causes the threshold voltage drop and finally leads to the rising of the drain current ($I_{DS}$). As schematically illustrated in Fig. 1(c) and Fig. 1(d), the body bias modulates the threshold voltage of the MOSFET and results in the increase of the output current. The threshold voltage drop and the output current are expressed in equation (4) and (5), respectively [15]:

$$\Delta V_{TH} = V_{TH} - V_{TH0} = \gamma\left(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}\right) \quad (4)$$

$$I_{DS(sub)} = \mu C_o \frac{W}{L}(V_T)^2 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right] \quad (5)$$

where $V_{TH0}$ is the initial value of $V_{TH}$ without light exposure, $\phi_f$ is the surface potential, $\mu$ is the field-effect mobility of the MOSFET, $C_o$ is the capacitance of oxide gate, $W$ and $L$ are the channel width and length, respectively, $\gamma$ is the body-effect coefficient, and $n$ is the inverse slope of the subthreshold swing.

In order to illustrate the light-induced body bias effect more clearly, a PD-MOS with width to length ratio of 102 $\mu$m/1$\mu$m and a PD area of 102$\mu$m×5$\mu$m is simulated by using Silvaco TCAD. The relation between $\Delta V_{BS}$ and the light intensity is extracted and presented in Fig. 2. Here, $\Delta V_{BS} = V_{BS} - V_{BS0}$, is the variation of the bias between the substrate and the source of the MOSFET, that is, the bias between the substrate and the source of the MOSFET when the PD-MOS is exposed in various light intensities ($V_{BS}$) minus its counterpart in dark ($V_{BS0}$). It can be found that when the light intensity is less than 10nW/cm$^2$, with the light intensity rising, $\Delta V_{BS}$ changes little and when the light intensity is 1nW/cm$^2$, $\Delta V_{BS}$ is less than 1mV. When

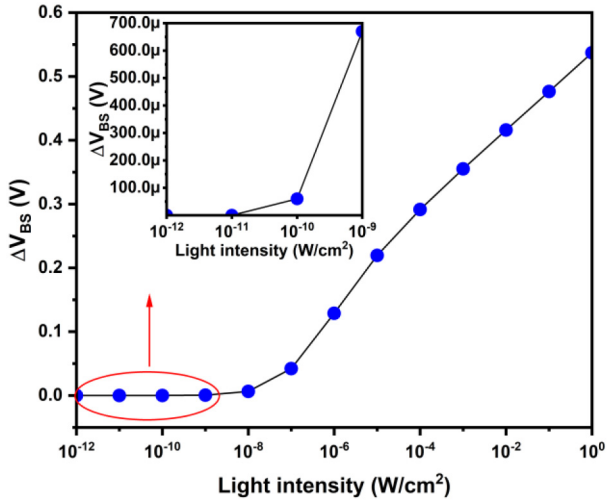



**FIGURE 2.** Simulated change of the potential of substrate, $\Delta V_B$ (the potential of substrate in light minus the potential of substrate in dark) as a function of light intensity.

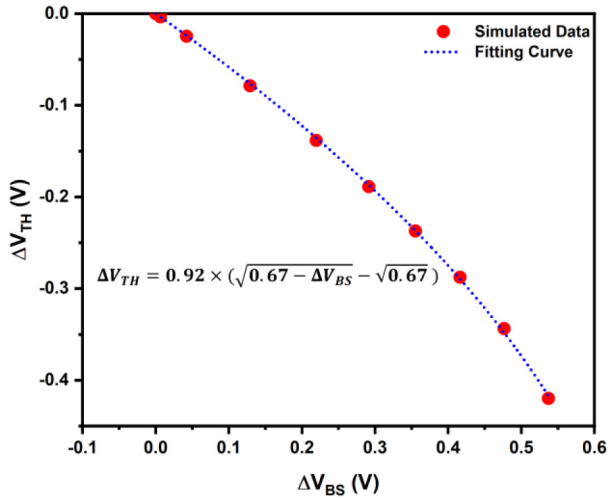



**FIGURE 3.** Simulated threshold voltage change $\Delta V_{TH}$ (the threshold voltage in light minus that in dark) as a function of the variation of the bias between the substrate and the source, $\Delta V_{BS}$ ($V_{BS}$ *in light minus* $V_{BS}$ *in dark*) and the fitting curve with the function $\Delta V_{TH} = \gamma(\sqrt{\phi_f - \Delta V_{BS}} - \sqrt{\phi_f})$.

the light intensity is more than 10nW/cm$^2$, with the light intensity rising, $\Delta V_{BS}$ keeps a quasi-linear rising relation with the logarithm of the light intensity, which is consistent with our analytical model.

Besides, the variation of threshold voltage (the threshold voltage when the PD-MOS is exposed in various light intensities minus the threshold voltage in dark), $\Delta V_{TH}$ changing with $\Delta V_{BS}$ are also extracted from the simulated results and the details are presented in Fig. 3. It shows that $\Delta V_{TH}$ decreases gradually with $\Delta V_{BS}$ along a quasi-linear trend. The fitting function relation is listed as follows:

$$\Delta V_{TH} = V_{TH} - V_{TH0} = 0.92 \times \left(\sqrt{0.67 - \Delta V_{BS}} - \sqrt{0.67}\right) \quad (6)$$

Combining both the figures, the conclusion that the output current $I_{DS(sub)}$ changes quasi-linearly with the light intensity could be obtained. Therefore, the PD-MOS can detect light or serve as a novel optical sensor.

### B. CHARACTERIZATION OF PD-MOS

The aim of this work is to develop an image sensor array with high dynamic range similar to human retinal based on our novel photoelectric device: PD-MOS. With that purpose, the discrete PD-MOS device is characterized firstly. As shown in Fig. 4 (a), the transfer curve of a discrete PD-MOS device whose size is 80$\mu$m×80$\mu$m with a 62$\mu$m×62$\mu$m PD area upon the light intensity ranging from 0 to 10mW/cm$^2$ with the bias between the drain and the source of PD-MOS, $V_{DS}$ = 1V and the bias of the cathode of PD,$V_{PD}$ = 1V is measured. With the light intensity going up, the transfer curves shift negatively implying the threshold voltages decrease and the output currents go up, which agrees with the results of the aforementioned analytical model and simulation results.

From the measured transfer curves, the photocurrents of the PD-MOS working in both modes for various light intensities (1nW/cm$^2$ to 10mW/cm$^2$) are calculated. Take the logarithm of both the photocurrent and light intensity and then fit the two groups of points linearly, respectively. The results presented in Fig. 4 (b) show that when the PD-MOS works in BJT mode ($V_{GS}$ = −0.7V), with the light intensity ranging from 10nW/cm$^2$ to 10mW/cm$^2$, the photocurrent and the light intensity keep a good linearity, indicating the dynamic range of the PD-MOS working in BJT mode is not less than 120dB. When setting $V_{GS}$ = 0.2V, the PD-MOS goes into sub-threshold region, upon the light intensity ranging from 1nW/cm$^2$ to 10mW/cm$^2$, the photocurrent and the light intensity also keep a good linearity, indicating the dynamic range of the PD-MOS working in the subthreshold mode is wider than 140dB.

The gain of PD-MOS working in different modes is also investigated. As shown in Fig. 4 (c), upon the light with the intensity 7$\mu$W/cm$^2$ and the wavelength 570nm, the gain grows exponentially with $V_{GS}$, indicating that the gain of PD-MOS in sub-threshold region is far greater than its counterpart in BJT mode. Therefore, if there is a need to detect the light with very small irradiance or image under dim light condition, PD-MOS working in sub-threshold region is a better choice due to its high gain and thus, high ratio of signal to noise. In this work, the PD-MOS in the pixel of the image sensor array is designed to work in the sub-threshold region so that it is more favorable to image under dim light condition.

Furthermore, the spectral responsibility of PD-MOS in two different modes (BJT, $V_{GS}$ = −0.4V and sub-threshold region $V_{GS}$ = 0.4V) are measured, respectively under the light intensity, 7$\mu$W/cm$^2$ to mark its capability sensitive to light, which is shown in Fig. 5. It can be found that the spectral responsibility of PD-MOS working in BJT mode is less than 10 A/W at its peak wavelength,

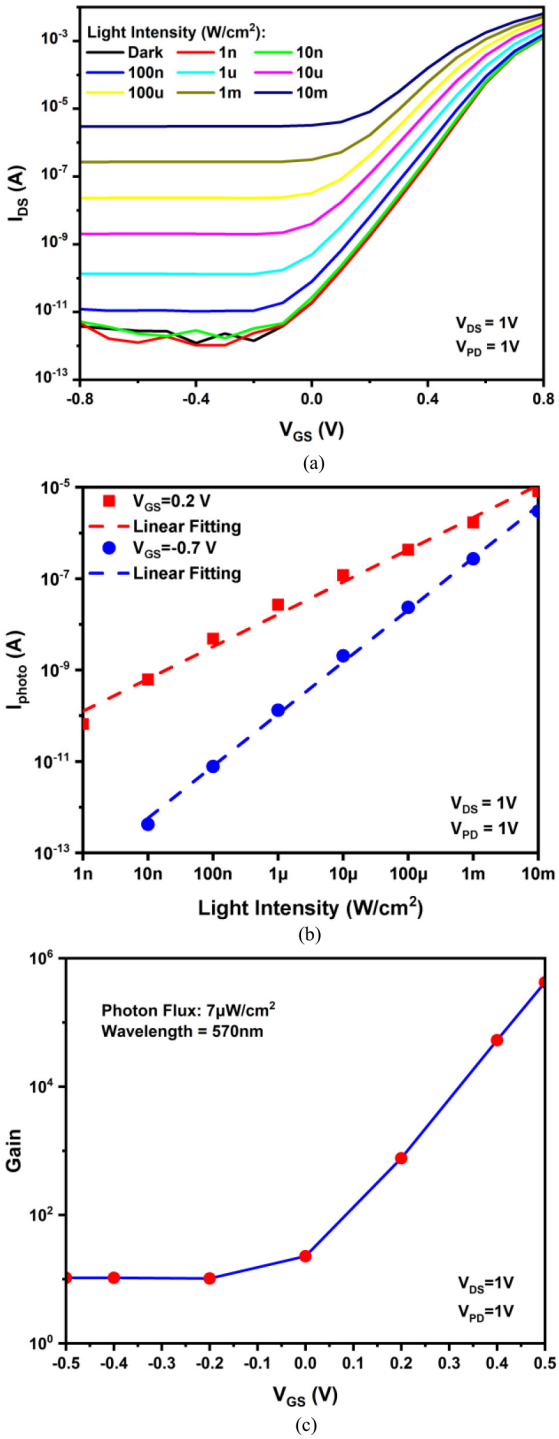



**FIGURE 4.** **(a) Measured transfer characteristics of PD-MOS upon light intensity ranging from 0 to 10mW/cm$^2$ with the bias between the drain and the source of PD-MOS, $V_{DS} = 1V$ and the bias of the cathode of PD,$V_{PD} = 1V$; (b) Extracted curves of photocurrent with respect to light intensity when PD-MOS works in sub-threshold mode ($V_{GS} = 0.2V$) or BJT mode ($V_{GS} = -0.7V$); (c) Measured gain varying with the bias between the gate and source of PD-MOS ($V_{GS}$) exposed in the light whose intensity is $7\mu$W/cm$^2$ and wavelength is 570 nm with $V_{DS} = 1V$ and $V_{PD} = 1V$.**

while the spectral responsibility of PD-MOS working in sub-threshold region is more than 25000A/W at the peak wavelength.

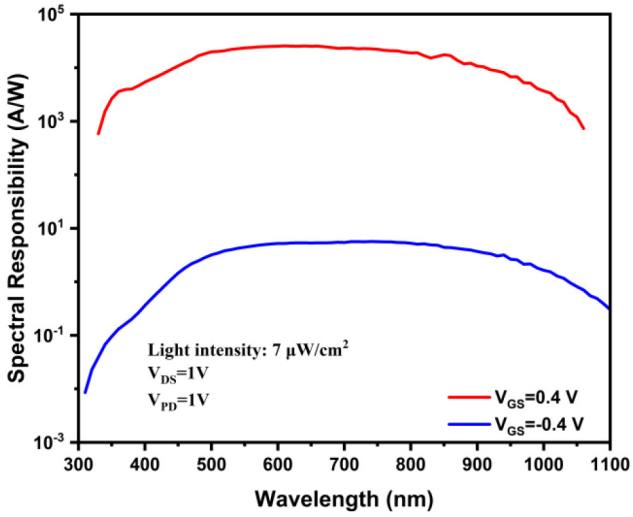



**FIGURE 5.** **Measured spectral responsibility of PD-MOS in two different regions (BJT, $V_{GS} = -0.4V$ and the sub-threshold, $V_{GS} = 0.4V$) upon the light intensity: $7\mu$W/cm$^2$ with $V_{DS} = 1V$ and $V_{PD} = 1V$.**

### C. PIXEL DESIGN

The basic pixel design of our image array is a two-transistor-one-photodiode (2T1D) pixel circuit consisting of a PD-MOS and a switch transistor (Tsel), which has been elaborated in [17], [18].

Be analogous to the logarithm pixel, the 2T1D pixel also does not take the time integral of photo-induced charges during the photoelectric conversion process, which results in the function of random access of our pixel whether in time domain or space domain. This characteristic of random access is more akin to the function of human retinal photoreceptor, which benefits the readout circuit to acquire the signal faster, or read out some concerned signal independently. Also, it is the characteristic that renders us unable to make use of correlated double sampling (CDS) technology which has been adopted frequently by traditional image sensors in order to lower the fixed pattern noise (FPN). Therefore, based on the feature of random access of 2T1D pixel, a new scheme reducing the FPN is proposed which will be illustrated in detail shortly afterwards. Besides, the random access of 2TID pixel allows us to take the method of global reset which enables the signal to be read out more quickly.

## III. ARRAY DESIGN AND CHARACTERIZATION

The architecture of our image array chip is illustrated schematically in Fig. 6 and it consists of the following components: a 12×12 pixel array, a reference column with its pixels shielded from the light, a row selector module (Digital Control, Row Decoder and Row Driver), 12 column PGAs (programmable gain amplifier), 12 column ADCs (analog-to-digital convertor) and the column multiplexer. The image sensor array chip is manufactured through a commercial 180nm CMOS process and its topological micro-graphic view is shown in Fig. 7.

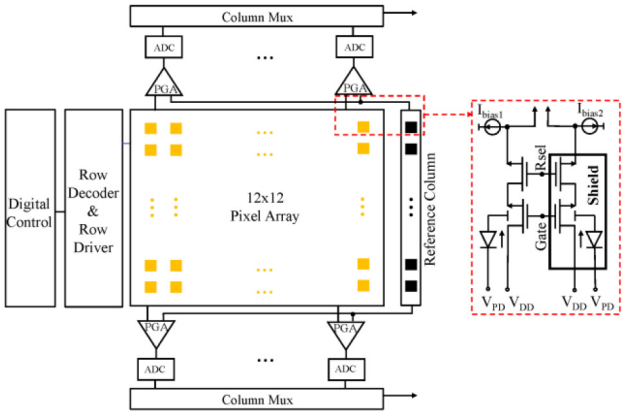



**FIGURE 6.** The architecture of the image sensor array chip including a 12×12 pixel sensor array, one dark pixel reference column, one row selector (Digital Control, Row Decoder and Row Driver), 12 column PGAs (programmable gain amplifier), 12 column ADCs (analog-to-digital convertor) and the column multiplexer.

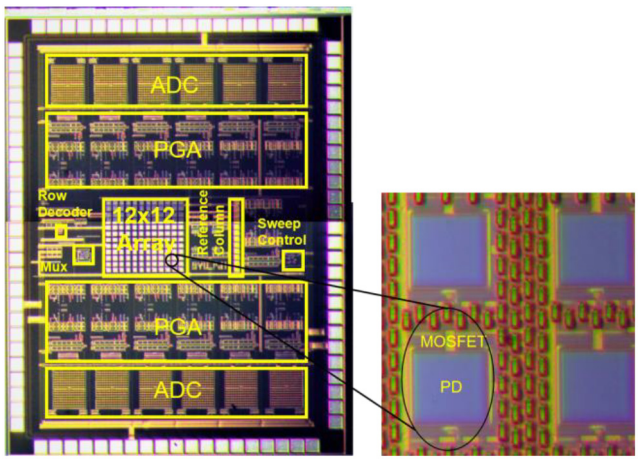
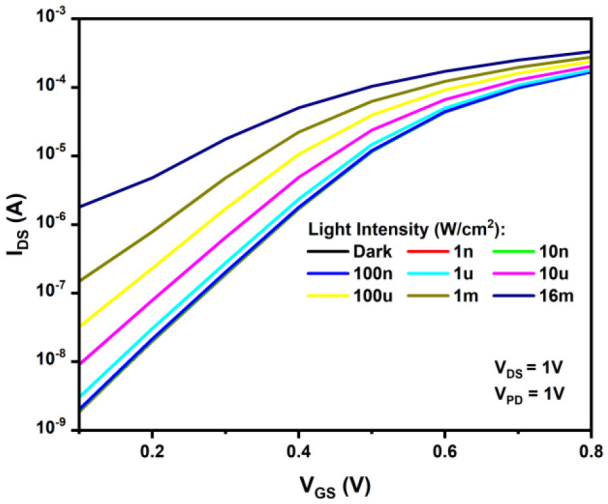
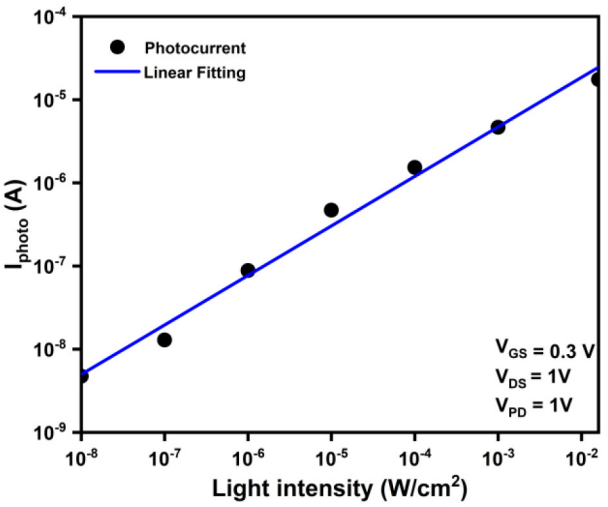



**FIGURE 7.** The topological micro-graphic view of the image sensor array.




(a)




(b)

**FIGURE 8.** (a) Measured transfer characteristic of the PD-MOS in a pixel with the light intensity set from dark to 16mW/cm² and with $V_{DS}$ and $V_{PD}$ both biased at 1V; (b) Linearly fitting the extracted photocurrent points for the light intensity ranging from 10nW/cm² to 16m W/cm² with $V_{GS}$ biased at 0.3V, $V_{DS}$ biased at 1V and $V_{PD}$ biased at 1V.

The 12×12 pixel array is centered on the chip and the 2T1D structure mentioned above constitutes the basic pixel unit which comprises a PD-MOS of 35$\mu$m×35$\mu$m and a neighboring switch transistor, "Tsel" whose ratio of width to length is 5$\mu$m/0.35$\mu$m. As shown in the zoomed-in individual pixel of Fig. 7, the MOSFET in the PD-MOS is designed in a shape of ring surrounding the PD whose size is 22$\mu$m×22$\mu$m, thus, the ratio of width to length is greatly improved to 102$\mu$m/1$\mu$m. The transfer characteristic of the PD-MOS embedded in a pixel is measured with the light intensity set from 10nW/cm$^2$ to 16mW/cm$^2$, $V_{DS}$ and $V_{PD}$ both biased at 1V and is presented in Fig. 8 (a). Since we mainly intend to image with the pixel array in low light conditions, as aforementioned, the PD-MOS in a pixel is designed to work in the sub-threshold region which could contribute greater gain and ratio of the signal to noise. Thus, the bias between the gate and the source, $V_{GS}$ can only be tuned from 0.1V and the transfer characteristic is measured by increasing $V_{GS}$ from 0.1V to 0.8V. The relation between the photocurrent and the light intensity is fitted linearly with the points extracted from the transfer characteristic by biasing $V_{GS}$ at 0.3V, $V_{DS}$ and $V_{PD}$ at 1V and the results are presented in Fig. 8 (b). It shows that when increasing the light intensity from 10nW/cm$^2$ to 16mW/cm$^2$, the photocurrent, $I_{photo}$ almost goes up linearly, indicating that the dynamic range is no narrower than 120dB.

Digital control, row decoder and row driver constitute a row selector to scan rows sequentially. The column multiplexer plays the role of column gating, that is the column scanning. They are located near the pixel array in order to avoid the crosstalk maybe caused by the long wiring. During each row scanning period, the column elements in the row are output one by one through column gating. After all the

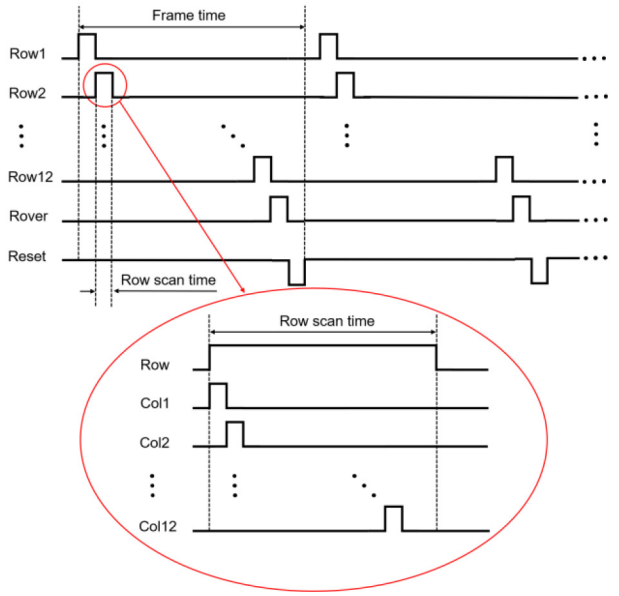



**FIGURE 9.** **The timing diagram of the row scanning and column scanning. "Rover" is the end signal of all the row scanning and "Reset" applied to the cathode of PD of PD-MOS is the global resetting signal of the pixel array.**

twelve rows are scanned, an end signal "Rover" is generated and transmitted to other modules. Once the end signal of row scanning is detected, a global resetting signal named "Reset" which is a low level and applied to the cathode of PD of PD-MOS is produced to reset the whole pixel array. Until this moment, the scanning of one frame image is finished and the next frame scanning is upcoming. The cycle continues and the scanning timing is shown in Fig. 9.

The PGAs and the ADCs are arranged symmetrically on the top and bottom of the image array chip, respectively. The gain of PGAs are tunable from 2 to 150 by applying a digital signal of 3 bits. The ADC with sample rate, 4.16 MHz is used to convert the analog signal from the output of the PGA to the digital signal of 12 bits and is designed with the principle of successive approximation register (SAR). The resulted digital signal can be further processed by the subsequent image signal processor or image acquisition module.

In order to suppress the FPN of the pixel sensor array, a reference pixel column which is shielded from the light with metal layers, is arranged adjacent to the 12×12 pixel array. The output signals from the dark reference pixel and the light pixel are fed into the two input terminals of a PGA, respectively. Thus, a differential signal becomes the output of the PGA and suppression of the FPN can be obtained.

However, it should be noted that the differential output of PGA cannot completely remove the FPN. In order to suppress the FPN more effectively, a tunable current mirror structure is designed at the output terminals of the pixel array and the reference column and the equivalent circuit is detailed in Fig. 6. The tunable current mirrors "$I_{bias1}$" and "$I_{bias2}$" supply the constant current biases, respectively. According to the concept of the virtual open circuit for the

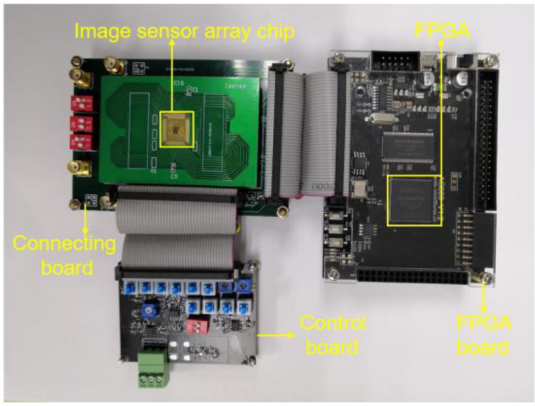



**FIGURE 10.** **The real time image acquisition system based on our image sensor array chip which includes a connecting board, a control board and a FPGA board.**

**TABLE 1.** **Summary of the image sensor array chip information.**

| | |
|---|---|
| **Pixel pitch** | 35μm×35μm |
| **Fill factor** | 39.5% |
| **Array size** | 525μm×485μm |
| **Chip size** | 2.24mm×3mm |
| **Gain of PGA** | tunable from 2 to 150 |
| **ADC** | sample rate, 4.16 MHz; resolution: 12bits; INL, ±1.0 LSB; DNL, ±0.5 LSB |
| **Power** | ⩽60mW |

PGA, the constant current flows in the sequence: the PD-MOS, the switch transistor and the current mirror structure. When the value of the constant current supplied by the current mirror structure is adjusted, the potential at the source of the switch transistor which is also the input terminal of the PGA is modified correspondingly. Then, the output of the PGA could be regulated through the tunable current mirror structure.

## IV. RESULTS OF IMAGING AND ANALYSIS

Table 1 summarizes the related information of the image sensor array chip. In order to capture an image of the image sensor array, a real time imaging acquisition system is set up, which contains a dark box, a light source whose intensity could be tuned precisely, an upper computer, an image sensor array chip, a connecting board, a FPGA board, a control board and some power supply. The dark box is used to separate the image sensor array from the outside light. The light source whose intensity could be adjusted exactly in a large range is needed to test the imaging capability of the image sensor array upon various light intensity. The connecting board acts as a connector which connects the image sensor array chip with other parts of the imaging system, such as the control board and the FPGA board. The control board is used to switch working mode (testing mode or scanning mode) of the image sensor array chip or adjust the gain of PGA. The FPGA board serves to acquire image. These three parts are at the heart of the imaging system

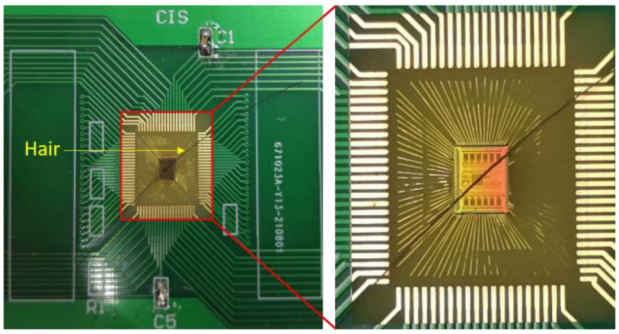



**FIGURE 11.** A hair with its diameter approximately 60-70$\mu$m is placed on the pixel array.

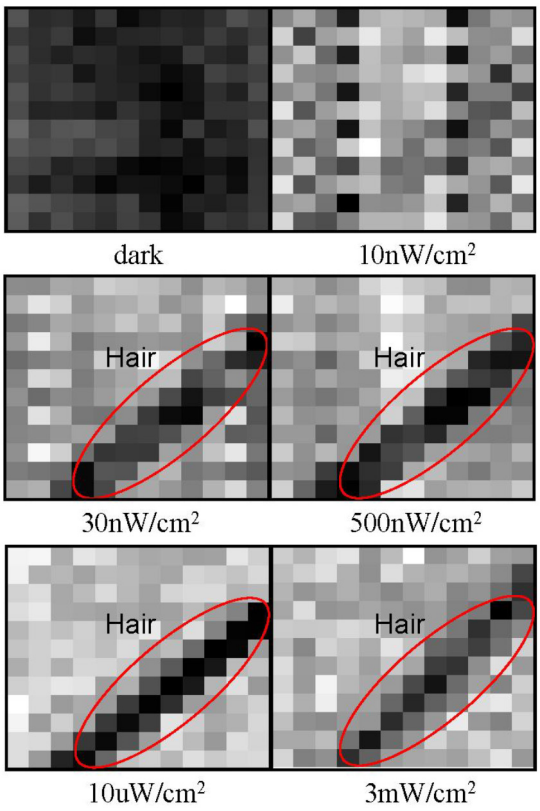



**FIGURE 12.** The acquired images under the light intensity: dark, 10nW/cm$^2$, 30nW/cm$^2$, 500nW/cm$^2$, 10$\mu$W/cm$^2$ and 3mW/ cm$^2$.

and are shown in Fig. 10. The upper computer shows the acquired images by FPGA.

A hair with its diameter approximately 60-70$\mu$m is selected as the imaging object of the image sensor array since there are only 144 pixels, about 0.5mm$\times$ 0.5mm field of view without lens and the hair is placed on the pixel array shown in Fig. 11. The experiment is conducted upon a series of light intensities: from dark to 3mW/cm$^2$ and the acquired images are demonstrated in Fig. 12. The hair occupies about two pixels since the diameter of a hair is in the range of about 60$\mu$m to 70$\mu$m. Furthermore, it could be found that until exposed to the light with its intensity

**TABLE 2.** Comparison of this work with the state-of-the-art.

| Parameters | M. Bae [5] | SM Hussain [9] | This Work |
|---|---|---|---|
| Technology | 0.35-µm (standard) | 0.18-µm (standard) | 0.18-µm (standard) |
| Supply Voltage (V) | 3.3 | 1.8/3.3 | 3.3 |
| Pixel Pitch (µm$^2$) | 10×10 | 15×15 | 35×35 |
| Fill Factor | 28.4% | 60% | 39.5% |
| Pixels Resolution | 160×120 | 200×200 | 12×12 |
| Dynamic Range (dB) | 106 | 53 | 110 |

10nW/cm$^2$, the hair become visible. When the light intensity comes to 3mW/cm$^2$, the limit of light source, the hair is still distinguishable. The experimental results indicate that the dynamic range of the image sensor array is no narrower than 110dB. Furthermore, the comparison between this work and the prior related state-of-the-art work is listed in Table 2.

## V. CONCLUSION

Inspired by human retina, the PD-MOS working in the subthreshold region has the high and adjustable gain (up to $10^5$), wide dynamic range (greater than 140 dB) and high spectral responsibility (up to $10^4$ A/W). The image sensor array based on the PD-MOS can image from the low-level light intensity 10nW/cm$^2$ to 3mW/cm$^2$ and the dynamic range is wider than 100dB, making it promising for imaging and vision applications.

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