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A New IR-Drop Model That Improves Effectively the Brightness Uniformity of an AMOLED Panel

PAUL C.-P. CHAO (Senior Member, IEEE), SHIH-SONG CHENG, CHIU-HAO CHEN, AND KUEI-YU LEE

Department of Electronics and Electrical Engineering, National Yang-Ming Chiao-Tung University, Hsinchu 300, Taiwan

CORRESPONDING AUTHOR: P. C.-P. CHAO (e-mail: pchao@nycu.edu.tw)

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ABSTRACT A new model characterizing the IR drop in an active-matrix organic light-emitting diode (AMOLED) display is built successfully by this study, which can be used to effectively improve brightness uniformity by adjusting gray levels addressed accordingly to pixels in the panel. The IR-drop refers to the voltage drops along the thin power lines from the external driver at panel edge to internal pixels. The built IR-drop model is in a form of vector and matrix with parameters and variables such as equivalent resistances of horizontal/vertical power lines and the current through the drive thin film transistors (TFTs) and OLEDs in pixels. With precisely calibrated parameters, the model can be solved for the voltage drops at given sub-pixels in the AMOLED panel. Based on the solved dropped voltages at each pixel, the gray level assigned to the pixel V_{data} can be adjusted accordingly to restore the desired pixel luminance. The proposed compensation was implemented in a 14-inch AMOLED panel with FHD resolution for performance validation. The experimental results show less than 2.5% of prediction error on voltage drops, leading to effective compensations that improves the measured pixel currents from 66.1% to 89.7%, 70.3% to 92.9%, and 48.8% to 85.1% of the desired, non-dropped currents, respectively, for red, green, and blue illuminance at the L255 gray level. Also from experiments are substantial improvements of 21.7%, 21.5%, and 35.3% on the brightness uniformity of the panel displayed for red-, green-, blue-images at L255 gray, respectively.

INDEX TERMS IR-drop, brightness uniformity, voltage drop, compensation, iterative numerical analysis, drive thin film transistor (DTFT), active-matrix organic light-emitting diode (AMOLED) displays.

I. INTRODUCTION

Active-Matrix organic light-emitting diode (AMOLED) displays are regarded as one of most promising display technologies, which have merits such as high contrast ratio, good image quality, fast response time, wide color gamut, and low dynamic power consumption. In recent years, the demand on medium- or large-sized AMOLED panels become imminent and developed towards much better user experience. However, these panels suffer inevitably a more severe problem of emission non-uniformity due to IR-drop. The IR-drop refers to the unavoidable voltage drops along power lines from the driver at the panel edge to the pixels of the AMOLED panel, which leads to inaccurate addressing in gray levels to each pixel, resulting in intolerant gray level drops in luminance from CMOS source drivers at the panel edge to other areas. To solve the problem, a few techniques were reported to compensate the voltage drops along power lines, which can be classified into internal and external compensations. The internal one is realized with developing new pixel circuits [1]–[17], where the voltage supplied by the power line degraded by IR-drop is designed in the pixel as source voltage to charge a capacitor in the pixel for compensating threshold voltage (V_{th}) of the driving thin film transistor (DTFT). Although this approach did reduce the luminance degradation due to IR-drop, the assumed perfect cancellation between V_{th} and dropped supplied voltage is not

guaranteed, limiting the compensation effect. On the other hand, the external compensations were realized with external feedback circuits [18]–[22] outside of the panel, where the voltage drops at every sub-pixel were sensed in required short times to orchestrate the adjustments on the gray levels for compensating IR-drops. These approaches often face the difficulties of current-sensing inaccuracy, especially for very low gray levels, inadequate time for sensing from inner pixels via fine electrodes to the external CMOS circuit, and much higher costs to implement associated sensing and compensating CMOS circuity.

To ease the aforementioned difficulties in compensating IR-drop for AMOLED panels, some studies explored the possibility of establishing equivalent circuit models to estimate IR-drop and then compensate. Jung *et al.* [23] established an IR-drop model in 2006 to estimate the IR-drop without experimental validation and compensation. Juan *et al.* [24] reported in the same year an IR-drop model but for passive matrix OLED (PMOLED). Yum *et al.* [25] in 2020 reported another IR-drop model to assist the existing compensation by the pixel circuit, leading to a good result of 99.32% in compensation accuracy, with both pixel and IR-drop compensations active. In this study, a new IR-drop model is proposed to solely compensate the brightness non-uniformity of an AMOLED panel. This IR-drop model is built successfully as in equations of vectors and matrices via the theory of equivalent circuitry to solve for voltage drops along the power lines in the panel, and then distilling a compensation scheme. Calibrated next by experiments, the built model is capable of estimating voltage drops at all pixels, and further to adjust effectively gray levels for compensation, showing favorable brightness uniformity over the panel area.

The paper is organized as below. The new IR-drop model and the new compensation scheme are synthesized in Section II. Section III presents experimental validations of the performance offered by the model for non-uniformity compensation on a 14-inch AMOLED panel. Section IV concludes this study.

II. MODELING AND COMPENSATING IR-DROP

A. MODELING IR-DROP

An equivalent circuit model is built herein to characterize the IR-drops along power lines in an AMOLED panel with $m \times n$ resolution, as shown in Fig. 1. On the other hand, in Fig. 2 is a typical pixel circuit composed of two TFTs and one capacitor, where the drive thin film transistor (DTFT) controls via varied gate voltage the driving current through the OLED for a given illumination level. Simplifying the electronics in a pixel to a current source driven by the DTFT leads to the IR-drop model in Fig. 1 for ensuing modeling and analysis with adequate precision. Also in Fig. 1 are R_v and R_h, the wire resistances of the power line segments between two adjacent sub-pixels along the vertical and horizontal directions, respectively. On the other hand, R_{ext} is the wire resistance between the sub-pixels at the edge of the panel and external biasing voltages. $I_{i,j}$'s are the current sources that

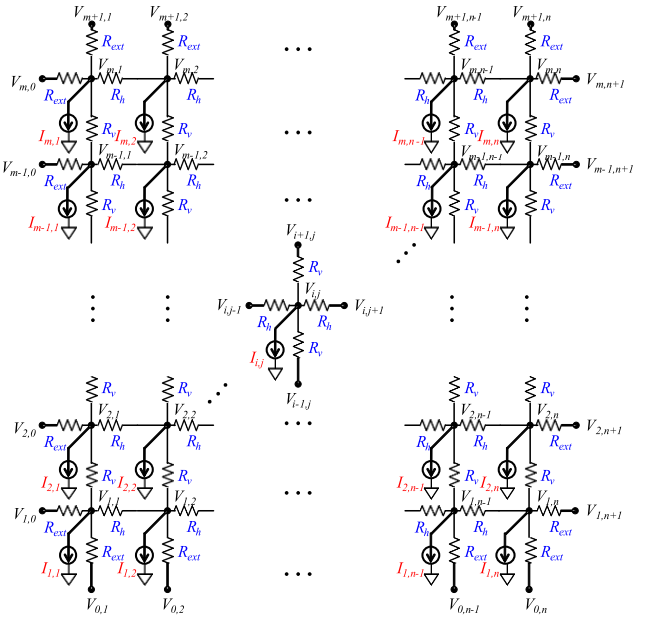


FIGURE 1. The equivalent circuit model built to characterize the IR-drop along power lines in an AMOLED panel.

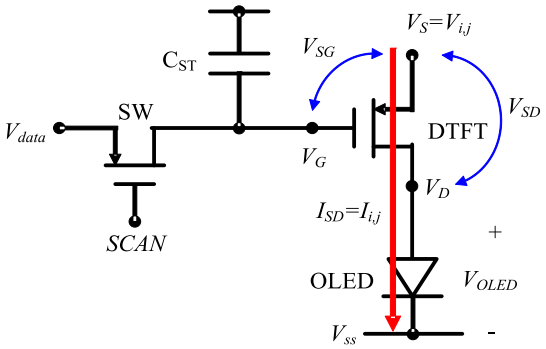


FIGURE 2. A typical pixel circuit with IR-drop in an AMOLED panel.

capture the currents driving OLEDs in sub-pixels towards illumination, which are generated by the DTFTs. $V_{i,j}$'s are the actual, dropped biasing voltages at pixels, providing the source voltage of DTFTs, as seen in Fig. 2. $V_{i,j}$'s are actually supplied by the power source V_{dd} via power lines from panel edge to sub-pixels, usually assumed to be the same as V_{dd} for correct illumination but actually lower than V_{dd} due to IR drop in long power lines from V_{dd} at the panel edge to $V_{i,j}$'s at pixels. Note that the distribution of $V_{i,j}$'s over the panel serves well as an quantitative measure of IR-drop.

To model IR-drop, the associated equivalent circuit in Fig. 1 is first modeled by nodal equations of voltage equilibria at $V_{i,j}$'s for each sub-pixel in Fig. 1 based on Kirchhoff law, yielding

$$\frac{V_{i-1,j}-V_{i,j}}{R_v}+\frac{V_{i+1,j}-V_{i,j}}{R_v} + \frac{V_{i,j-1}-V_{i,j}}{R_h}+\frac{V_{i,j+1}-V_{i,j}}{R_h}=I_{i,j}, \quad (1)$$

where $I_{i,j}$'s are the OLED current driven and controlled by DTFT as seen in Fig. 2. Eq. (1) can be rewritten as

$$\begin{aligned} &-V_{i,j}\left(\frac{2}{R_v}+\frac{2}{R_h}+\frac{0}{R_{ext}}\right)+V_{i-1,j}\left(\frac{1}{R_v}\right)+V_{i+1,j}\left(\frac{1}{R_v}\right)\\ &\quad+V_{i,j-1}\left(\frac{1}{R_h}\right)+V_{i,j+1}\left(\frac{1}{R_h}\right)\\ &=I_{i,j}\quad i=2,\ldots m-1;\quad j=2,\ldots n-1 \end{aligned} \tag{2}$$

As for the sub-pixels at panel edge, the associated nodal equations can also be derived in a similar way, which are given in Appendix. In the next step, all the nodal equations at sub-pixels are assembled into a vector-matrix form as

$$\mathbf{M}\mathbf{v}=\mathbf{L}, \tag{3}$$

where $\mathbf{M}$ is a matrix capturing all resistances, $\mathbf{v}$ is a vector composed of all $V_{i,j}$'s, while $\mathbf{L}$ is another vector containing OLED current, $I_{i,j}$'s. $\mathbf{M}$ is actually

$$\mathbf{M}=\begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & & \cdots & \mathbf{0}\\ \mathbf{A} & \mathbf{B} & \mathbf{C} & \mathbf{0} & & & \vdots\\ \mathbf{0} & \mathbf{C} & \mathbf{B} & \mathbf{C} & & & \\ & & \ddots & \ddots & \ddots & & \\ & & & \mathbf{C} & \mathbf{B} & \mathbf{C} & \mathbf{0}\\ \vdots & & & \mathbf{0} & \mathbf{C} & \mathbf{B} & \mathbf{A}\\ \mathbf{0} & \cdots & & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}, \tag{4a}$$

where sub-matrices are

$$\mathbf{A}=\begin{bmatrix} \mathbf{0} & \mathbf{0} & & \cdots & \mathbf{0}\\ \mathbf{0} & \frac{1}{R_{ext}} & & & \vdots\\ & & \ddots & & \\ \vdots & & & \frac{1}{R_{ext}} & \mathbf{0}\\ \mathbf{0} & \cdots & & \mathbf{0} & \mathbf{0} \end{bmatrix}, \tag{4b}$$

$$\mathbf{B}=\begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & & \cdots & \mathbf{0}\\ \frac{1}{R_{ext}} & \mathbf{B_1} & \frac{1}{R_h} & \mathbf{0} & & & \vdots\\ \mathbf{0} & \frac{1}{R_h} & \mathbf{B_2} & \frac{1}{R_h} & & & \\ & & \ddots & \ddots & \ddots & & \\ & & & \frac{1}{R_h} & \mathbf{B_2} & \frac{1}{R_h} & \mathbf{0}\\ \vdots & & & \mathbf{0} & \frac{1}{R_h} & \mathbf{B_1} & \frac{1}{R_{ext}}\\ \mathbf{0} & \cdots & & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}, \tag{4c}$$

$$\mathbf{C}=\begin{bmatrix} \mathbf{0} & \mathbf{0} & & \cdots & \mathbf{0}\\ \mathbf{0} & \frac{1}{R_v} & & & \vdots\\ & & \ddots & & \\ \vdots & & & \frac{1}{R_v} & \mathbf{0}\\ \mathbf{0} & \cdots & & \mathbf{0} & \mathbf{0} \end{bmatrix}, \tag{4d}$$

$$\mathbf{B_1}=-\left(\frac{1}{R_v}+\frac{1}{R_h}+\frac{2}{R_{ext}}\right), \tag{4e}$$

and

$$\mathbf{B_2}=-\left(\frac{2}{R_v}+\frac{2}{R_h}+\frac{0}{R_{ext}}\right). \tag{4f}$$

$\mathbf{v}$ in Eq. (3) reflects actually the voltage distribution on a panel, which is of the form

$$\mathbf{v}=\begin{bmatrix}\mathbf{v_0} & \mathbf{v_1} & \cdots & \mathbf{v_m} & \mathbf{v_{m+1}}\end{bmatrix}^{\mathrm{T}}, \tag{5a}$$

where sub-vectors are

$$\begin{aligned} \mathbf{v_0}&=\begin{bmatrix} V_{0,0}\\ V_{0,1}\\ \vdots\\ V_{0,n}\\ V_{0,n+1}\end{bmatrix}, \mathbf{v_1}=\begin{bmatrix} V_{1,0}\\ V_{1,1}\\ \vdots\\ V_{1,n}\\ V_{1,n+1}\end{bmatrix}, \cdots,\\ \mathbf{v_m}&=\begin{bmatrix} V_{m,0}\\ V_{m,1}\\ \vdots\\ V_{m,n}\\ V_{m,n+1}\end{bmatrix}, \mathbf{v_{m+1}}=\begin{bmatrix} V_{m+1,0}\\ V_{m+1,1}\\ \vdots\\ V_{m+1,n}\\ V_{m+1,n+1}\end{bmatrix}. \end{aligned} \tag{5b}$$

On the other hand, $\mathbf{L}$ in Eq. (3) is the current distribution on a panel, which is of the form

$$\mathbf{L}=\begin{bmatrix}\mathbf{I_0}\ \mathbf{I_1}\cdots\mathbf{I_m}\ \mathbf{I_{m+1}}\end{bmatrix}^{\mathrm{T}}, \tag{6a}$$

where sub-vectors are

$$\mathbf{I_0}=\begin{bmatrix}0\\0\\\vdots\\0\\0\end{bmatrix}, \mathbf{I_1}=\begin{bmatrix}0\\I_{1,1}\\\vdots\\I_{1,n}\\0\end{bmatrix}, \ldots, \mathbf{I_m}=\begin{bmatrix}0\\I_{m,1}\\\vdots\\I_{m,n}\\0\end{bmatrix}, \mathbf{I_{m+1}}=\begin{bmatrix}0\\0\\\vdots\\0\\0\end{bmatrix}. \tag{6b}$$

B. COMPENSATING IR DROPS

To compensate IR-Drop for better brightness uniformity, the first step is to solve Eq. (3) for $\mathbf{v}$ and $\mathbf{L}$, the dropped voltages in $\mathbf{v}$ and the associated OLED currents in $\mathbf{L}$, and then in the second step the compensation can be orchestrated. The detailed computation for the afore-mentioned solution/compensation is illustrated by a flow in blocks in Fig. 3. To solve Eq. (3) for $\mathbf{v}$ and $\mathbf{L}$, one should note first that in Fig. 2 where there is the typical, simple pixel circuit, the source voltage (Vs) of the DTFT is connected to the power line of V_{dd}, which is equivalent to $V_{i,j}$. The generated source-to-drain electric current (I_{SD}) of the DTFT is the determined by the source-to-gate voltage (V_{SG}) and the source-to-drain voltage (V_{SD}), which equals to $I_{i,j}$, that is,

$$I_{SD}=I_{i,j}=\kappa(V_{SG}-|V_{th-DTFT}|)^2(1+\lambda V_{SD}), \tag{7}$$

where κ is a process-related parameter, $V_{th-DTFT}$ is V_{th} of the DTFT, and λ is a parameter due to channel length modulation. V_G, the gate voltage of DTFT, is updated at V_{data} to display the desired gray signal as the switch (SW) TFT

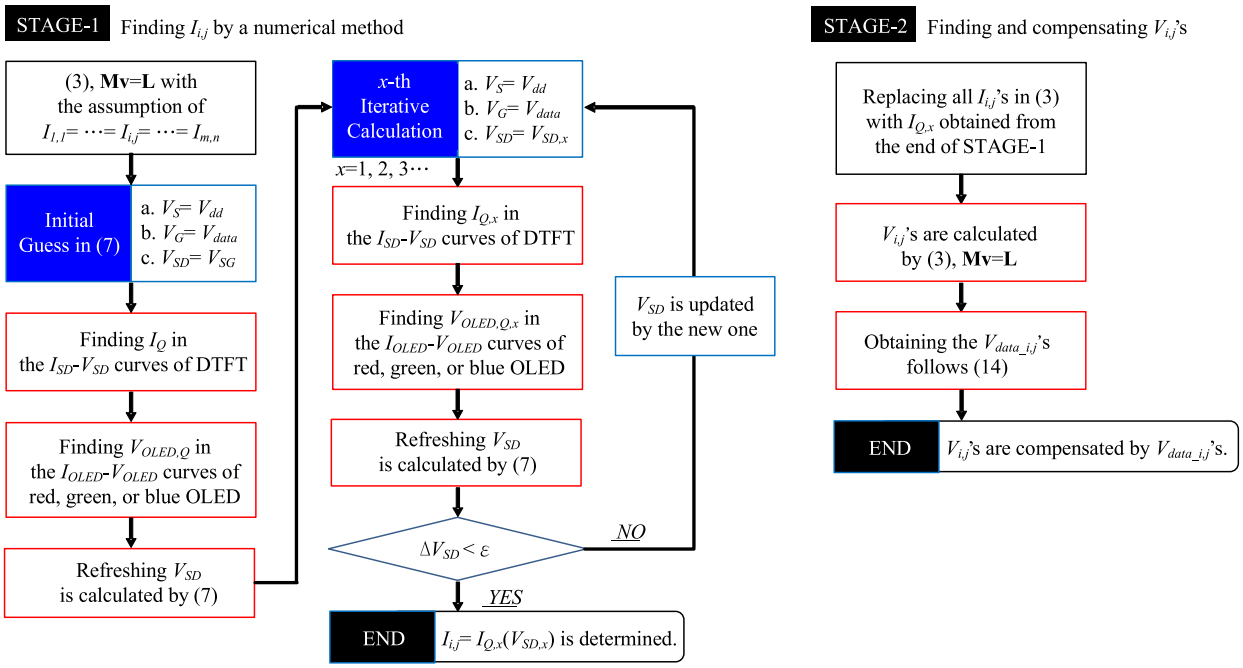


FIGURE 3. **The proposed computation process used to predict and then compensate IR drops of the power lines in an AMOLED panel.**

is turned on. On the other hand, V_{SD} is determined by $V_{i,j}$, V_{OLED} , and V_{SS}, since

$$V_{SD} + V_{OLED} = V_{i,j} - V_{SS}, \tag{8}$$

where V_{SS} can be considered as a given constant.

The computation flow for IR-Drop compensation is orchestrated based on Eqs. (3), (7), and (8), leading to that in Fig. 3. In STAGE-1, the OLED currents $I_{i,j}$'s are solved based on the nonlinear equations (3), via multiple numerical iterations. In practice, the AMOLED panel is first illuminated at a given gray level. V_{dd} and V_{data} are next measured to serve as known parameters in solving Eqs. (3). Then the iterations for solving Eqs. (3) starts with assuming all sub-pixels experiencing identical currents, that is,

$$I_{1,1} = \cdots = I_{i,j} = \cdots = I_{m,n}, \tag{9}$$

to be substituted into Eq. (3) to find the solution of $I_{i,j}$, through iterations. To this end, the electrical characteristics, i.e., I-V curves, of DTFT and OLEDs in the AMOLED panel are also measured, as shown in Figs. 4. For the initial guess, the DTFTs are set up with the same levels of voltages for V_S, V_G, and V_{SD}. I_Q can then be estimated based on the curves in Fig. 4(a), using bilinear interpolation, yielding

$$I_Q = \frac{I_P - I_{P-1}}{V_{SG,P} - V_{SG,P-1}}\left(V_{SG,Q} - V_{SG,P-1}\right) + I_{P-1}, \tag{10}$$

where $V_{SG,P}$, $V_{SG,P-1}$, I_P, and I_{P-1} are obtained from measurements. $V_{OLED,Q}$ can be found based on the I_Q estimated by Eq. (10) and the curve of the OLED in Fig. 4(b). Next, V_{SD} is updated based on Eq. (7) by $V_{SD,1}$, and then, the iterations go on, for example, to arrive at I_{Q1}, $V_{OLED,Q,1}$, and $V_{SD,2}$ at the end of the next iteration. The continuous iterations are designed herein to stop as the difference between two consecutive V_{SD}'s through iterations becomes smaller than a pre-designated value, ε, the description of which is given by

$$\Delta V_{SD} = \left|V_{SD,x+1} - V_{SD,x}\right|; x = 1, 2, \ldots, \tag{11}$$

$$\begin{cases} \Delta V_{SD} < \varepsilon \rightarrow \text{END}, \\ \Delta V_{SD} \geq \varepsilon \rightarrow \text{REPEAT}, \end{cases} \tag{12}$$

where ε is defined as a threshold value, below which based on experience the proposed iterative computation to solve for V_{SD}'s of DTFTs in sub-pixels converges successfully with the adequate prediction accuracy on V_{SD}'s. With Eq. (12) in hands, STAGE-1 stops with the solved V_{SD}'s, while the associated $I_{i,j}$ are to be derived in the next stage, STAGE-2. In this stage, it starts with replacing all $I_{i,j}$'s in Eq. (3) with the I_Q obtained at the end of STAGE-1, and then $V_{i,j}$'s are calculated. Thus, the voltage drop at sub-pixels can be obtained by

$$\delta_{i,j} = V_{dd} - V_{i,j}, \tag{13}$$

where $\delta_{i,j}$ captures the undesired voltage drop from V_{dd} at sub-pixel i,j. Towards compensating the OLED current to restore illuminance back to the case without IR-Drop, V_{data} is adjusted by

$$V_{data\_i,j} = V_{data} - \delta_{i,j}. \tag{14}$$

Therefore, the compensated current could be expressed by substituting Eqs. (14) to (7), yielding

$$I_{SD} = I_{C\_i,j} = \kappa\left(V_{dd} - V_{data} - |V_{th-DTFT}|\right)^2\left(1 + \lambda V_{SD,x}\right), \tag{15}$$

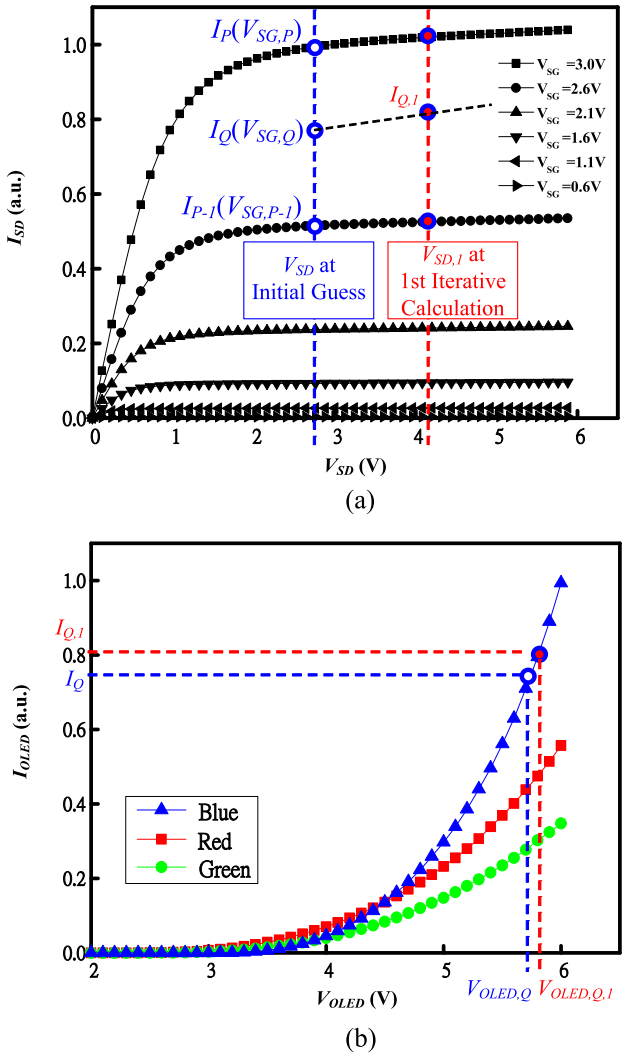


FIGURE 4. Measured electrical characteristics of (a) DTFT, (b) red-, green-, and blue-OLED in the 14-inch FHD AMOLED panel, which are used for calibrating the proposed compensation.

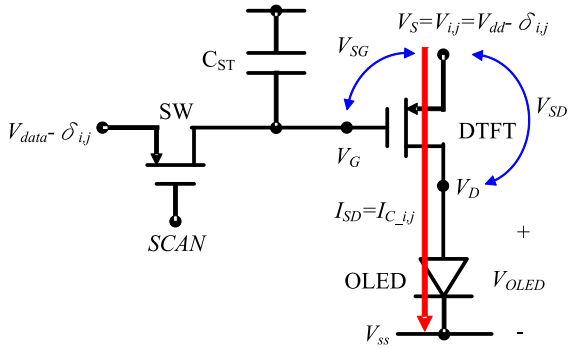


FIGURE 5. The electric currents compensated by an adjusted *Vdata* based on the biasing voltage *Vdd* predicted by the built IR-drop model.

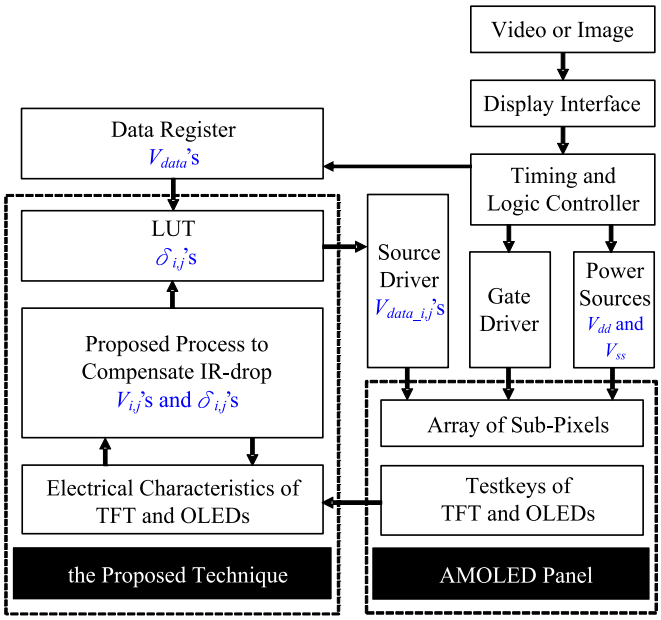


FIGURE 6. The display system built to implement the proposed IR-drop compensation.

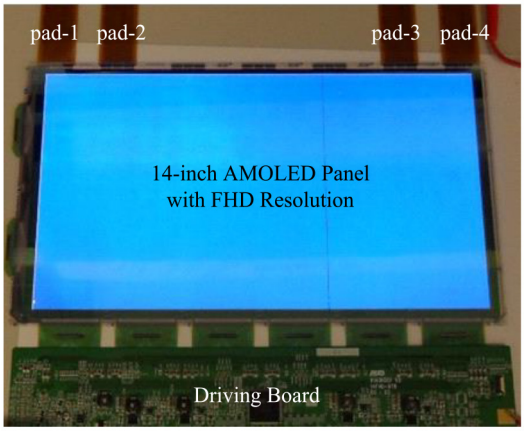
where it is seen that $\delta_{i,j}$ is absent in the compensated OLED current, restoring successfully the OLED current back to the originally desired level, since the dropped V_{SG} is replaced by a non-dropped V_{dd}; in other words, the voltage drop along the power line is successfully compensated.

With the compensation scheme successfully developed, a display system in an AMOLED panel is next built for performance validation. This built display system is schematically illustrated in Fig. 6 in blocks, where special designed testkeys were implemented next to the array of sub-pixels in the panel in order to monitor the electrical or optical characteristics required to calibrate the model in Eq. (3) and further facilitate the compensation in Eq. (14) developed in this subsection. Using the display system as shown in Fig. 6, the voltage drops at each sub-pixel in the panel, $V_{i,j}$'s, are predicted with red-, green-, and blue-images illuminated by the panel for different gray levels, then the corresponding compensating bias voltages, $\delta_{i,j}$'s, are calculated based on Eq. (13) and implemented. These $\delta_{i,j}$'s are stored in the memory of a look-up table (LUT) to compensate V_{data}'s of each sub-pixel via Eq. (14) to provide new $V_{data\_i,j}$'s. Next, new $V_{data\_i,j}$'s are delivered into the display interface to adjust gray levels in the input images for addressing each sub-pixel at the desired grays. For the hardware operation to implement the aboves, with the LUT loaded with $\delta_{i,j}$'s, the source driver outputs $V_{data\_i,j}$'s, the new V_{data}'s adjusted by $\delta_{i,j}$'s from the LUT, then the $V_{data\_i,j}$'s are delivered into the sub-pixels in the AMOLED panel to generate the compensated currents as seen in Eq. (15), which are supposed to be back to level where there is no IR drops. In this way, the brightness uniformity displayed by the panel should be substantially improved even in the presence of IR drops.

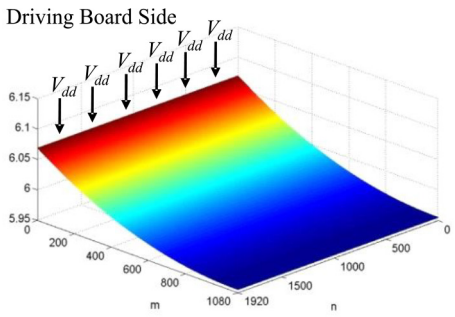
III. EXPERIMENTAL VALIDATION

A. VALIDATING THE IR-DROP MODEL

An AMOLED panel in a resolution of full high definition (FHD) was manufactured to validate the modeling and compensation proposed. The panel has six ports connected to the driving board via a flexible printed circuit (FPC)



(a)



(b)

FIGURE 7. **(a) The FHD AMOLED panel for validating the proposed compensation and (b) the result of predicting biasing voltage distribution of V_{dd} in the panel.**

and another four ports at the opposite side of the panel for measuring voltage drops, as shown in Fig. 7(a). The equivalent circuit model was first calibrated to identify all its parameters, and then several simulation runs were conducted to validate the proposed compensation. The electrode resistances R_h, R_v and R_{ext} in the model of the panel in Eq. (3) are measured, resulting in 2.6Ω, 5.4Ω and 10^{-7}Ω, respectively, while the power voltages on the driving board side of the panel, V_{dd} and V_{ss}, are set up as 6.15V and −2.45V, respectively. Next, the biasing voltages on sub-pixels, $V_{i,j}$'s, were solved based on Eq. (3) via the proposed computation process shown in Fig. 3. The solved distributions on biasing voltages, $V_{i,j}$'s, are plotted in Fig. 7(b). With the distributed biasing voltage calculated, on the other hand, the realistic biasing voltages are measured at Pads 1 to 4 for comparison, the locations of which are shown in Fig. 7(a), far away from V_{dd} at the other side of the panel, where there is the driving board. The measured and calculated biasing voltages are listed in Table 1 for comparison, where the mean squared errors of predicting the biasing voltages by the built model as compared to measured counterparts are **as low as 1.42%, 1.40%, and 2.32%**, respectively, for red, green, and blue images displayed at the gray level of 255. In addition to 255 gray level, the panel is displayed at all other gray levels,

TABLE 1. **Measured versus calculated voltages.**

Illuminating Red Image at L255 gray			
		Measured	**Calculated**
Monitored Position	Pad 1	5.768 V	5.769 V
	Pad 2	5.586 V	5.769 V
	Pad 3	5.608 V	5.769 V
	Pad 4	5.791 V	5.769 V
Mean Squared Error		1.50%	
Illuminating Green Image at L255 gray			
		Measured	**Calculated**
Monitored Position	Pad 1	5.802 V	5.802 V
	Pad 2	5.619 V	5.802 V
	Pad 3	5.642 V	5.802 V
	Pad 4	5.825 V	5.802 V
Mean Squared Error		1.49%	
Illuminating Blue Image at L255 gray			
		Measured	**Calculated**
Monitored Position	Pad 1	5.544 V	5.606 V
	Pad 2	5.369 V	5.606 V
	Pad 3	5.413 V	5.606 V
	Pad 4	5.589 V	5.606 V
Mean Squared Error		2.44%	

the measurements of which are summarized in Figs. 8(a), along with predicted counterparts based on the model built by this study and the errors. It is seen from these figures that the predicted gray levels with IR-drop estimated by the model built by this study are lower than their measurement counterparts at lower gray levels, while higher at higher gray levels, indicating that IR-drop is more significant for higher gray levels. The overall voltage errors are within the range of −0.70% to 1.42%, −0.58% to 1.40%, and −1.58% to 2.32% for red-, green- and blue-images illuminated, respectively. Next, the two sets of particular sub-pixels located at row 1, column 330 (at the top edge of the panel, i.e., beside the external power source) for the no-voltage-drop case and at row 1080, column 330 (at the other side and the edge of the panel) for the voltage-drop case are considered to measure $V_{i,j}$'s, V_{data}'s and distilling voltage drops, $\delta_{1080,330}$'s, aiming to validate the effectiveness of the compensation scheme proposed by this study. The results are shown in Figs. 8(b), where the voltage drops, $\delta_{1080,330}$'s, are calculated based on Eq. (13), while $V_{data\_1080,330}$'s are designated for compensations based on Eq. (14). It can be seen from the subfigures (b) in Figs. 8 that the voltage drops, $\delta_{1080,330}$'s, range from 0.088V to 0.381V, 0.039V to 0.348V, and 0.115V to 0.544V in illuminating red-, green-, and blue-images from L0 to L255 grays. With new $V_{data\_1080,330}$'s for compensation in hands, the compensated current along with un-compensated counterparts are shown in subfigures (c) for performance validation. It can be seen from these subfigures (c) that the OLED currents are compensated from $I_{1080,330}$'s to $I_{C\_1080,330}$'s, much closer to the desired, non-dropped current of $I_{1,330}$, presenting the effectiveness of the proposed model and compensation that can improve the pixel currents in practice from 66.1% (uncompensated) to 89.7% (compensated), 70.3% to 92.9%, and 48.8% to 85.1% of the desired, non-dropped currents, respectively, for red, green, and blue illuminance at the L255 gray level.

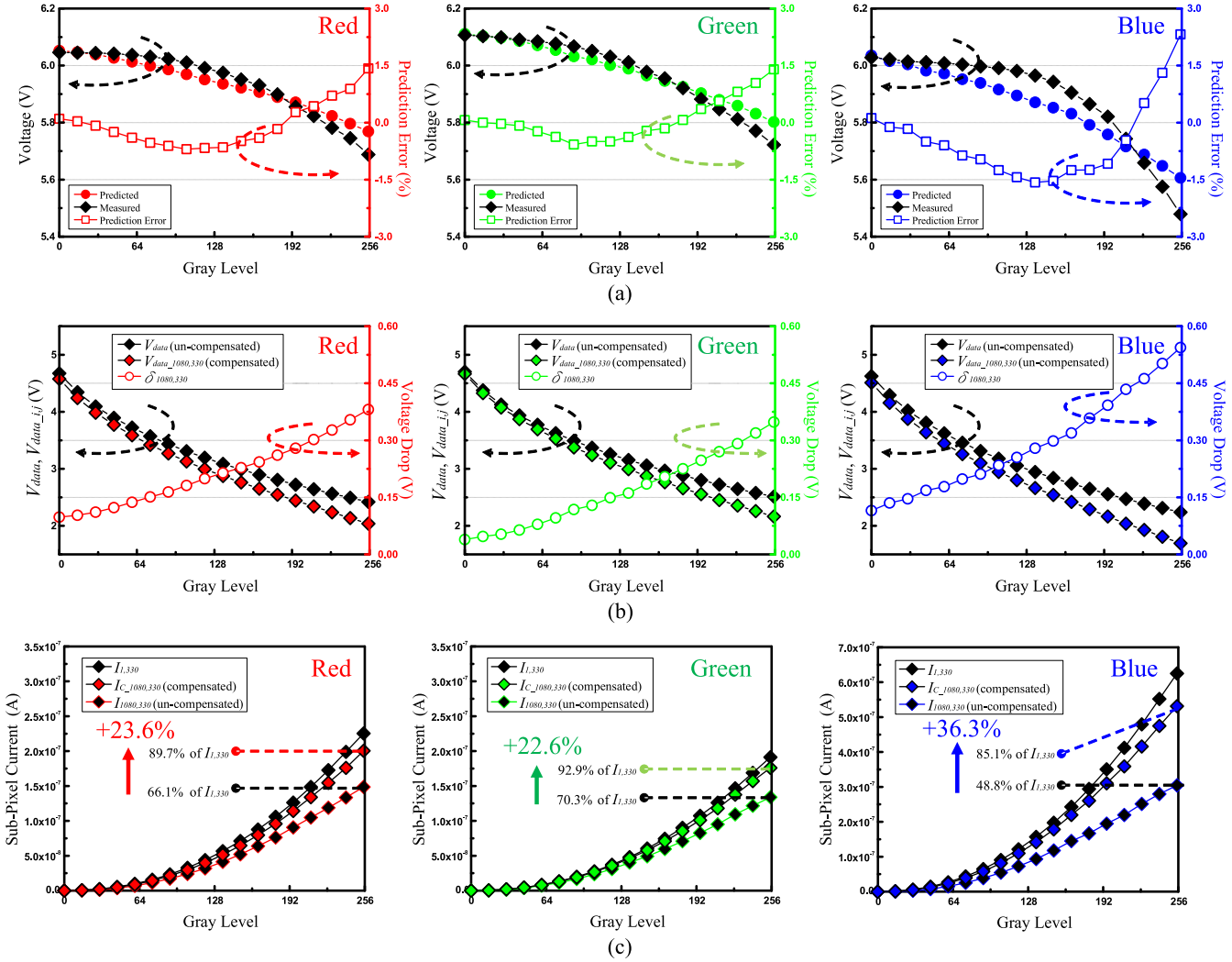


FIGURE 8. **(a) The predicted, measured voltages $V_{i,j}$'s and their corresponding prediction errors at sub-pixels at row 1080 and column 330; (b) V_{data}'s, $V_{data\_1080,330}$'s, and their $\delta_{1080,330}$'s for compensation; (c) The desired, non-dropped OLED current, $I_{1,330}$'s, the dropped and uncompensated $I_{1080,330}$'s, and the compensated $I_{C\_1080,330}$'s, for different pixels of red-, green-, and blue-images at varied gray levels.**

B. IMPLEMENTING COMPENSATION INTO A PANEL TO INCREASE OVERALL BRIGHTNESS UNIFORMITY

With the IR-drop model and the compensation scheme established successfully, a display system in a 14-inch FHD AMOLED panel was built with the compensation implemented, the associated computation of which is illustrated in Fig. 6, where the voltage drops at sub-pixels are first calculated by Eq. (13), then $\delta_{i,j}$'s, are stored in a LUT and used to derive the corresponding $V_{data\_i,j}$'s by Eq. (14) for compensating IR-drop in the illuminated panel. The derived $V_{data\_i,j}$'s are next delivered to each sub-pixel. Then the brightness uniformities of the panel are measured as illuminated with red-, green- or blue-images at the L255 grays. Based on the measurement at 9 points on the panel, the locations of which are shown in Fig. 9, the brightness uniformity can be evaluated following [26]

$$\text{Brightness Uniformity} = \frac{\text{minimum}(lum_1, \ldots, lum_9)}{\text{maximum}(lum_1, \ldots, lum_9)} \times 100\%, \tag{16}$$

where lum_1, ..., and lum_9 are the measured luminances at pt.-1, ..., and 9, respectively. Figs 10 give the photos showing the illuminated panels, where it can be clearly seen that with proposed compensation based on the built IR-drop model implemented, the brightness uniformities are successfully increased from 55.6% to 77.3%, 60.6% to 82.1%, and 47.3% to 82.6%, respectively, for red-, green-, and blue-images displayed at L255 gray, with their **significant increases of 21.7%, 21.5%, and 35.3% in uniformity**. Note that despite the improvements, the measured images in Figs. 10 are not compensated to 100% of perfect brightness uniformity. This is due to the process variations of TFTs used for constructing the pixel circuit, especially the threshold drifts of the drive TFTs in pixels. To solve the problem, effective pixel circuits [1]–[17] and external drive circuits [18]–[22] were proposed to compensate the variations, which are actually compatible with the IR-drop compensation proposed by this study, since V_{data} can be adjusted first by Eq. (15), then adjusted again by those [1]–[17] to compensate threshold

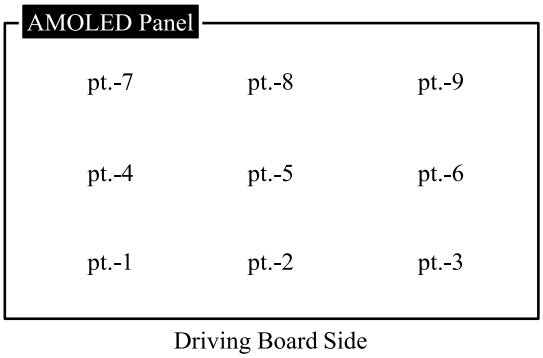


FIGURE 9. **The nine points where the luminance uniformity of an AMOLED panel is measured [26].**

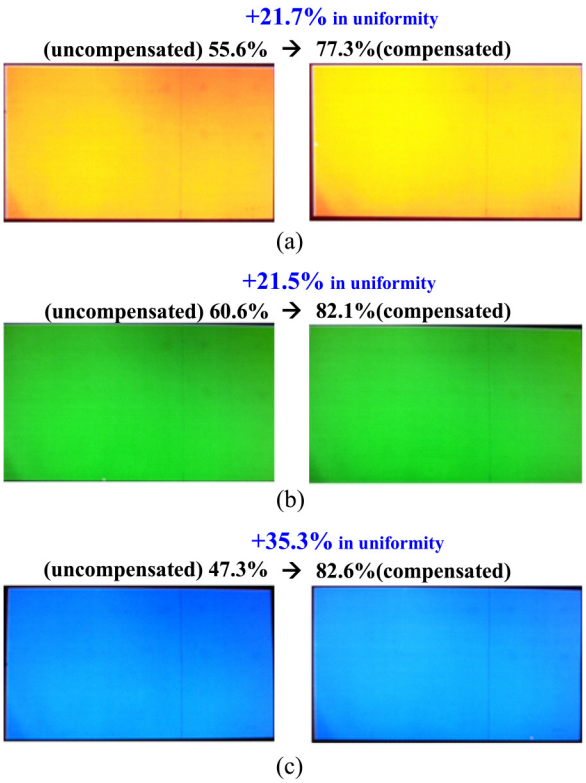


FIGURE 10. **The increased brightness uniformity of a 14-inch FHD AMOLED panel illuminating (a) red-, (b) green-, and (c) blue-images at L255 gray level.**

drifts, without performance compromised for compensating both IR-drop and threshold drifts.

IV. CONCLUSION

A new modeling technique via the equivalent circuitry is proposed by this study to predict the IR-drop phenomenon of medium- or large-sized AMOLED panels. The built model is in result in a vector-matrix form, which can be solved to predict the IR-drop in actual voltage biases on sub-pixels. The prediction precision of the model was further validated successfully based on experimental data of pixel biases and currents. With the model ready, the compensation was next carried out by elevating pixel grey levels via V_{data} to result in the originally designated, non-dropped OLED currents at pixels, successfully reducing the brightness non-uniformity of an AMOLED panel due to IR-drop. The aforementioned compensation was realized via a LUT in a 14-inch FHD AMOLED panel for performance validation. The panel was illuminated at L255 gray for red-, green-, and blue-images, while the biasing voltages and uniformity levels at edges and corners of the panel are measured. In result, the averaged errors of predicting biasing voltages are as low as 1.50%, 1.49%, and 2.44%, respectively, for red, green, and blue images displayed at the gray level of 255, respectively. With the proposed compensation implemented, the uniformity is improved significantly from 55.6% to 77.3%, 60.6% to 82.1%, and 47.3% to 82.6% for red-, green-, and blue-images displayed at L255 gray, respectively; that is, substantial improvements of 21.7%, 21.5%, and 35.3% in brightness uniformity, clearly showing the effectiveness of the built model and proposed compensation scheme.

APPENDIX

Based on Eq. (2), the current-balance equations for the pixels at display edges and corners can be derived and shown below.

1) *Equations for the sub-pixels at upper edge:*

$$-V_{m,j}\left(\frac{1}{R_v}+\frac{2}{R_h}+\frac{1}{R_{ext}}\right)+V_{m-1,j}\left(\frac{1}{R_v}\right)+V_{m+1,j}\left(\frac{1}{R_{ext}}\right)+V_{m,j-1}\left(\frac{1}{R_h}\right)+V_{m,j+1}\left(\frac{1}{R_h}\right)=I_{m,j}\quad i=m;\quad j=2,\ldots n-1, \tag{17}$$

2) *Equations for the sub-pixels at lower edge:*

$$-V_{1,j}\left(\frac{1}{R_v}+\frac{2}{R_h}+\frac{1}{R_{ext}}\right)+V_{0,j}\left(\frac{1}{R_{ext}}\right)+V_{2,j}\left(\frac{1}{R_v}\right)+V_{1,j-1}\left(\frac{1}{R_h}\right)+V_{1,j+1}\left(\frac{1}{R_h}\right)=I_{i,j}\quad i=1;\quad j=2,\ldots n-1, \tag{18}$$

3) *Equations for the sub-pixels at left edge:*

$$-V_{i,1}\left(\frac{2}{R_v}+\frac{1}{R_h}+\frac{1}{R_{ext}}\right)+V_{i-1,1}\left(\frac{1}{R_v}\right)+V_{i+1,1}\left(\frac{1}{R_v}\right)+V_{i,0}\left(\frac{1}{R_{ext}}\right)+V_{i,2}\left(\frac{1}{R_h}\right)=I_{i,1}\quad i=2,\ldots m-1;\quad j=1, \tag{19}$$

4) *Equations for the sub-pixels at right edge:*

$$-V_{i,n}\left(\frac{2}{R_v}+\frac{1}{R_h}+\frac{1}{R_{ext}}\right)+V_{i-1,n}\left(\frac{1}{R_v}\right)+V_{i+1,n}\left(\frac{1}{R_v}\right)+V_{i,n-1}\left(\frac{1}{R_h}\right)+V_{i,n+1}\left(\frac{1}{R_{ext}}\right)=I_{i,n}\quad i=2,\ldots m-1;\quad j=n, \tag{20}$$

5) *Equations for the sub-pixels at corners:*

$$-V_{1,1}\left(\frac{1}{R_v}+\frac{1}{R_h}+\frac{2}{R_{ext}}\right)+V_{0,1}\left(\frac{1}{R_{ext}}\right)+V_{2,1}\left(\frac{1}{R_v}\right)+V_{1,0}\left(\frac{1}{R_{ext}}\right)+V_{1,2}\left(\frac{1}{R_h}\right)=I_{1,1}\quad i=1;\quad j=1, \tag{21}$$

$$-V_{m,1}\left(\frac{1}{R_v}+\frac{1}{R_h}+\frac{2}{R_{ext}}\right)+V_{m-1,1}\left(\frac{1}{R_v}\right)+V_{m+1,1}\left(\frac{1}{R_{ext}}\right)+V_{m,0}\left(\frac{1}{R_{ext}}\right)+V_{m,2}\left(\frac{1}{R_h}\right)=I_{m,1}\quad i=m;\quad j=1, \tag{22}$$

$$-V_{1,n}\left(\frac{1}{R_v}+\frac{1}{R_h}+\frac{2}{R_{ext}}\right)+V_{0,n}\left(\frac{1}{R_{ext}}\right)+V_{2,n}\left(\frac{1}{R_v}\right)+V_{1,n-1}\left(\frac{1}{R_h}\right)+V_{1,n+1}\left(\frac{1}{R_{ext}}\right)=I_{1,n}\quad i=1;\quad j=n, \tag{23}$$

$$-V_{m,n}\left(\frac{1}{R_v}+\frac{1}{R_h}+\frac{2}{R_{ext}}\right)+V_{m-1,n}\left(\frac{1}{R_v}\right)+V_{m+1,n}\left(\frac{1}{R_{ext}}\right)+V_{m,n-1}\left(\frac{1}{R_h}\right)+V_{m,n+1}\left(\frac{1}{R_{ext}}\right)=I_{m,n}\quad i=m;\quad j=n. \tag{24}$$

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PAUL C.-P. CHAO (Senior Member, IEEE) received the Ph.D. degree from Michigan State University, USA, and he was with Chrysler Corp., Detroit, USA. He joined National Yang-Ming Chiao-Tung University (NYCU), Taiwan, where he is currently a University Distinguished Professor of the Electronics and Electrical Engineering Department. He has published more than 450 peer-reviewed papers (books, journal papers, conferences, and reports) and 38 patents. His research interests focus on sensors, actuators, and their interface circuitry. He was the recipient of the 1999 Arch T. Colwell Merit Award from Society of Automotive Engineering, Detroit, USA; The 2019 Technical Achievement Award, IEEE Sensors Council; The 2017 Presidential Outstanding Professor of Engineering in Nation (Taiwan) (awarded by the President of the Nation in the Presidential House of Taiwan); Two 2017 Future Technology Awards (Taiwan Oscar Invention Award) from Ministry of Science and Technology (MOST), Taiwan Government; the 2018 Outstanding Professor of Electrical Engineering in Nation, Taiwan, National Association of Electrical Engineering, Taiwan; the Outstanding Research Award of MOST, 2018; the Technical Achievement Award, Sensors Council, IEEE, USA, in 2019; the Distinguished Institutional Award, American Society of Mechanical Engineering (ASME), USA, in 2019. The Best Paper Award of the ASME ISPS Conference 2019. He has served as the University Associate Vice President of NYCU for academic affairs from 2009 to 2010 and Research and Development in 2015 and also received the award of the 2017 Best Topical Editor, Runner up, IEEE SENSORS JOURNAL. He is currently a Topical Editor of IEEE SENSORS JOURNAL and IEEE INTERNET OF THINGS JOURNAL. He was a Distinguished Lecturer for IEEE Sensors Council from 2018 to 2020. He is an ASME Fellow.

SHIH-SONG CHENG received the B.S. degree in electrical engineering from National Dong Hwa University, Hualien County, Taiwan, in 2007, and the M.S. degree in electronics and electrical engineering from National Yang-Ming Chiao-Tung University, Hsinchu, Taiwan, in 2010, where he is currently pursuing the Ph.D. degree in electronics and electrical engineering. His research interests focus on display electronics and optoelectronics of active-matrix electroluminescent displays, including pixel circuitry, driving scheme, gate driver on array, and image quality improvement.

CHIU-HAO CHEN received the M.S. degree in electronics and electrical engineering from National Yang-Ming Chiao-Tung University, Hsinchu, Taiwan, in 2011. His research interests focus on thin-film transistors and active-matrix organic light-emitting diode display.

KUEI-YU LEE received the B.S. degree in electrical engineering from Taiwan Ocean University, Keelung, Taiwan, in 2007, and the M.S. and Ph.D. degrees in electronics and electrical engineering from National Yang-Ming Chiao-Tung University, Hsinchu, Taiwan, in 2009 and 2012, respectively. His research interests focus on thin-film transistors and active-matrix organic light-emitting diode display.