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Low Switching Loss Split-Gate 4H-SiC MOSFET With Integrated Heterojunction Diode

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ABSTRACT A 4H-SiC MOSFET with p-type region injection and integrated split gate and heterojunction diode is proposed in this paper. Compared with the conventional MOSFET, the proposed structure has a lower on-resistance and switching loss. And the gate oxide layer has been well protected by the p-type region, which reduces the electric field in gate oxide layer at the off-state. The on-resistance of device can be greatly reduced by increasing the doping concentration of current spreading layer and will not cause a huge electric field in gate oxide layer. The specific on-resistance is decreased by about 27.8% and the static characteristic ($BV^2/R_{on,sp}$) of the device is improved about 37.3%. SiC material has a high third quadrant turn-on voltage due to its wide band gap characteristics. The use of heterojunction integration can take place of parasitic body diode and reduce its turn-on voltage, avoid the bipolar degradation effect, and improves the reverse recovery characteristics. To evaluate the dynamic performance, the reverse transmission capacitance (C_{rss}) and gate-drain charge (Q_{gd}) of the proposed structure have been studied in this paper via numerical simulations. Based on the simulation, the HF-FOM ($C_{rss}\times R_{on,sp}$) and HF-FOM^2 ($Q_{gd}\times R_{on,sp}$) of the proposed structure are decreased by about 87% and 86%, respectively. Meanwhile, the reverse turn-on voltage and reverse recovery characteristics are also improved, and the total energy loss decreases by about 37.3%.

INDEX TERMS Silicon carbide, specific on-resistance, switching energy loss, figure of merit, heterojunction diode.

I. INTRODUCTION

Sic has good material properties, such as wide band gap, high electron mobility, high breakdown electric field, and stable physical and chemical properties [1]–[3]. It is widely used in power semiconductor devices and has excellent application prospects. Compared with the silicon insulated gate bipolar transistor (Si IGBT), the SiC metal oxide semiconductor field effect transistor (MOSFET) has a faster switching speed and a lower switching loss [4]–[9], [30].

Planar gate power MOSFET is widely used for high-speed switching applications since it features a lower reverse transfer capacitance (C_{rss}) compared with trench MOSFET. The split-gate (SG) MOSFET improves the switching speed and decreases the C_{rss} by decreasing the overlap area of the gate to the drain electrode [10]. However, the use of SG MOSFET will usually increase the resistance of the device under the same cell size [11]–[13], and make the electric field crowding in the gate oxide under high voltage [26], which will affect the reliability of the device for long-term use. The values of HF-FOM ($C_{rss}\times R_{on,sp}$) and HF-FOM^2 ($Q_{gd}\times R_{on,sp}$) are usually compared to measure the performance of the device under high-frequency operation [14]–[15]. These values are not only related to the C_{rss} and Q_{gd}, but also related to the specific on-resistance ($R_{on,sp}$). How to decrease the $R_{on,sp}$ without degenerating other performance also needs to be studied.

Due to the wide band gap of SiC material, the forward turn-on voltage (V_F) of the third quadrant body diode is large, which usually requires an anti-parallel Schottky barrier diode (SBD) as a freewheeling diode (FWD), will increase the chip area, introduce stray inductance and increase energy loss. Some literature studies have demonstrated the

integration of SBD in the structure to reduce the third quadrant conduction voltage drop and improve the reverse recovery characteristics [23], [28]. But, when the SBD structure is close to the gate electrode, it will bring metallization pollution and affect the reliability of the device [25]. And due to the mirror force effect and tunneling effect, it will bring a large leakage current, and degenerate the performance of the device.

Heterojunction diode (HJD) is composed of polysilicon and SiC, which is expected to obtain good performance due to its unipolar effect similar to SBD. Some researches have been reported, Tanaka *et al.* [30] fabricated heterojunction diodes with P+-polysilicon on the n-type 4H-SiC epitaxial layer, showing that HJD has ultra-low V_{on} and lower leakage current in 2005. Pérez-Tomás *et al.* [31] first fabricated and analyzed the characteristics of n-n Si/SiC HJDs in 2007. Ni *et al.* [32] first fabricated trench MOS with integrated HJD in 2014. An and Hu [33] simulated a separated gate trench MOS integrated with HJD, indicating that HJD can improve the reverse recovery characteristics, and can inhibit the conduction of the pin body diode in 2019. Therefore, HJD is considered a new option to improve the device's overall performance.

In this paper, we propose a new 1200 V class 4H-SiC MOSFET integrated heterojunction diode with a p-type polysilicon region between split gate (HJD-SG-MOS). The HJD of the proposed structure is composed of P+-polysilicon and N-4H-SiC. The bottom of the P+-polysilicon is at the same height as the bottom of the gate oxide layer, which can effectively reduce the electric field at the gate corner and ensure the reliability of gate oxide layer. In addition, the HJD enables the device to work under the high doping concentration of current spreading layer (CSL), thus the $R_{on,sp}$ can be effectively reduced without changing chip area. The proposed structure has a higher static performance and lowers dynamic performance compared to the conventional structure. The integrated HJD can reduce the hole injection efficiency, due to the lower barrier height of the electron compared with the hole. The HJD, which turns on before the parasitic pin diode, can reduce the V_F and improve the reverse recovery characteristics. The gate oxide corner has a low electric field and is effectively protected thanks to the electric field shielding effect of the p-type region and the p-base region, which improves the reliability of the device [16]–[21]. To illustrate the superiority of HJD-SG-MOS, we chose the conventional MOSFET (Con-MOS) as a reference. The static and dynamic characteristics of the HJD-SG-MOS and Con-MOS are verified by simulations using the SILVACO Atlas TCAD [20].

II. DEVICE STRUCTURE AND ENERGY BAND ANALYSIS

Fig. 1 shows the cross-section of the Con-MOS and HJD-SG-MOS. The two structures have the same cell thickness and width, and the doping concentration of drift is 8×10^{15} cm^{-3}. The doping concentration of p-base is 2×10^{17} cm^{-3} for both structures, and the depth of p-base is 1.2 μm. The

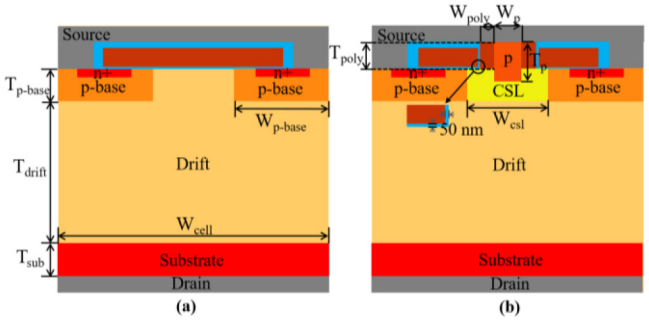

FIGURE 1. Schematic cross sections of (a) Con-MOS, which is used for reference in this article, and (b) HJD-SG-MOS.

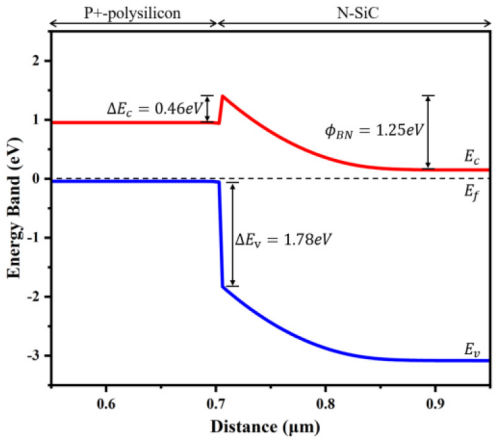

FIGURE 2. Energy-band diagram of P+-polysilicon/N-SiC heterojunction at thermal equilibrium.

thickness of drift layer for the Con-MOS and HJD-SG-MOS is 10 μm. The channel oxide layer thickness of HJD-SG-MOS and Con-MOS is 50 nm, and the thickness of oxide layer beside the polysilicon of HJD-SG-MOS is also 50 nm, and the external oxide layer is 0.5 μm, which can be formed by thermal oxidation and SiO_2 chemical vapor deposition [22]. The planar channel length is set 0.8 μm and channel mobility is about 20 cm^2/Vs. The doping concentration of the p-type ion-implantation region and P+-polysilicon in the HJD-SG-MOS is 1×10^{18} cm^{-3} and 1×10^{20} cm^{-3}, respectively. The integration of HJD is composed of p-type polysilicon and n-type 4H-SiC, which is located between the split gate. Meanwhile, due to the JEFT effect formed by p-type region and p-base region, additionally P+-polysilicon is much stronger than that of Con-MOS, therefore it is decided to add CSL to HJD-SG-MOS to reduce the on-resistance. In this structure, the gate corner is the same height as HJD, this greatly reduces the electric field of the gate corner in the off-state of the device. Detailed parameters are shown in Table 1.

Fig. 2 shows the energy band of the P+-polysilicon/N-SiC heterojunction diode at thermal equilibrium. The energy gap of the conduction band is 0.46 eV and the energy band gap of valence bands is 1.78 eV. The simulation result of

TABLE 1. Device parameter in simulation.

PARAMETER	VALUE
Thickness N+ source junction, T_{N+}	0.2 μm
Thickness of drift, T_{drift}	10 μm
Thickness of substrate, T_{sub}	1 μm
Thickness of p-base, $T_{p\text{-}base}$	1.2 μm
Thickness of p-type region, T_p	1.2 μm
Thickness of P+-polysilicon, T_{poly}	0.7 μm
Width of cell, W_{cell}	10 μm
Width of p-base, $W_{p\text{-}base}$	3.5 μm
Width of CSL, W_{CSL}	3 μm
Width of P+-polysilicon, W_{poly}	0.5 μm
Width of p-type region,W_p	1 μm
Doping concentration of CSL, N_{CSL}	6×10^{16} cm^{-3}
Doping concentration of substrate, N_{sub}	1×10^{19} cm^{-3}
Doping concentration of drift, N_{drift}	8×10^{15} cm^{-3}
Doping concentration of p-base, $N_{p\text{-}base}$	2×10^{17} cm^{-3}
Doping concentration of p-type region, N_p	1×10^{18} cm^{-3}

the energy band is similar to that of previously reported literature [3]–[33], which shows it's reasonable. The barrier height for electron can be calculated as the peak value of conduction energy minus the Fermi level energy (E_f), which is 1.25 eV. The electrons have a much lower barrier height compared with holes, this allows electrons easily flow from N-SiC to P+-polysilicon, but holes can hardly flow from P+-polysilicon to N-SiC. Due to the low barrier height for electrons, the V_F of HJD can be reduced, improving the reverse recovery characteristics of the device. Meanwhile, the p-type ion-implantation region can reduce the electric field in the polysilicon and gate oxide layer to avoid dynamic degradation.

III. NUMERICAL SIMULATION AND RESULT ANALYSIS

In this section, we use the SILVACO Atlas to simulate the characteristics of the proposed structure and conventional structure and analyze the result which is based on semiconductor theory. In this simulation, some physical models are added, including the Selberherr impact ionization model (impact Selb), the parallel electric field dependence model (fldmob), the concentration and temperature dependent model (analytic), the Shockley-Read-Hall recombination model (SRH), the auger recombination model (auger), the incomplete ionization model (incomplete), and the bandgap narrowing model (BGN) [19], [24].

A. EFFECT OF KEY STRUCTURE PARAMETERS OF HJD-SG-MOS

The high doping concentration of CSL can effectively help the diffusion of electrons from the source to the drain.

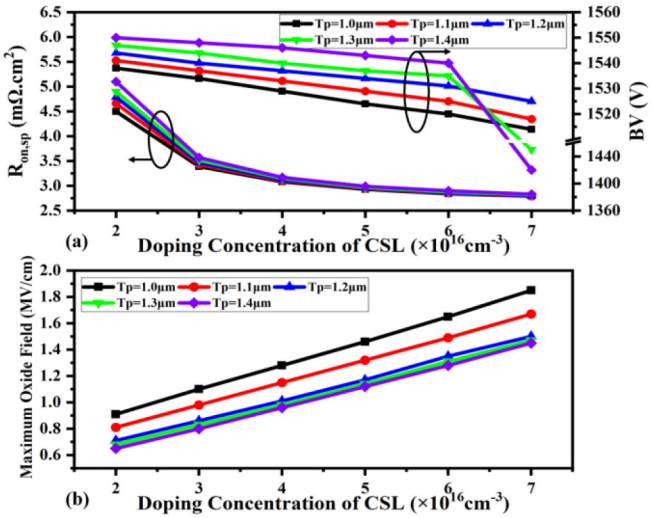

FIGURE 3. The influence of the doping concentration of CSL and the thickness of p-type region on (a) $R_{on,sp}$, and (b) maximum electric field in the oxide at V_{ds} = 1200 V and V_{gs} = 0 V.

But will increase the electric field in gate oxide, polysilicon, and the p-type region at off-state. And the excessive concentration of CSL will cause an electric field crowding phenomenon, which may lower the breakdown voltage. To alleviate this phenomenon, and makes a good shielding effect, the parameters of CSL and the added p-type region should be considered.

Fig. 3 shows the influence of the doping concentration of CSL and the thickness of p-type region (Tp) on the $R_{on,sp}$ and the maximum oxide field (E_{ox}) at drain bias of 1200 V. When the low concentration of CSL is low, the larger the Tp, the larger the $R_{on,sp}$ of the device, as shown in Fig. 3(a). The electric field shielding effect formed by the p-type doping region can be stronger with a larger Tp, as shown in Fig. 3(b). With the concentration of CSL increasing, the higher electron concentration increases the current path between the source to the drain, effectively reducing the JEFT effect, decreasing $R_{on,sp}$ [29]. But at the same time, E_{ox} is almost linear variation. Tp has little effect on the on-resistance of the device under high concentration of CSL, when the doping concentration is lower than 7×10^{16} cm^{-3}, the larger Tp can undertake electric field more uniform and improve BV. With a higher doping concentration of CSL, the BV will decrease gradually.

When the doping concentration of CSL is 7×10^{16} cm^{-3} and Tp is 1.3 μm or 1.4 μm, the electric field crowding phenomenon will appear. Fig. 4 shows the electric field distributions of HJD-SG-MOS when (a) Tp is 1.2 μm and (b) Tp is 1.4 μm at critical voltage. The critical breakdown electric field of SiC material is 3 MV/cm [7]. When Tp is 1.2 μm, the drain voltage when SiC reaches the critical electric field is 1525 V. But, while Tp is 1.4 μm, due to the p-type region will undertake a larger electric field, the critical electric field will be reached in advance,

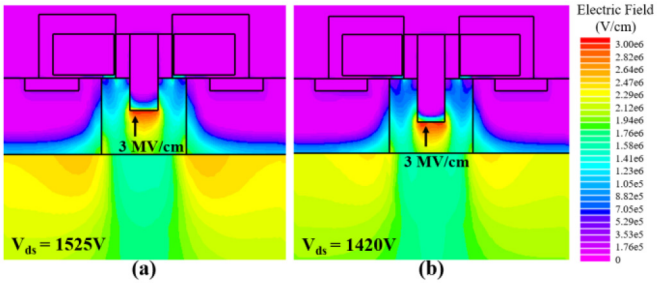

FIGURE 4. The electric field distribution of HJD-SG-MOS when (a) Tp = 1.2 μm and (b) Tp = 1.4 μm at critical voltage.

which is 1420 V. It is clear that when the doping concentration of CSL is beyond 6×10^{16} cm^{-3}, the reduction of $R_{on,sp}$ is not obvious, but BV still decreases. The figure of merit (FOM=$BV^2/R_{on,sp}$) is usually considered as a trade-off between BV and $R_{on,sp}$. When Tp is 1.2 μm and the concentration of CSL is 6×10^{16} cm^{-3}, the FOM is 811 MW/cm^2. Based on the above analysis, Tp is henceforth considered as 1.2 μm and the doping concentration of CSL is 6×10^{16} cm^{-3}.

To avoid the reduction of BV caused by electric field crowding, the width of p-type region (W_p) and the doping concentration of p-type region need further consideration. Fig. 5 shows the doping concentration of p-type region and Wp on the BV and E_{ox}. As expected, increasing the doping concentration of p-type region and Wp could decrease E_{ox}, the wider and more doping concentration of p-type doping region can form a stronger JEFT effect when the device is off-State, to effectively reduce the electric field at the gate oxide. As Fig. 5(a) shows, BV increases with the increase of doping concentration of p-type region at first, but when it reaches 9×10^{17} cm^{-3}, while Wp is 0.6 μm, the BV decreases significantly, and the electric field crowding phenomenon at the corner of p-type region degenerate the BV. As mentioned above, 3 MV/cm is considered as SiC critical electric field, when Wp is 0.6 μm and the doping concentration of p-type region is 9×10^{17} cm^{-3}, the critical electric field will be reached in advance, which is 1500 V. Wp of 1 μm and Wp of 0.8 μm don't occur electric field crowding phenomenon. The wider the width of the p-type region, the more uniform the electric field can understand, reducing the electric field distribution on the surface of the p-type region. It is worth mentioning that when the CSL doping concentration is 6×10^{16} cm^{-3}, the $R_{on,sp}$ of the HJD-SG-MOS does not change significantly with the increase of the concentration and the width of the p-type region. Considering the fabrication process of the structure, Wp between 0.8 μm and 1 μm is acceptable. Meanwhile, to avoid the electric field crowding phenomenon and to keep a good shielding effect, the doping concentration of p-type region is 1×10^{18} cm^{-3}. Based on the above analysis, Wp is considered as 1 μm and the doping concentration of p-type region is 1×10^{18} cm^{-3}.

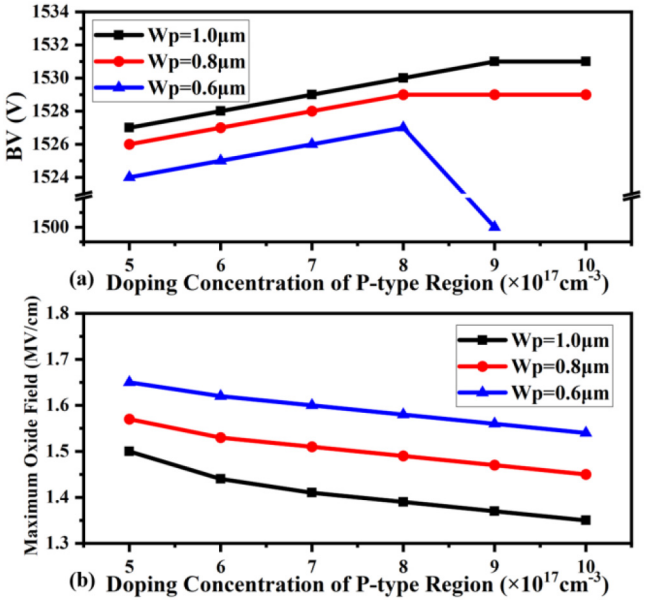

FIGURE 5. The influence of the doping concentration and the width of p-type region on (a) BV, and (b) maximum electric field in the oxide (E_{ox}) at drain bias of 1200 V.

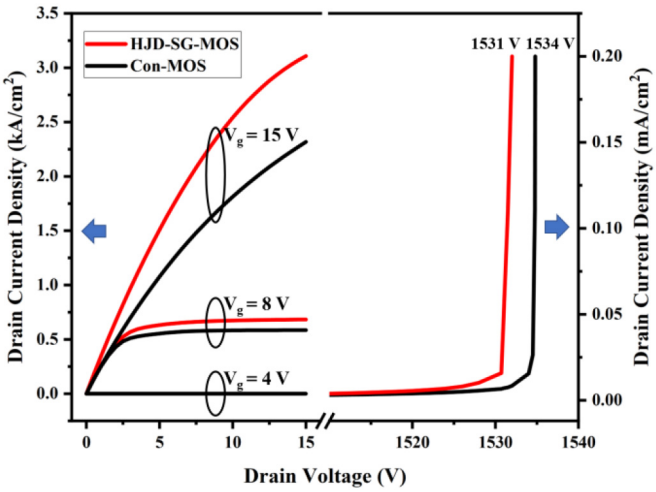

FIGURE 6. On-State output characteristic curves and off-State breakdown voltage output characteristic curves of the HJD-SG-MOS and Con-MOS.

B. COMPARISON BETWEEN TWO STRUCTURES

In the following part of this paper, we will focus on comparing the various characteristics of the two structures, such as IV characteristics, breakdown characteristics and various dynamic characteristics. Fig. 6. shows the on-State characteristic and off-State characteristic of the Con-MOS and HJD-SG-MOS, it can be calculated that the $R_{on,sp}$ of HJD-SG-MOS and Con-MOS are 2.89 m$\Omega\cdot$cm^2 and 4 m$\Omega\cdot$cm^2, respectively (V_{gs} = 15 V, V_{ds} = 1 V). The $R_{on,sp}$ decreases by 1.11 m$\Omega\cdot$cm^2, about 27.8%. Since the high concentration of CSL makes the current path wider at low drain voltages, this assists to disperse current to the drift.

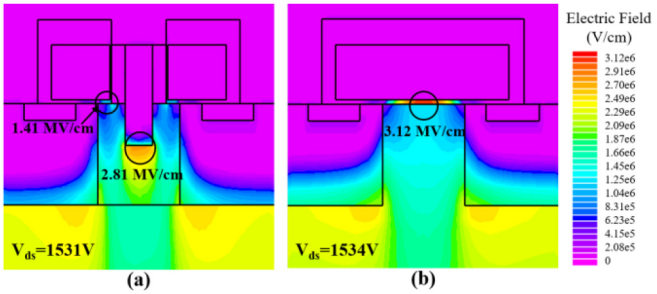

FIGURE 7. Off-State electric field contours of (a) HJD-SG-MOS and (b) Con-MOS at critical voltage.

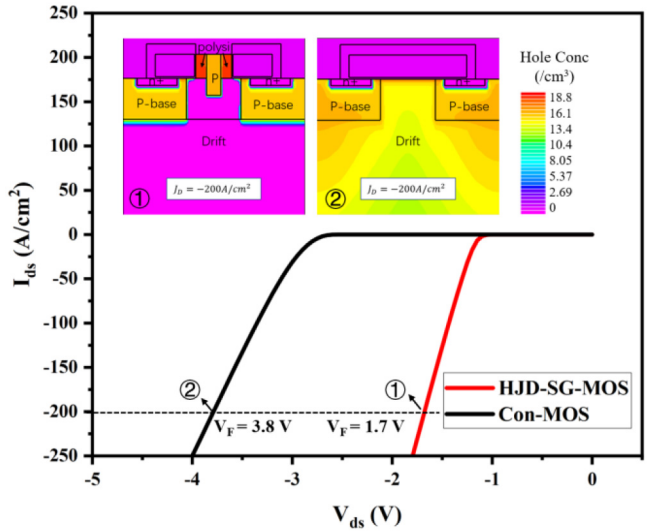

FIGURE 8. Reverse conduction I-V characteristics for the HJD-SG-MOS and Con-MOS. The inserted figures show the hole concentration distribution in the two devices at $J_D = -200$ A/cm^2.

Fig. 7 shows the off-state electric field contours of HJD-SG-MOS and Con-MOS at critical voltage. When the Con-MOS reaches critical breakdown, the huge electric field, which is exceeds 3 MV/cm, is concentrated at the oxide and this reduces the reliability of long-term use. But at HJD-SG-MOS, the bottom of P+-polysilicon and the bottom of gate oxide are at same height, and the p-type ion-implantation region can undertake electric field and decrease the electric field at polysilicon and gate oxide, the electric field in gate oxide layer at critical voltage is 1.41 MV/cm, the gate oxide layer is effectively protected.

The FOM is used to demonstrate the trade-off between BV and $R_{on,sp}$, although the HJD-SG-MOS exhibits a similar breakdown voltage (1531 V) to that of Con-MOS (1534 V), due to the reduction of $R_{on,sp}$, HJD-SG-MOS shows a better static performance than Con-MOS, and it is calculated to 811 MV/cm^2 and 588 MV/cm^2, respectively. It means that the FOM has improved by about 37.3%.

Fig. 8. Shows the reverse conduction IV characteristics of two devices at gate voltage bias −5 V, due to HJD has a low barrier height for electrons so that the HJD-SG-MOS can form an electron current at a low V_F, which flows from

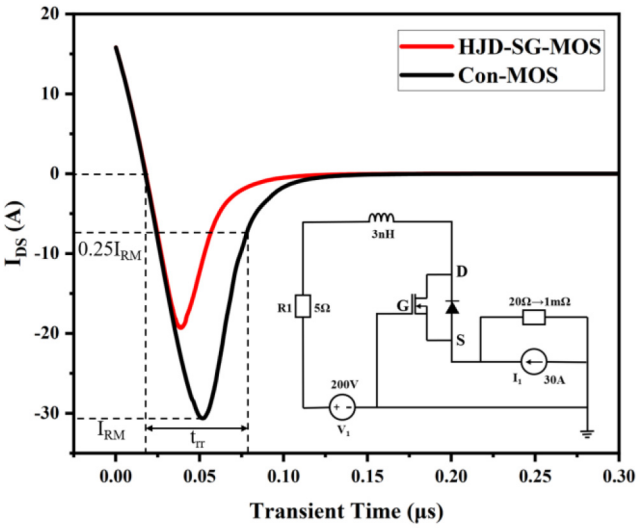

FIGURE 9. Reverse recovery characteristics of the HJD-SG-MOS and the Con-MOS. Inset: test circuit.

polysilicon to the source easily, can be turned on before p-base/n-drift body diode, and the V_F of HJD-SG-MOS and Con-MOS is 1.7 V and 3.8 V, respectively. The inserted figures show the hole concentration distribution of HJD-SG-MOS and Con-MOS at $J_d = -200$ A/cm^2. The results show that the HJD-SG-MOS has an extremely low hole concentration at drift compared to Con-MOS, which can suppress the conduction of pin diode and the bipolar degradation effect.

In order to study the reverse recovery characteristics, gate charge characteristics, and switching characteristics of devices, SPISCES and MIXEDMODE are used in the SILVACO Atlas TCAD.

Fig. 9 illustrates the reverse recovery characteristics of the two structures, the test circuit diagram is inserted into it [29]. The HJD-SG-MOS has effectively improved recovery characteristics. Compared with Con-MOS, the reverse recovery time (t_{rr}) decreased from 61 ns to 44 ns, it is a decrease of about 27.9%. Meanwhile, the peak reverses current (I_{RM}) and reverse recovery charge (Q_{rr}) decreased by 36.9% and 54.9%, respectively. As mentioned above, the proposed structure has a low hole concentration distribution at drift, so that the recombination process of minority and majority carriers can be reduced, therefore the reverse recovery characteristics are improved.

The reverse transmission capacitance (C_{rss}) influenced by the drain voltage of two devices is depicted in Fig. 10. Compared with Con-MOS, HJD-SG-MOS shows smaller C_{rss}. The HJD-SG-MOS reduces the overlapping area of gate and drain to decrease the coupling of the gate and drains, and the p-type region introduces an electric field shielding effect that can also decrease the coupling. The C_{rss} of HJD-SG-MOS and Con-MOS extracted at drain bias 800 V is 16 pF/cm^2 and 93 pF/cm^2, respectively. The HJD-SG-MOS shows a superior high-frequency figure of merit (HF-FOM), which is decreased from 372 mΩ·pF to 46.2 mΩ·pF, it is a

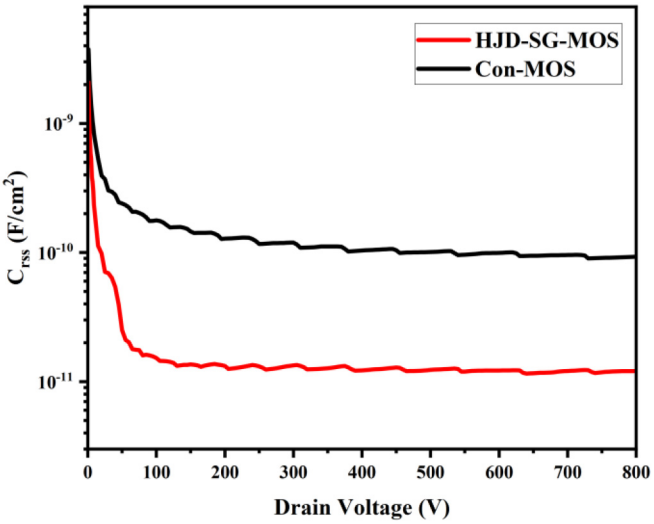

FIGURE 10. The C-V characteristics of the HJD-SG-MOS and Con-MOS at a frequency of 1MHz.

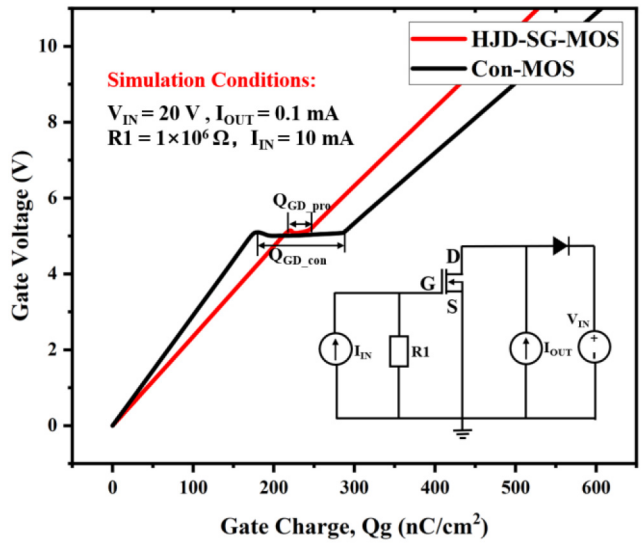

FIGURE 11. Gate charge characteristics of the HJD-SG-MOS and the Con-MOS. Inset: test circuit.

decrease of about 87%. Thus, the HJD-SG-MOS is expected to have a faster switching speed and lower switching loss.

Fig. 11 shows the gate charge (Q_g) of the two structures evaluated by the test circuit in the inset. Two structures have a similar height of miller plateau, which means they have the same threshold voltage. The gate-drain charge can be calculated by integrating the gate input current and the test time [27]. According to simulation, $Q_{gd,sp}$ values of the HJD-SG-MOS and Con-MOS are 21 nC/cm^2 and 108 nC/cm^2, respectively. Meanwhile, the miller platform of HJD-SG-MOS is shorter than that of Con-MOS, and the HF-FOM^2 decreases from 432 mΩ·nC to 60.7 mΩ·nC, it is a decrease of about 86%.

In 2017, K. Han proposed a buffer-gate region MOSFET with a high doping concentration of JEFT region (BG-MOSFET_H), which was explained by simulation and experiment [10]. A method is proposed to extend the p-type shielding region to the edge of split-gate MOSFET and add a high doping concentration of n-type region in the central region to reduce the on-resistance. This method is very interesting, BG-MOSFET_H has greatly improved the device HF-FOM and HF-FOM^2. After removing the contact resistance, the on-resistance is 6.69 mΩ · cm^2, and the HF-FOM and HF-FOM^2 are 154 mΩ·pF and 401 mΩ·nC, respectively. Compared to the conventional MOSFET (also removing the contact resistance), the HF-FOM and HF-FOM^2 have 3.4× and 3.5× smaller. The HJD-SG-MOS proposed in this paper has a lower on-resistance of 2.89 mΩ · cm^2, and the HF-FOM and HF-FOM^2 are 46.2 mΩ·pF and 60.7 mΩ·nC, respectively. The device performance has been further optimized.

Finally, the switching characteristics of the two structures are also studied. The double-pulse test circuit is used to measure the switching energy loss of two structures. The switching waveforms of the two structures are shown in Fig. 12(a). Fig. 12(c) shows the double-pulse test circuit used for testing switching performances, the gate voltage source is turned on from -5 V to 15 V. From Fig. 12 (a), we can see that HJD-SG-MOS has a shorter miller platform, which is aligned with the results indicated in Fig. 11. And it can also be seen that the switching speed of HJD-SG-MOS is much faster than Con-MOS. The turn-on energy loss and turn-off energy loss can be calculated by the integration of $I_{ds} \times V_{ds}$ and turn-on delay time or turn-off delay time, respectively [15]. Fig. 12(b) shows the switching energy loss of Con-MOS and HJD-SG-MOS. The energy loss of HJD-SG-MOS has a great improvement compared to Con-MOS, the total energy loss decreased from 78 μJ to 49 μJ, decreasing about 37.3%.

In order to show the feasibility of the proposed HJD-SG-MOS, the brief fabrication process is shown in Fig. 13. First, the epitaxial layer and the CSL are grown on the substrate in turn, as Fig. 13(a) shows. Second, the p-type region is formed by ion implantation. Third, as shown in Fig. 13(c), the inductively coupled plasma reactive ion etching (RIE) and ion-implantation are carried out to form p-base region and n+ source junction region, respectively. Fourth, RIE is used to etch both left and right sides of CSL of p-type region, as mentioned above, the width of p-type region is acceptable between 0.8 μm and 1 μm, which reduces the requirements for etching accuracy, and improves process feasibility. Fifth and sixth, the P+-polysilicon is formed by the refill and re-etch processes, as Figs. 13(e)-(f) shows. Seventh, Fig. 13(g) shows the formation process of the gate electrode, the dry thermal oxidation grows high-quality gate oxide to keep good interface quality of SiC/SiO_2 and gate control ability, then the polysilicon gate is deposited, and thick oxide is filled. Eighth, metal is deposited to form the source electrode and drain electrodes, and the complete structure is shown in Fig. 13(h).

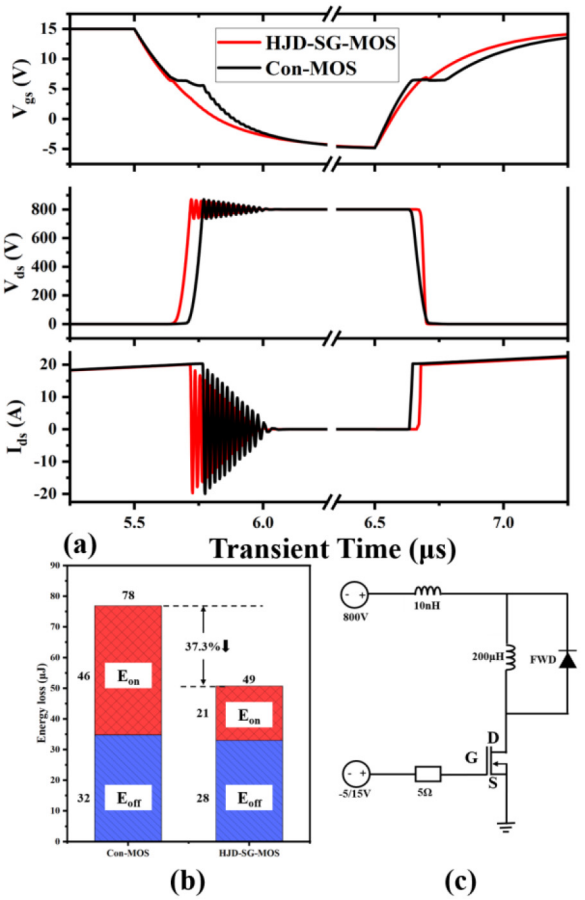

FIGURE 12. **(a) Turn-on and turn-off waveforms of two structures with test frequency 1MHz. (b) Switching energy loss of two structures. (c) Double-pulse test circuit used for switching operation.**

TABLE 2. **Characteristics of the proposed HJD-SG-MOS and Con-MOS.**

Characteristics	Con-MOS	HJD-SG-MOS
$R_{on,sp}$[a] (mΩ·cm^2)	4.00	2.89
BV (V)	1534	1531
$BV^2/R_{on,sp}$ (MW/cm^2)	588	811
E_{ox}[b] (MV/cm)	2.58	1.31
V_F[c] (V)	3.8	1.7
t_{rr} (ns)	61	44
C_{rss}[d] (pF/cm^2)	93	16
$C_{rss}\times R_{on,sp}$ (mΩ·pF)	372	46.2
Q_{gd} (nC/cm^2)	108	21
$Q_{gd}\times R_{on,sp}$ (mΩ·nC)	432	60.7
E_{total} (μJ)	78	49

[a]$R_{on,sp}$ at V_{gs} = 15 V and V_{ds} = 1 V, [b]E_{ox} is the maximum electric field in oxide at drain bias 1200 V, [c]V_F is obtained at V_{GS} = -5 V and J_D = -200 A/cm^2, [d]C_{rss} at V_{ds} = 800 V and frequency 1 MHz.

Table 2 summarizes the static characteristics and dynamic characteristics of the proposed HJD-SG-MOS and Con-MOS, including specific on-resistance ($R_{on,sp}$), breakdown voltage (BV), reverse recovery time (t_{rr}), reverse transmission capacitance (C_{rss}), gate-drain charge (Q_{gd}) and total energy loss (E_{total}). To facilitate the comparison of the overall performance of the two structures, FOM ($BV^2/R_{on,sp}$), HF-FOM ($C_{rss}\times R_{on,sp}$), and HF-FOM^2 ($R_{on,sp}\times Q_{gd}$) have also been presented.

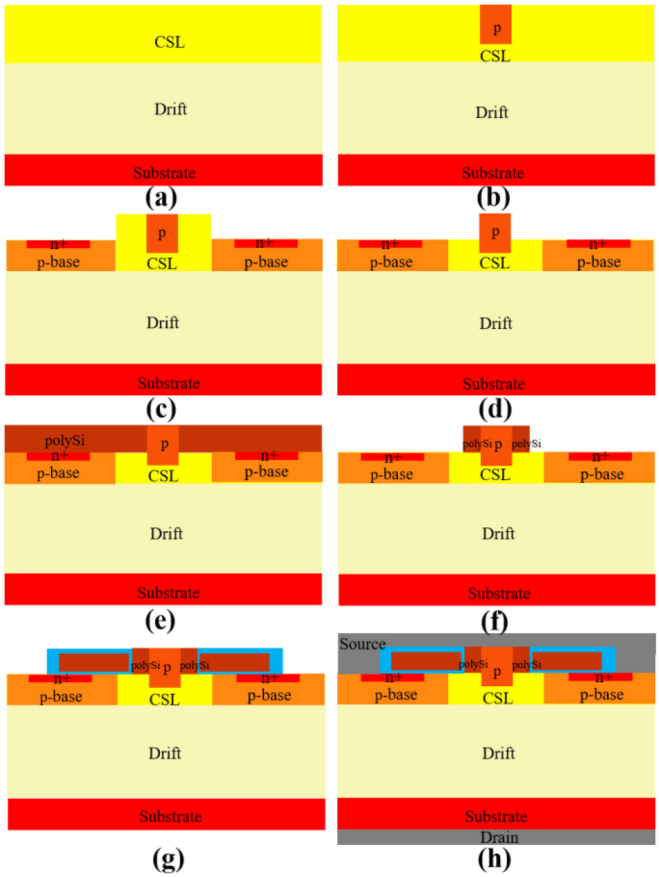

FIGURE 13. **Brief fabrication process of HJD-SG-MOS.**

IV. CONCLUSION

In this article, a 4H-SiC MOSFET integrated heterojunction diode with p-type poly-silicon region between split gates is proposed and numerically investigated using the SILVACO Atlas TCAD. The bottom of P+-polysilicon is at the same height as the bottom of the gate oxide layer and the p-type region is formed by ion implantation, which can effectively reduce the electric field in the gate oxide layer under the high concentration of CSL. The CSL can reduce the $R_{on,sp}$ of the device, which improves the static performance. The P+-polysilicon and N-SiC HJD reduces the electron barrier height and due to the hole collection effect, the reverse recovery characteristics is improved. By relying on the reduction of the overlapping area of gate and drain, it can reduce the coupling of gate and drain, and decrease the gate-drain charge and reverse transmission capacitance. Through the double-pulse circuit test, it is proved that the proposed structure improves the switching characteristics and reduces the

switching loss. The enhanced performance makes the HJD-SG-MOS a promising candidate for 1200 V class MOSFET applications.

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