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Schottky-Embedded Isolation Ring to Improve Latch-Up Immunity Between HV and LV Circuits in a 0.18 μm BCD Technology

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ABSTRACT As the high-voltage (HV) and low-voltage (LV) circuits are integrated together in a common silicon substrate, the parasitic latch-up path between neighboring HV and LV circuits with limited spacing in layout would be triggered into latch-up state to cause unrecoverable failure in the chip. In this work, the isolation ring of HV n-well (HVNW) / N-buried layer (NBL) with Schottky-embedded junction to overcome the lateral HV-to-LV latch-up path was proposed and verified in a 0.18μm HV bipolar-CMOS-DMOS (BCD) technology. From the experiment results of the proposed Schottky-embedded isolation ring, the holding voltage (Vh) in the lateral HV-to-LV parasitic latch-up path can be increased to be greater than the voltage difference between the different power supplies of the neighboring HV and LV circuits. Furthermore, the layout spacing between the neighboring HV and LV circuits can be significantly reduced to save chip area. The proposed Schottky-embedded isolation ring is a cost-effective solution to provide good latch-up immunity among the HV-to-LV circuit blocks with a short layout distance.

INDEX TERMS Holding voltage, HV n-well (HVNW), isolation ring, Latch-up, N-buried layer (NBL), Schottky embedded junction.

I. INTRODUCTION

With the development of CMOS processes, high-voltage (HV) and low-voltage (LV) circuits have between integrated together on a single chip to achieve better efficiency for complex circuit applications. With mixed-voltage circuits integrated on a chip, the parasitic lateral latch-up path was formed between the neighboring HV-to-LV circuit blocks [1]–[3]. When such a parasitic latch-up path was triggered on by external overshooting or undershooting transient noises, it would cause serious burned-out failure located between the HV-to-LV circuit blocks in the chip.

Latch-up issue is one of the essential reliability challenges in CMOS IC products [4], [5]. A variety of techniques had been reported to prevent latch-up issue, including process optimization, modified layout structure, widening the spacing between two power supply regions, etc. [6]–[8]. In order to prevent the latch-up issue in the LV circuit blocks that was triggered by the latch-up current test (I test) applied at the HV pins, the additional guard ring structure formed by the N-buried layer (NBL) with HV n-well (HVNW) was used to isolate the whole LV circuit blocks from the common p-type substrate. Therefore, the latch-up issue inside the LV circuit blocks near to the HV I/O pins can have a higher latch-up immunity. But, the chip still suffered the latch-up issue between the neighboring HV and LV circuits [2], [9], regardless of the guard ring being added.

As shown in Fig. 1, the parasitic p-n-p-n paths existed not only between the HV PNP ESD device and HV circuit block, but also between the HV PNP ESD device and LV circuit block. For the HV device applications in the BCD process, the N-buried layer (NBL) with HV N-well (HVNW) will be often biased with the different voltages in the HV and LV circuit blocks. The abnormal latch-up path between the adjacent HV and LV circuit blocks was formed by the HV (36V) PNP ESD device at the VCC pin to the guard ring formed by the NBL/HVNW that biased at VDDE of

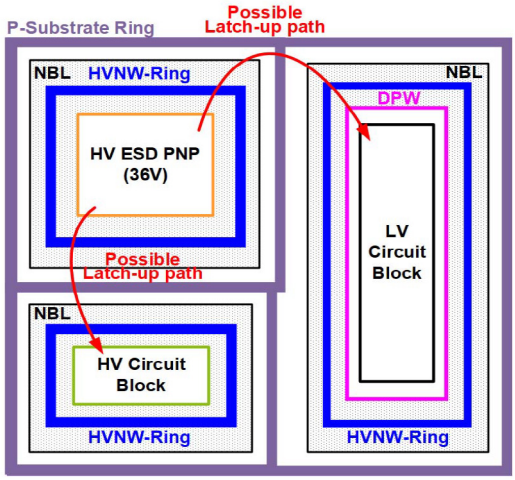

FIGURE 1. The latch-up path between adjacent lateral HV-to-LV circuit blocks with different power suppliers in a single silicon chip.

5V. This NBL/HVNW biased at VDDE was used to surround the whole LV circuit block with VDDI of 3.3V in our IC applications. A high latch-up risk from VCC (with the 36V PNP ESD device) and VDDE (to bias the isolation ring of HVNW/NBL) was found in such a mixed-voltage chip layout, if the layout distance between them was not wide enough.

The layout spacing from the HVNW in the HV circuit blocks to the HVNW/NBL of the additional guard ring structure must be separated by a large distance to prevent the parasitic latch-up path between neighboring HV and LV circuit blocks. A typical wider spacing was specified as $\sim$ 60 μm by the foundry in a 0.18μm HV bipolar-CMOS-DMOS (BCD) technology, which can provide different devices with the operating voltages from 1.8V to 45V.

Recently, the Schottky junction realized in CMOS process were reported to improve the latch-up immunity [10], [11], or to increase the holding voltage of the SCR device for on-chip ESD protection [12]. In this work, the isolation ring of HVNW/NBL with Schottky-embedded junction is proposed to improve latch-up immunity between the adjacent HV and LV circuit blocks. By connecting the isolation ring of HVNW/NBL through the Schottky junction to VDDE, the holding voltage of the abnormal latch-up path between VCC (with the PNP ESD device) and VDDE (to bias the isolation ring of HVNW/NBL) can be greater than the voltage difference between them. Thus, the separation spacing between these two HVNWs, as specified in the design rules by foundry, can be significantly reduced to save layout area in the chip.

A test chip to verify the effectiveness of the proposed Schottky-embedded isolation ring for latch-up prevention between HV and LV circuits has been drawn and fabricated in a 0.18μm BCD process. The dc curve tracer (Tek370B) is used to verify the holding voltage of the latch-up path.

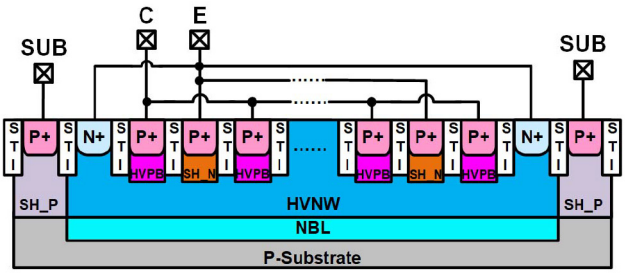

FIGURE 2. Device cross-sectional view of the isolated 36V PNP ESD device.

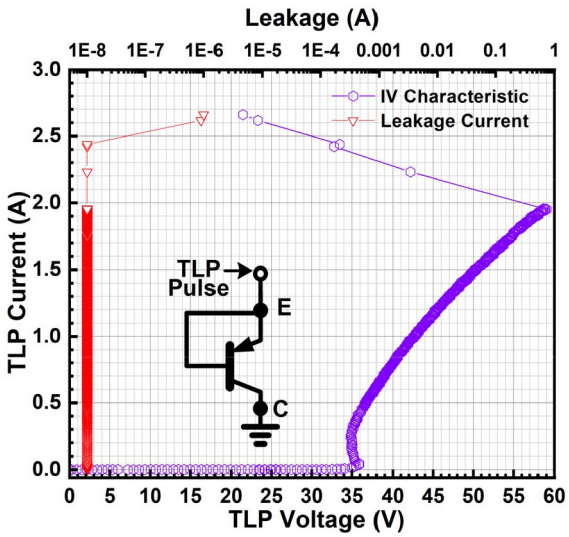

FIGURE 3. TLP-measured I–V characteristic of the isolated 36V PNP ESD device under positive emitter-to-collector TLP stress.

In addition, the latch-up current-trigger test is performed to verify the latch-up immunity, as comparing to the reference design.

II. HV PNP ESD DEVICE AND SCHOTTKY BARRIER DIODE

To investigate the effectiveness of the proposed Schottky-embedded isolation ring for latch-up prevention, several devices are studied and measured from the silicon chip in the first step, including the 36V HV PNP ESD device and the 16-V Schottky barrier diode (SBD) provided by the foundry in a 0.18-μm HV BCD technology. The PNP BJT device with non-snapback I-V behavior had been provided by foundry as on-chip ESD protection device for high-voltage applications, especially to protect the high-voltage power pin without latch-up danger in itself [13]. The cross-sectional view of an isolated 36V HV PNP ESD device is shown in Fig. 2 with total 6 fingers, in which each finger is drawn with a channel width of 120 μm and a channel length of 3 μm. The TLP-measured I–V characteristic of the isolated 36V HV PNP ESD device under positive emitter(E)-to-collector(C) TLP stress is shown in Fig. 3, where the turn-on voltage (Vt1), holding voltage (Vh), and the second breakdown current (It2) of this HV PNP ESD device are 36 V, 35 V, and $\sim$ 2.0 A, respectively.

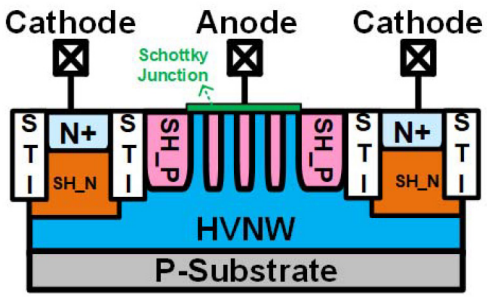

FIGURE 4. The cross-sectional view of the stand-alone 16-V Schottky barrier diode (SBD).

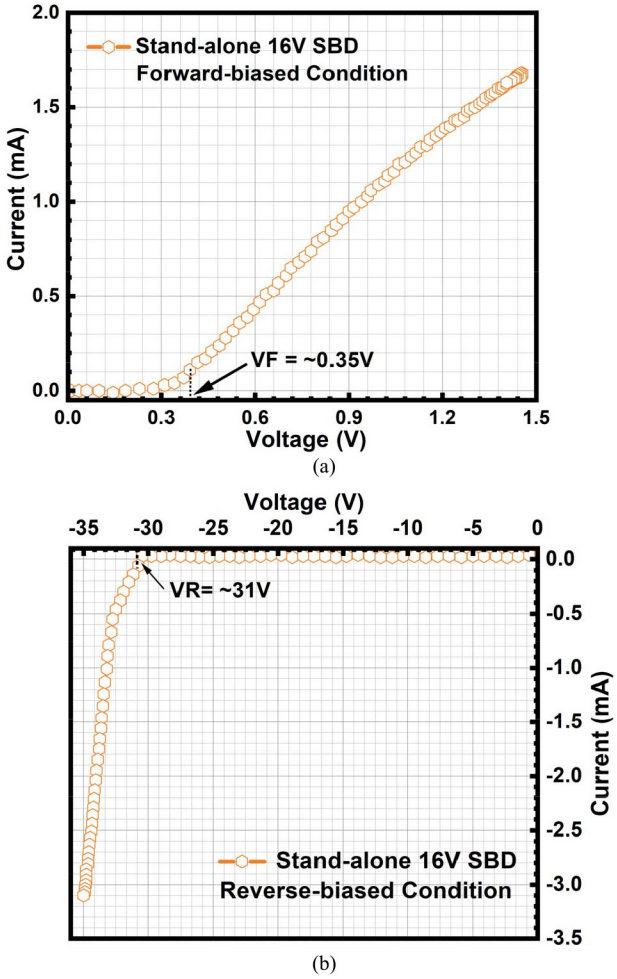

FIGURE 5. The measured dc I-V characteristic of the stand-alone SBD device under (a) forward-biased condition, and (b) reverse-biased condition.

The cross-sectional view of a stand-alone 16-V Schottky barrier diode (SBD) is shown in Fig. 4. The Schottky junction which connected to the anode port must be surrounded by the guard ring of SH_P layer (a shallow P-well with light doping for high-voltage devices), as specified by design rules, to support the desired junction breakdown voltage and device reliability [14]. By following the layout guidance and

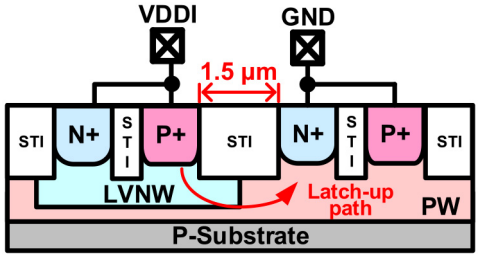

FIGURE 6. The cross-sectional view of the PNPN cell, which was used to present the parasitic p-n-p-n path inside the LV internal circuits.

design rules from foundry, a stand-alone 16-V Schottky barrier diode (SBD) has been fabricated in the given 0.18μm BCD process. The measured dc I-V characteristic of this stand-alone SBD device is shown in Fig. 5, where the forward cut-in voltage (VF) is about 0.35 V and the reversed breakdown voltage (VR) is around 31 V. This 16-V SBD will be further embedded into the isolation ring to increase the holding voltage of the abnormal latch-up path between VCC (with the PNP ESD device) and VDDE (to bias the isolation ring of HVNW/NBL) for latch-up prevention.

III. LATCH-UP TEST STRUCTURES

The parasitic p-n-p-n path inside the LV internal circuits would be triggered on to cause latch-up issue, when the trigger current is applied to the LV or HV I/O pins in the IC products [15], [16]. To verify such parasitic p-n-p-n path inside the LV internal circuits, a simple structure of PNPN cell is shown in Fig. 6 with the anode-to-cathode spacing of 1.5 μm in layout, which is drawn by considering the parasitic p-n-p-n path in the CMOS inverter cell (a typical logic gate) of a cell library provided by foundry. This simplified PNPN cell, which used to present the parasitic p-n-p-n path inside the LV internal circuits, is placed in parallel and near to the I/O pin for latch-up I-test verification.

To study the abnormal latch-up path between the adjacent HV and LV circuit blocks, three test structures (A1, A2, and A3) are arranged in the following and listed in Table 1. The PNPN cell located in the internal circuits would be triggered on to cause latch-up issue inside the internal circuits, when the latch-up trigger current is injected into the substrate from the I/O pin under the latch-up current test (I test). The test structure A1 is drawn to verify such a latch-up event, as shown in Fig. 7(a), where a VCC pin with the HV PNP ESD device is placed near to the LV internal circuits. The simple PNPN cell is used to present the parasitic p-n-p-n path in the LV internal circuits. The additional guard rings (N+/LVNW and P+) are added between the HV PNP ESD device and the PNPN cell of LV internal circuits. For injecting the latch-up trigger current into the p-type substrate to verify latch-up immunity, the additional P+ diffusion is placed in the p-type substrate and connected out to an external pin as the trigger node.

To avoid the internal latch-up issue triggering by the I/O pin under the latch-up I test, an isolation ring formed by

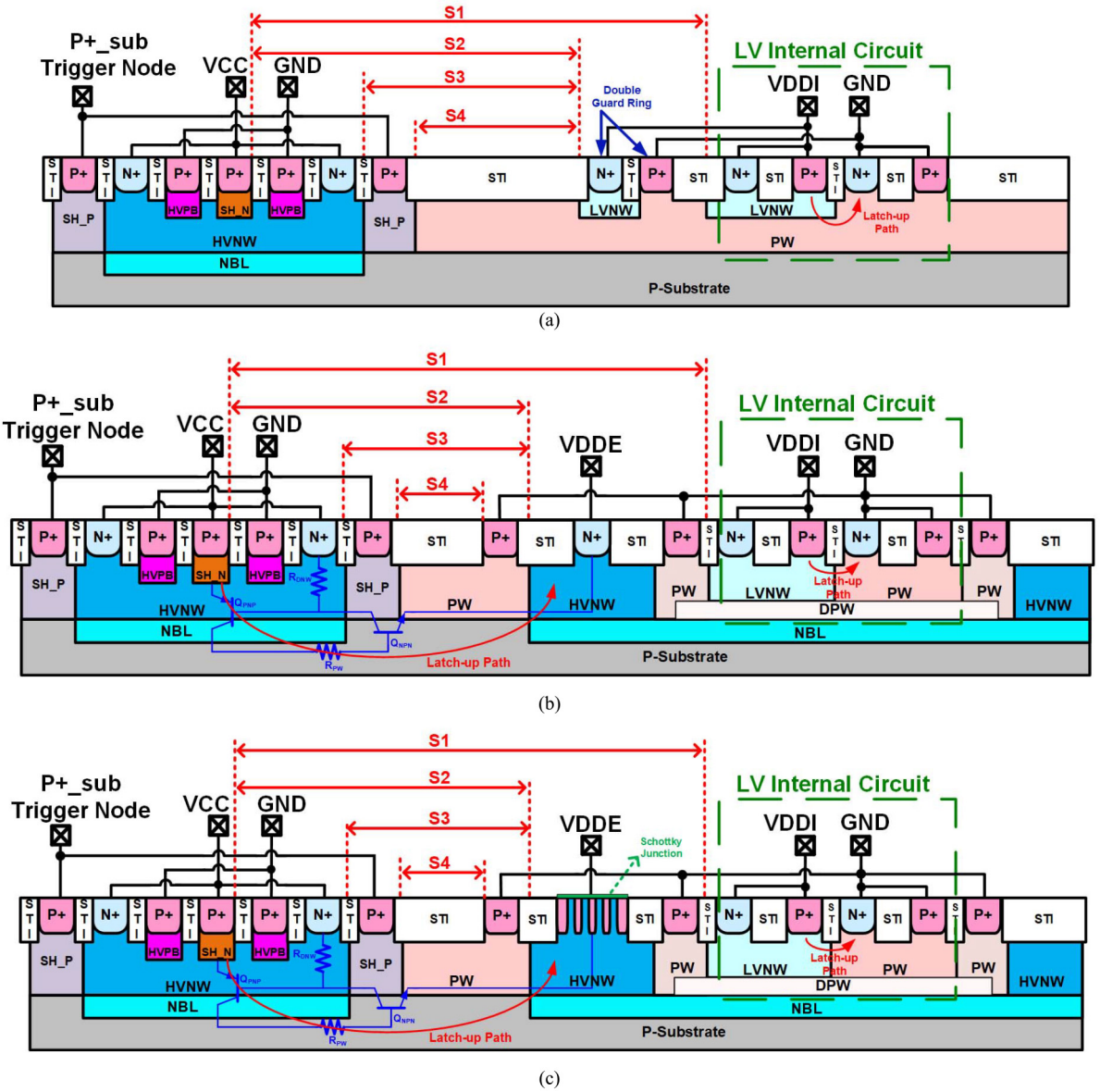

FIGURE 7. Test structures A1, A2, and A3 are drawn with the isolated 36V PNP ESD device along with (a) LV internal circuit with double guard ring, (b) LV internal circuit with isolation ring HVNW/NBL, and (c) LV internal circuit with Schottky embedded isolation ring, respectively.

TABLE 1. Combinations of latch-up test structures.

Test Structure	HV device	LV device	Guard Ring Style
A1	HV PNP ESD device	PNPN cell	N+/LVNW and P+
A2	HV PNP ESD device	PNPN cell	Isolation ring of NBL with HVNW
A3	HV PNP ESD device	PNPN cell	Schottky-embedded isolation ring of NBL with HVNW

the N-buried layer (NBL) with HV N-well (HVNW) was used to surround the whole LV internal circuits. Therefore, the PNPN cell of the LV internal circuits is isolated from the p-type substrate. The latch-up trigger current applied at the I/O pin will inject into the p-type substrate, but the injecting trigger current is isolated from LV internal circuits by the isolation ring of NBL with HVNW. Thus, the latch-up immunity of LV internal circuits against the latch-up I test applied at the I/O pins can be significantly improved. However, the isolation ring of NBL with HVNW has much deeper junction into the p-type substrate. When this isolation ring of N-buried layer (NBL) with HV N-well (HVNW) biased at VDDE is placed near to the HV PMOS (or P-type ESD device) biased at VCC, there is another extra latch-up path built from the VCC-biased P+ to the VDDE-biased NBL to cause the cross-domain latch-up event between VCC and VDDE [17].

TABLE 2. The spacing in each test structure.

Test Structure	S1 (μm)	S2 (μm)	S3* (μm)	S4 (μm)
A1	40	36	20	16.5
A2	40	30.5	14.5	8.5
A3	40	30.5	14.5	8.5
*S3 is the spacing between two adjacent HVNWs, which was originally given of ~60 μm.				

The test structure A2 is therefore drawn to verify such a cross-domain latch-up event, as shown in Fig. 7(b), where a VCC pin with the HV PNP ESD device is placed near to the LV internal circuits that is surrounded by isolation ring of N-buried layer (NBL) with HV N-well (HVNW). To verify latch-up immunity, the additional P+ diffusion is also placed in the p-type substrate and connected out to an external pin as the trigger node. When the trigger current is injected into the p-type substrate, the cross-domain latch-up path between VCC and VDDE, as well as the latch-up path inside the LV internal circuits, will be monitored to judge the latch-up occurrence. The spacing S1 in A2 test structure is kept the same as that of A1 for comparison.

To overcome the possible latch-up occurrence in the test structures A1 and A2, the simple way is to enlarge the distance between the HV PNP ESD device and the LV internal circuits in layout. For example, the spacing S3 between two HVNWs was specified to be greater than 58 μm in the given design rules by foundry. With the enlarged distance, the latch-up immunity can be improved with the penalty of cost increase (chip area). In this work, the spacing S3 is especially shortened in the layout of test structures to seek its impact on latch-up immunity, as listed in Table 2. The spacing S1 between the HV PNP ESD device and the LV internal circuits (simplified by the PNPN cell) among the test structures is kept the same of 40 μm.

To overcome the extra cross-domain latch-up path built from the VCC-biased P+ to the VDDE-biased NBL/HVNW, a Schottky junction is used to connect the isolation ring of NBL with HVNW to the VDDE. The test structure A3 with the proposed Schottky-embedded isolation ring is shown in Fig. 7(c), where a VCC pin with the HV PNP ESD device is placed near to the LV internal circuits that is surrounded by isolation ring of N-buried layer (NBL) with HV N-well (HVNW). As comparing to the test structure A2, a Schottky junction is used to connect the isolation ring (NBL with HVNW) in the test structure A3. The 16-V Schottky barrier diode (SBD) described in Section II is adopted to bias the isolation ring of NBL with HVNW to VDDE. A P+ diffusion is also placed in the p-type substrate and connected out to an external pin as the trigger node. The spacing S1 is kept the same of 40 μm for comparison under latch-up I test.

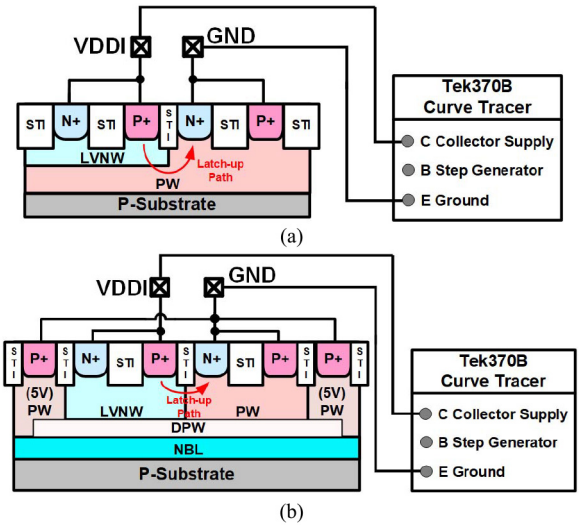

FIGURE 8. Setup to measure the latch-up DC I-V characteristics of LV internal circuit (presented by PNPN cell) of (a) the test structures A1, and (b) the test structures A2 and A3.

IV. EXPERIMENTAL RESULTS

The aforementioned three test structures (A1 ∼ A3) were fabricated in a 0.18μm HV bipolar-CMOS-DMOS (BCD) process with the 36V PNP ESD device, 16-V Schottky barrier diode, and the PNPN cell. Under latch-up test, VCC is biased at 36 V, VDDE is biased at 5 V, and VDDI is biased at 3.3 V.

A. DC I–V CURVES

To investigate the latch-up characteristics of the test. To investigate the latch-up characteristics of the test structures, the dc I–V curves of latch-up paths are measured by dc curve tracer (Tek370B) at room temperature (25 °C).

As shown in Fig. 8 with the measurement setups for the latch-up DC I-V characteristics for LV internal circuits, the collector (C) of curve tracer is applied to the VDDI node, the ground (E) is applied to the GND node. The dc I–V curves of all LV internal circuits (presented by the PNPN cell) in the test structures are measured by tracing anode-to-cathode from VDDI to GND, and the measured results are shown in Fig. 9. According to Fig. 9, the holding voltage (Vh) values of the LV internal circuits in the test structures A1, A2, and A3 are 1.02, 1.18, and 1.2 V, respectively. Moreover, the turn-on voltage (Vt1) in the test structure A2/A3 is higher than that of test structure A1, because the PNPN cell in the test structure A2/A3 is surrounded by the deep p-well (DPW) with NBL/HVNW. Since the holding voltage is only 1.02 ∼1.2 V, a large current will be conducted through the p-n-p-n path when latch-up happens under 3.3-V power supply. The occurrence of latch-up event can be observed by monitoring the current or voltage at VDDI.

The cross-domain HV-to-LV latch-up path from VCC to VDDE in the test structure A2 (A3) has been indicated in Fig. 7(b) [Fig. 7(c)]. The measurement setups to find DC I-V characteristics of latch-up path from VCC to VDDE are

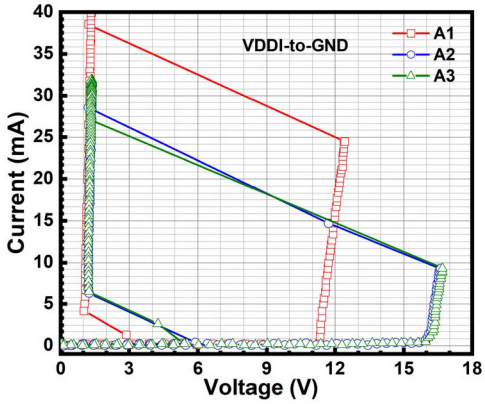

FIGURE 9. The measured DC I-V characteristics of the PNPN cell (LV internal circuits) in the test structures A1, A2, and A3.

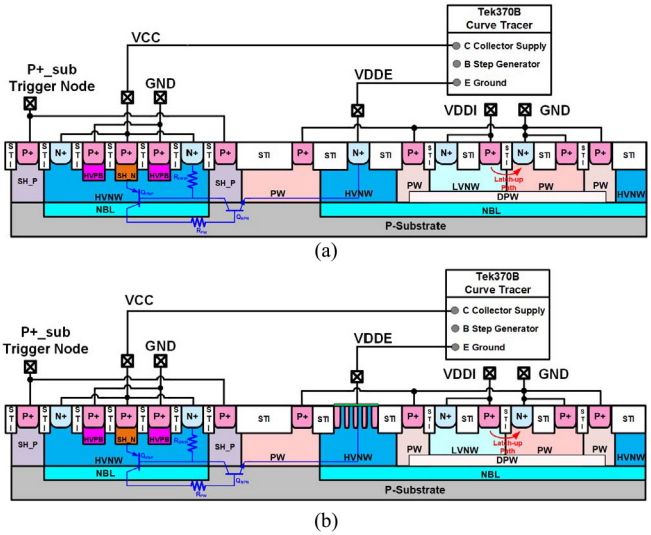

FIGURE 10. Measurement setups to find DC I-V characteristics of latch-up path from VCC to VDDE in (a) the test structure A2, and (b) the test structure A3.

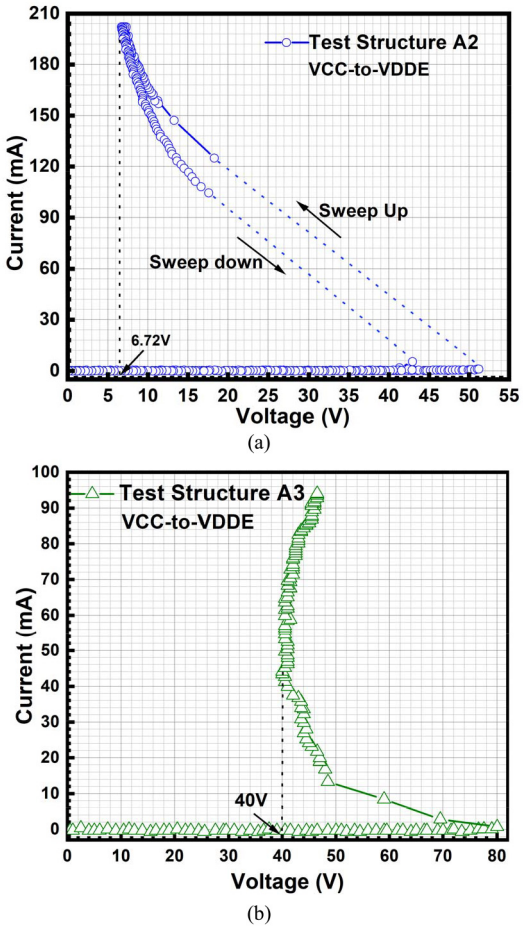

FIGURE 11. The measured DC I-V characteristics of the HV-to-LV latch-up paths from VCC to VDDE in (a) the test structures A2, and (b) the test structures A3.

shown in Figs. 10 (a) and 10(b), respectively. The collector supply of curve tracer is applied to the VCC pin of HV PNP ESD, and the ground is applied to the VDDE node. The measured DC I-V results of the HV-to-LV latch-up paths among the structures A2 and A3 are shown in Figs. 11 (a) and 11(b), respectively. From the measured results in Fig. 11(a), the holding voltage (Vh) of the test structure A2 is ~ 6.72 V, which is lower than 31 V (36 V - 5 V) of the voltage difference between VCC and VDDE. Based on the latch-up criterion, there will be a latch-up risk as long as the Vh of the test structure is below the voltage difference between VCC and VDDE. As shown in Fig. 11(b), the Vh of HV-to-LV latch-up path in the test structure A3 is 40 V, which is greater than the voltage difference between VCC (36V) and VDDE (5V). With the Schottky junction embedded into the isolation ring of NBL/HVNW in the test structure A3, the holding voltage of HV-to-LV latch-up path has been increased from 6.72 V to 40 V. With a Vh greater than the voltage difference between VCC and VDDE, the HV-to-LV latch-up occurrence in the test structure A3 can be fully avoided by the proposed Schottky-embedded isolation ring.

B. LATCH-UP CURRENT-TRIGGER TEST

Although the latch-up issue among these test structures can be evaluated from the measured dc I-V curves, the JEDEC standard (JESD78E) latch-up current-trigger test is referred to further validate their latch-up immunity at room temperature (25 °C) [18].

Fig. 12 shows the measurement setup of the JEDEC latch-up I test applied to the test structures. A positive trigger current with a typical pulse width of 10 ms is directly applied into the p-substrate via the additional P+_sub trigger pin that was especially drawn in the test structures. The cross-domain HV-to-LV latch-up path between VCC pin and VDDE, and the latch-up path in the LV internal circuits, will be monitored by an oscilloscope to judge the latch-up occurrence. Furthermore, among Fig. 12(a) ~ Fig. 12(c), the power sources of VCC (36V), VDDE (5V), and VDDI (3.3V) are in series with series resistances of 5 Ω, 10 Ω, and 50 Ω, respectively, to avoid the test structures being burned

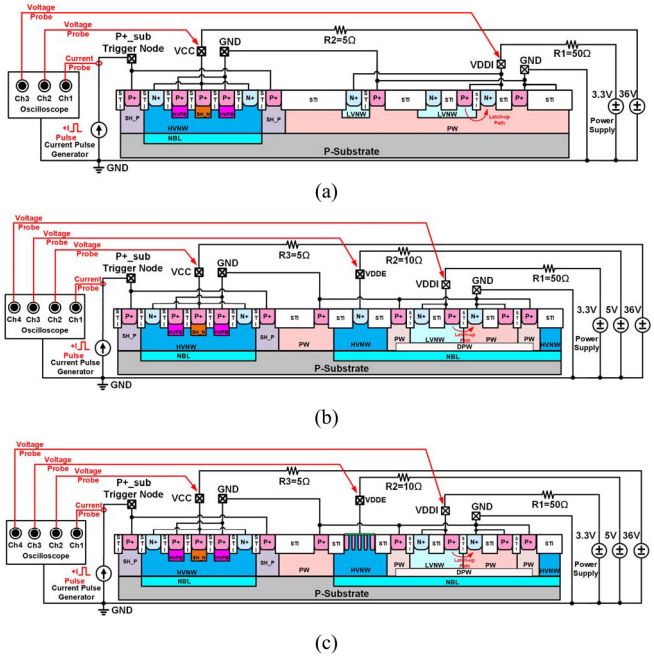

FIGURE 12. **Measurement setup of the latch-up I test applied to (a) the test structure A1, (b) the test structure A2, and (c) the test structure A3, with HV PNP ESD device and the LV internal circuit, where the positive trigger current is applied to the P+-sub trigger node.**

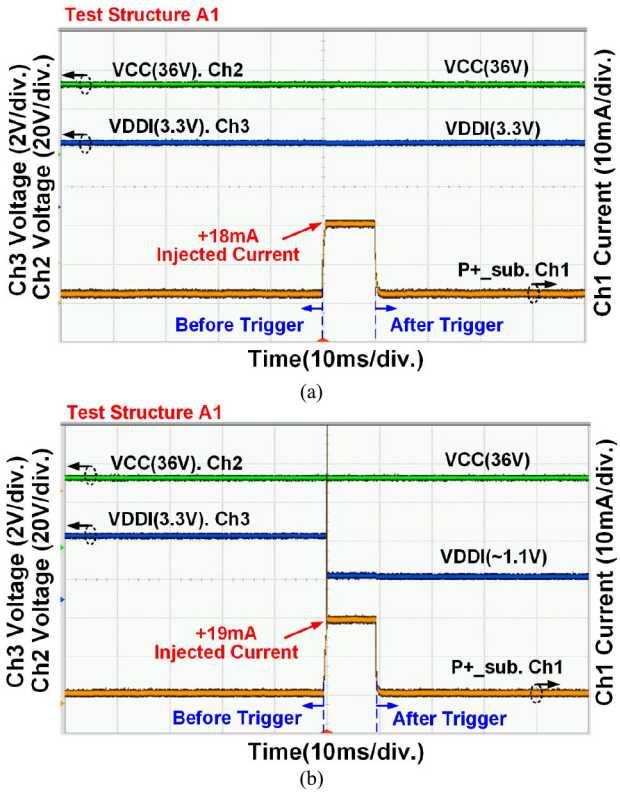

FIGURE 13. **Measured time-domain voltage and current waveforms on the test structure A1 with VCC at 36 V and VDDI of 3.3V under the positive latch-up I test of (a)18 mA, and (b) 19 mA.**

out if latch-up path was triggered on during the latch-up I test.

Fig. 12 (a) shows that a positive current pulse is applied to the P+ trigger node to inject the trigger current into the p-substrate. The corresponding voltage waveforms on the test structure A1 under the positive latch-up I test of 18 mA and 19 mA, are shown in Figs. 13(a) and 13(b), respectively. In Fig. 13(a), the voltage waveforms of VCC and VDDI are still kept the same before and after the trigger current of 18 mA was applied. This implies that no latch-up occurrence in the test structure A1 under such a latch-up I test of 18 mA. However, the parasitic latch-up path of LV internal circuit in the test structure A1 was triggered on by the trigger current of 19 mA, as the voltage at VDDI is clamped down to ∼1.1 V in Fig. 13(b). The clamped voltage of ∼1.1 V on VDDI is corresponding to the holding voltage of the p-n-p-n path in the internal circuits as measured in Fig. 9. After that, a huge leakage current is detected from VDDI to GND.

Figs. 12 (b) and 12(c) show the test structures A2 and A3 with a positive current pulse applied to the P+_sub trigger node. The corresponding time-domain voltage and current waveforms on the test structure A2 are shown in Figs. 14(a) and 14(b), after the injection of 45-mA and 50-mA current pulses, respectively. In Fig. 14(a), the voltage waveforms of VCC, VDDE, and VDDI are still kept the same before and after the trigger current of 45 mA was applied. This implies that no latch-up occurrence in the test structure A2 under such a latch-up I test of 45 mA. As comparing to the test results in Fig. 13(b), the latch-up immunity of the internal circuits is really improved by the isolation ring of NBL with HVNW.

In Fig. 14(b), after the latch-up I test of 50 mA, the voltage waveform of VCC was dropped down and kept at ∼ 6.8 V, as well as the voltage waveform of VDDE was also changed strangely. But, the voltage waveform on VDDI in Fig. 14(b) is still kept the same before and after the latch-up I test of 50 mA. From those observed voltage waveforms, the latch-up path of LV internal circuits in the test structure was not triggered on, but the HV-to-LV latch-up path between VCC pin and VDDE was triggered on by the trigger current of 50 mA.

On the other hand, with the measurement setup shown in Fig. 12 (c), which is the same as that in Fig. 12(b), the measured time-domain waveforms on the test structure A3 are shown in Fig. 15 with a latch-up I test of even up to 150 mA. As shown in Fig. 15, the voltage waveforms on VCC, VDDE, and VDDI in the test structure A3 is stably kept at 36 V, 5 V, and 3.3 V, respectively, after the latch-up I-test of 150 mA. This implies that neither latch-up occurrence in HV-to-LV latch-up path, nor latch-up occurrence in LV internal circuits, happened in the test structure A3. The latch-up immunity of cross-domain HV-to-LV latch-up path and the latch-up path in LV internal circuits can be significantly improved by the proposed Schottky-embedded isolation ring as that drawn in Fig. 7(c).

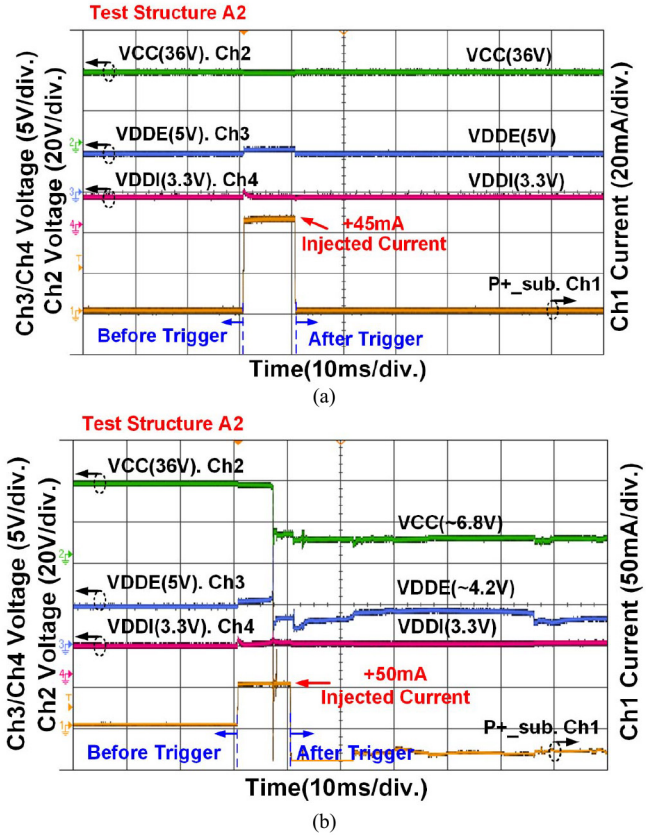

FIGURE 14. Measured time-domain voltage and current waveforms on the test structure A2 with VCC at 36 V, VDDE at 5V, and VDDI of 3.3V under the positive latch-up I test of (a) 45 mA, and (b) 50 mA.

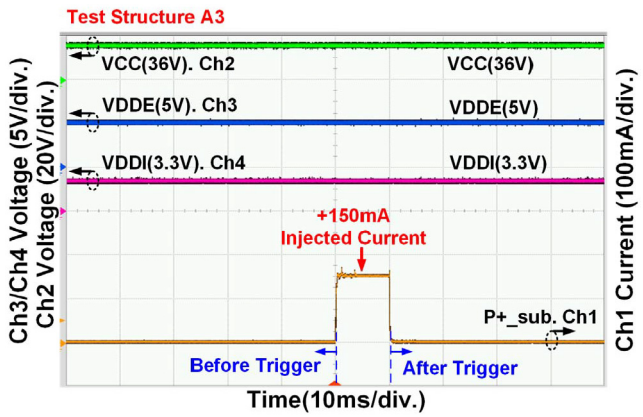

FIGURE 15. Measured time-domain voltage and current waveforms on the test structure A3 with VCC at 36 V, VDDE at 5 V, and VDDI of 3.3V under the positive latch-up I test of 150 mA.

From the experimental results, the Schottky-embedded junction (connecting the isolation ring of NBL with HVNW to VDDE) can significantly improve latch-up immunity of the test structure A3 by increasing the holding voltage of the parasitic latch-up path, but without enlarging the layout spacing between the HV PNP ESD device and the LV internal circuits.

V. CONCLUSION

The Schottky-embedded isolation ring for latch-up prevention between HV and LV circuits has been fabricated and investigated in a 0.18μm BCD process. By using the Schottky junction to connect the isolation ring of NBL with HVNW, the holding voltage of the parasitic p-n-p-n path can be increased greater than the voltage difference between the power supplies of HV circuits and LV internal circuits. Therefore, the cross-domain HV-to-LV latch-up path and the latch-up path in LV internal circuits can be significantly improved by the proposed Schottky-embedded isolation ring. The Schottky junction can be directly embedded onto the HVNW/BNL isolation ring without increasing the layout spacing between HV and LV blocks. The realization of Schottky junction is fully process-compatible in the given 0.18-μm HV BCD process by the foundry. The proposed Schottky-embedded NBL/HVNW isolation ring is an excellent and useful solution for latch-up prevention in the mixed-voltage CMOS ICs with the HV and LV circuit blocks integrated together in a compacted chip layout.

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