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Hf-Based and Zr-Based Charge Trapping Layer Engineering for E-Mode GaN MIS-HEMT Using Ferroelectric Charge Trap Gate Stack

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ABSTRACT E-mode hybrid ferroelectric charge storage gate (FEG) GaN HEMTs have shown promising performances for future power GaN device applications. The FEG-HEMT demonstrates a combination of ferroelectric polarization and charge trapping process in the ferro-charge-storage gate stack, leading to a positive threshold voltage shift for E-mode operations. In this work, FEG-HEMTs with various Hf-based and Zr-based charge trapping layers are systematically studied. FEG-HEMT which employed nitrogen incorporated HfO_2 (HfON) as the charge trapping layer shows an E-mode operation with the highest V_{th} (+2.3 V) after initialization. Moreover, the gate leakage of the HfON sample was further reduced due to the nitrogen incorporation, leading to a more complete charging process during initialization. The V_{th} instability is also addressed and investigated. The FEG-HEMT with HfON as the charge trapping layer showed a negligible V_{th} hysteresis (−43mV) and the highest V_{th} stability in both the PBTI (positive bias threshold voltage instability) and NBTI (negative bias threshold voltage instability) test measurements.

INDEX TERMS AlGaN/GaN, metal-insulator-semiconductor (MIS)-HEMT, enhancement-mode, charge trap gate stack, threshold voltage stability.

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) have emerged as important candidates for the next-generation power switching device applications. [1], [2]. Due to lower standby power dissipation, single-voltage operation, and fail-safe consideration, enhancement-mode (E-mode) is essential and GaN E-mode HEMT devices will play a crucial role in future electrical vehicle applications. Lately, a series of novel hybrid ferroelectric (HZO) charge trap gate stack schemes were presented to achieve E-mode operations [3], [4], [5]. A flash memory-like E-mode hybrid ferroelectric charge storage gate (FEG) GaN HEMT was introduced. Fig. 1 shows the schematic FEG-HEMT structure and the ferro-charge-storage gate stack structure. Due to the combination of the charge trapping layer (CTL) and the ferroelectric laminated layer, the threshold voltage would shift positively to a safety margin (+2.5 V) after a positive gate bias initialization and thus achieving an E-mode operation. The initialization process would result in a strong polarization in the ferro-stack and 2DEG electrons tunneling into the charge trapping layer and captured [4], [5]. Furthermore, since the polarization of the AlGaN/GaN heterostructure is not affected by the initialization charging process, the device shows both a high threshold voltage and a high current density at the same time. In the previous works, however, there still lacks an intensive study on the charge trapping abilities of various charge trapping layers and how they affect the V_{th} stability.

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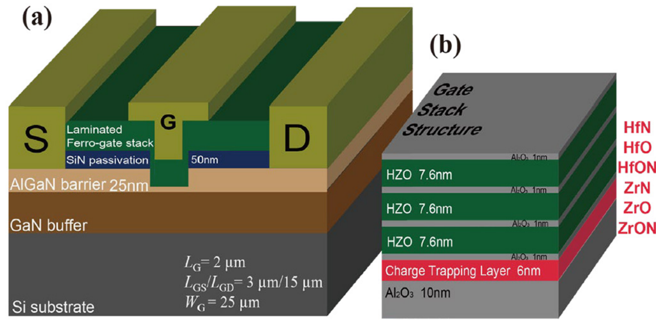

FIGURE 1. The schematic structure of the (a) E-mode hybrid ferroelectric charge storage gate (FEG) GaN HEMT (with device dimensions shown at the corner of the schematic structure) and (b) the schematic structure of the laminated ferroelectric charge storage gate stack.

V_{th} stability is a crucial issue for E-mode GaN operations, and thus very important for GaN FEG-HEMTs. As for FEG-HEMTs, the charge trapping and detrapping of the charge trapping layer strongly affects the V_{th} behaviors and cause V_{th} instability, which needs to be fully addressed. It is also important to point out that gate leakage induced incomplete charging process during the initialization process could also cause V_{th} instability.

Over the years, Hf-based and Zr-based high-k dielectrics have been adopted and investigated to replace conventional Si_3N_4 as CTLs, mainly due to their better scalability, large numbers of trapping sites, larger conduction band offset, and relatively higher dielectric constant. However, reports have shown that there exist O vacancy (V_O) levels in HfO_2 which plays a crucial role in the leakage current [6]. Moreover, trap-assisted tunneling through these high-k dielectrics could result in an increase in gate leakage current [7]. On the other hand, nitrogen incorporation in high-k dielectrics has been intensively researched. Nitrogen incorporation in high-k films showed an enhanced dielectric constant [8], [9], increase in crystalline temperature [10], and suppressed gate leakage [11]–[14]. All of which show promising properties to further increase and stabilize the threshold voltage of the E-mode FEG-HEMT.

In this letter, FEG-HEMTs with Hf-based and Zr-based oxides, nitrides, and oxynitrides as the charge trapping layer are systematically investigated by DC and PBTI tests to show the charge trapping properties. Benefiting from the nitrogen incorporation, the oxynitride samples showed larger V_{th} shifts after initialization due to the larger conduction band offset. Furthermore, suppressed gate leakage currents were also observed, resulting in a more complete charging process during the initialization. The V_{th} stability of the FEG-HEMTs is thus studied through the up and down DC sweep, a high gate bias PBTI (positive bias threshold voltage instability) stress test, and an NBTI (negative bias threshold voltage instability) stress test to further investigate the incomplete charging phenomenon in the charge trapping layer.

II. DEVICE FABRICATION

The AlGaN/GaN epitaxial layers were grown on silicon substrate by MOCVD. The AlGaN/GaN heterostructure epitaxial structure consisted of a 1-nm GaN cap layer, a 25-nm $Al_{0.23}Ga_{0.77}N$ barrier layer, a 4-μm undoped GaN layer, and a 100 nm AlN nucleation layer. The device fabrication starts with ohmic contact formation using an alloyed Ti/Al/Ni/Au metal stack. In-situ nitrogen plasma treatment was employed prior to the deposition of a 50-nm SiNx passivation layer using PECVD [15]. After passivation, the gate was fabricated. Nitride etch and gate recess were performed by a low-power ICP system and the remaining barrier thickness after etching was about 5 nm. The samples were then loaded into the ALD machine promptly. The gate stack growth by ALD consisted of a ferroelectric laminated structure (28 nm Al_2O_3-$HfZrO_4$-Al_2O_3) / charge trapping layer (6 nm) / tunneling oxide layer (10 nm Al_2O_3) (Fig. 1(b)). The adopted gate stack is identical to that of [4] and only the charge trapping layer has been modified. Six samples were fabricated with different charge trapping layers for comparison, namely (a) HfN (b) HfO_2 (c) HfON (d) ZrN (e) ZrO_2 (f) ZrON. The oxides (b, e) were grown by thermal ALD using H_2O as the oxidant and on the other hand, the nitrides (a, c) were grown by plasma ALD with N_2 plasma as the reactant. Both oxides and nitrides were deposited for 60 cycles. Additionally, the oxynitrides (c, f) were deposited with a cycle ratio of thermally grown oxide: plasma grown nitride = 1 : 1, for a total of 30 cycles (thermally grown oxide deposition immediately followed by a plasma grown nitride deposition). The six samples then underwent post-deposition annealing in N_2 ambient at 400 °C. After the gate stack deposition, ion implantation was used for mesa isolation. For the gate metal deposition process, a 4μm gate region was defined to form the T-gate structure. Ni/Au (50nm/300nm) was then deposited by electron beam evaporation as the gate metal.

III. RESULTS AND DISCUSSION

A. THRESHOLD VOLTAGE SHIFT CHARACTERISTICS AND BAND ALIGNMENT

Six samples were measured for the transfer characteristics before and after the initialization process to show the charge trapping abilities of different charge trapping layers (CTL) (Fig. 2). The V_{th} shift shown in Fig. 2 is a combination of data of two I_D-V_G characteristics, which is a V_G sweep from −8 to 0 and a V_G sweep from 0 to +8. The reason there exists a negative to zero V_{GS} DC transfer characteristic is to show the V_{th} value before the initialization, demonstrating the V_{th} shift before and after the initialization. Furthermore, the negative V_{GS} doesn't affect the initialization process. After the initialization process, devices showed V_{th} values of −0.49, 1.53, 2.3, −0.99, 0.62, and 1.12 V for the FEG-HEMT device with HfN, HfO_2, HfON, ZrN, ZrO_2, and ZrON as the CTL, respectively (The V_{th} was determined at the drain current of 1 μA/mm). Meanwhile, the devices showed positive V_{th} shift values of +3.83, +6.53, +7.56 V, +4.01, +5.56, and +5.84 for the FEG-HEMT device with

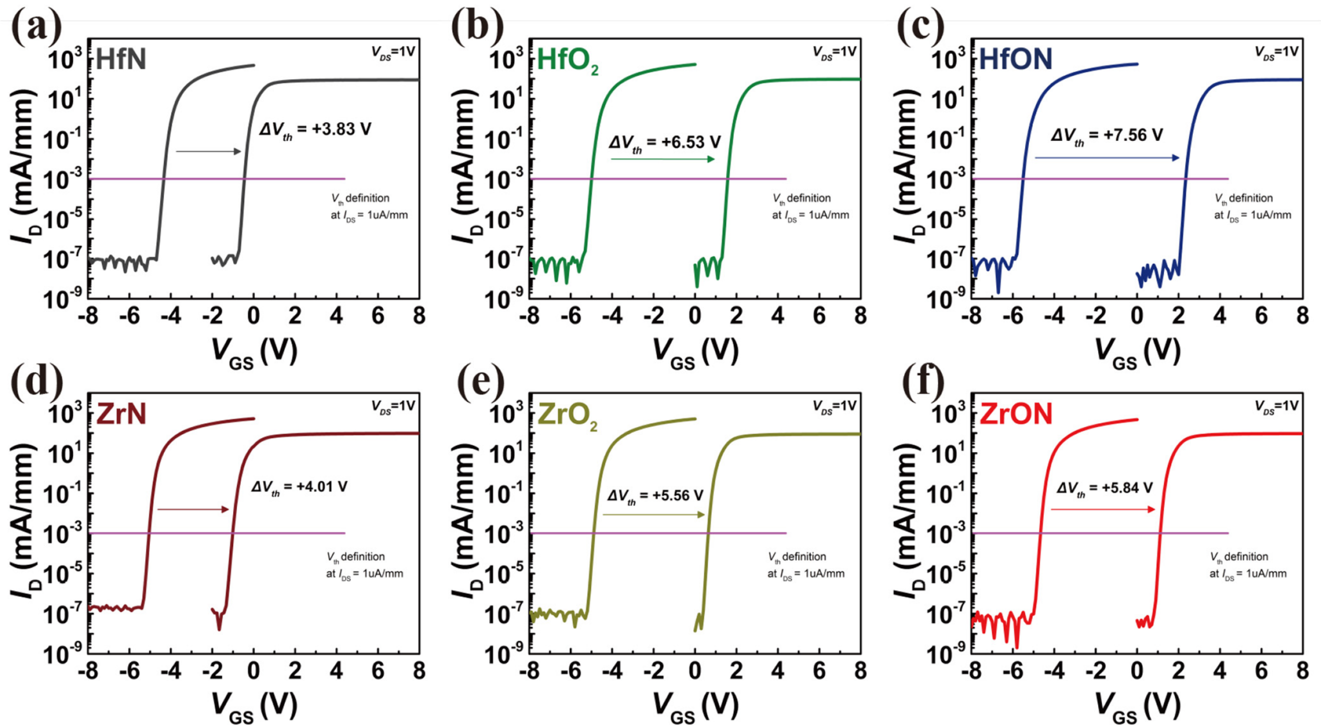

FIGURE 2. I_D-V_G **characteristics showing** V_{th} **shifts of FEG-HEMTs with (a) HfN (+3.83 V), (b)** HfO_2 **(+6.53 V), (c) HfON (+7.56 V), (d) ZrN (+4.01 V), (e)** ZrO_2 **(+5.56 V), and (f) ZrON (+5.84 V) as the charge trapping layer before and after the initialization (**V_{GS} **= 16 V,** V_{DS} **= 0 V for 1ms).**

HfN, HfO_2, HfON, ZrN, ZrO_2, and ZrON before and after the initialization ($V_{GS} = 16$ V, $V_{DS} = 0$ V for 1ms), respectively. Nitride CTL samples had the lowest V_{th} shifts and even resulted in D-mode operations after initialization. The possible reason is that transition metal nitrides are metallic and they are usually used as electrodes and not for charge storage [16]. Samples with oxynitride CTL such as ZrON and HfON had higher V_{th} shifts than oxide dielectrics (HfO_2, ZrO_2), nitrogen incorporation increases the dielectric constant of ZrO_2 [8] and HfO_2 [9] and further redistribute the electric field in the ferroelectric gate stack. When the same electric field is applied to the gate dielectric for the initialization process, the electric field across the Al_2O_3 tunneling layer is increased. This results in more electrons tunneling into the CTL and leads to a higher V_{th} shift [17].

In addition, the important characteristic of the charge trapping layer is its capability to confine the electrons, which would directly lead to higher threshold voltages after initialization. Figure 3(a) shows the band alignment of the Hf-based and Zr-based oxide and oxynitride charge trapping layers [8], [18], [19], [20], [21]. The conduction band offset of ZrON and HfON with respect to Al_2O_3 is higher than that of ZrO_2 and HfO_2. The larger ΔE_Cs of oxynitrides from the Al_2O_3 layer directly contributes the enhancement of the direct tunneling during initialization due to the reduced barrier heights induced by nitrogen incorporation (Figure 3(b)). Furthermore, out of the 6 samples, FEG-HEMT with HfON as the CTL showed the largest V_{th} shift, indicating a sign of more charge trapping in the HfON CTL than in other samples. The largest ΔE_C (HfON) with deeper trapping energy would result in the largest V_{th} shift and the best electron confinement, which is a key factor for improved GaN E-mode performance and better V_{th} stability [20]. Moreover, the increase in crystalline temperature due to the nitrogen incorporation in HfO_2 could also help with the charge trapping process [10], [17]. The charge trapping behaviors of dielectric layers are strongly dependent on the deep trapping processes. It is commonly known that amorphous materials contain higher deep trap density than polycrystalline materials and possess higher disorder and band-tail localization, thus enhancing the charge trapping capability [22]. With the help of nitrogen incorporation, the partial crystallization in HfO_2 could be mitigated during the 400°C post-deposition annealing process [23], [24]. In addition, Hf-based dielectrics had higher V_{th} shifts than Zr-based dielectrics either oxide or oxynitride, suggesting that Hf-based dielectrics have higher trap density and relatively higher crystalline temperature.

B. GATE BREAKDOWN CHARACTERISTICS

Figure 4 shows the I_G–V_G characteristics of all the devices. Devices showed a gate breakdown voltage of 21.4, 23.4, 22.9, 22.2, 22.8, and 24.1 V for the device with HfN, HfO_2, HfON, ZrN, ZrO_2, and ZrON, respectively. The gate breakdown voltage was determined as the drain current reaches 1 μA/mm. It has been reported that trap-assisted tunneling through these high-k dielectrics is the reason for gate leakage to occur [7]. As for the case of HfO_2, O vacancy (V_O) levels

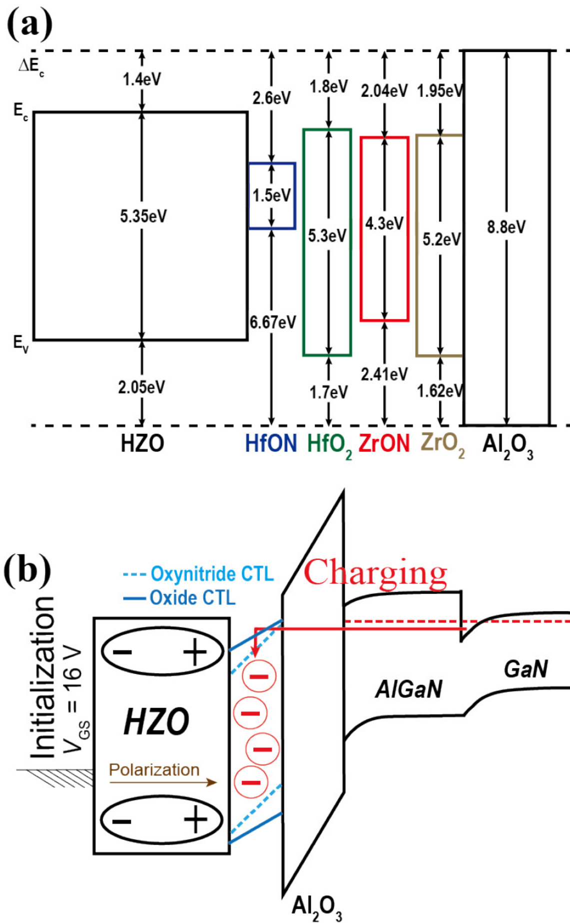

FIGURE 3. (a) The band alignment of the Hf-based and Zr-based oxide and oxynitride charge trapping layers with respect to Al_2O_3 and (b) Schematic band diagram of polarizing the ferroelectric gate stack during initialization, illustrating a charge storage process of a FEG-HEMT with oxide or oxynitride CTL [4].

(which are located at ~1.2eV below the bottom of the conduction band) play a crucial role in electron leakage current. From Fig. 4 we could see that with the help of the nitrogen incorporation effect, the gate leakage current of HfON was much lower than that of HfO_2. The reason why the HfON sample showed reduced gate leakage current is because of the elimination of V_O related gap states. Nitrogen incorporation could effectively deactivate V_O related gap states by changing the charge states of V_O from neutral ($V_O{}^0$) to positive ($V_O{}^{2+}$) [11]. Meanwhile, the same trend was observed in Zr-based dielectrics but the effect of nitrogen incorporation in ZrO_2 was not obvious.

Furthermore, gate leakage at $V_G = 16$ V needs to be fully addressed. Due to the initialization process of the FEG-HEMT, gate leakage could cause an incomplete charging process and thus leading to V_{th} instabilities. FEG-HEMT with ZrON as CTL shows a larger gate leakage current of $1.1*10^{-5}$ mA/mm at $V_G = 16$ V compared to HfON as CTL shows a lower gate leakage current of $5.22*10^{-6}$ mA/mm (Figure 4).

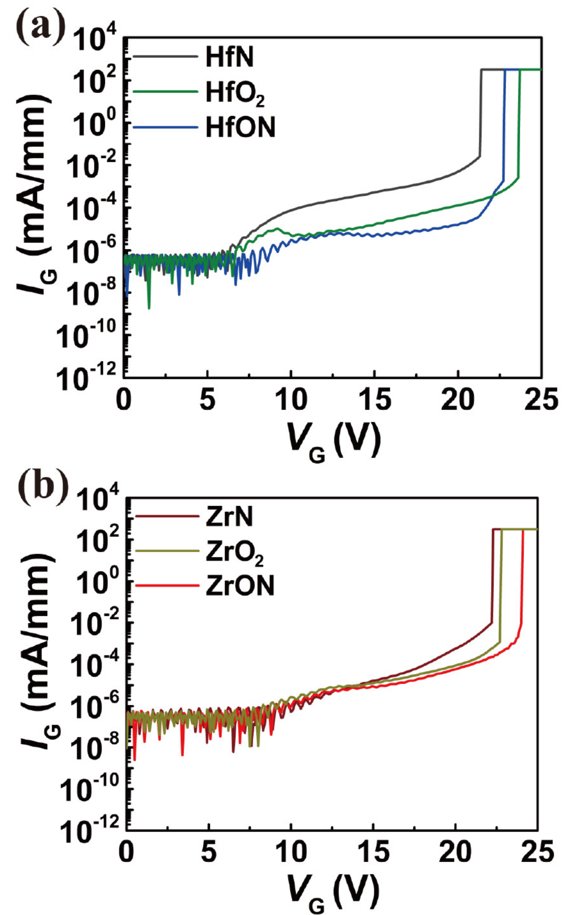

FIGURE 4. Gate leakage and gate breakdown I_G-V_G characteristics of FEG-HEMTs with Hf-based and Zr-based charge trapping layers.

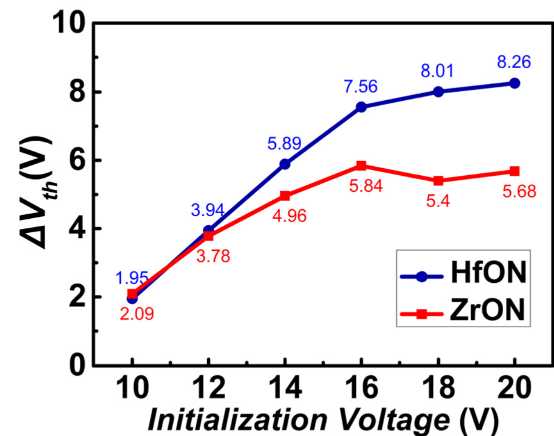

FIGURE 5. V_{th} shifts versus different initialization voltages from the range 10 to 20 V.

Figure 5 shows the V_{th} shifts of the HfON and the ZrON CTL sample under different initialization voltages. The V_{th} shifts showed a gradual increase when the gate was biased from 10-16 V. When samples underwent initialization larger than 16 V, the increase of V_{th} slowed. This may be due to the CTL already reached the maximum charge storage capacity.

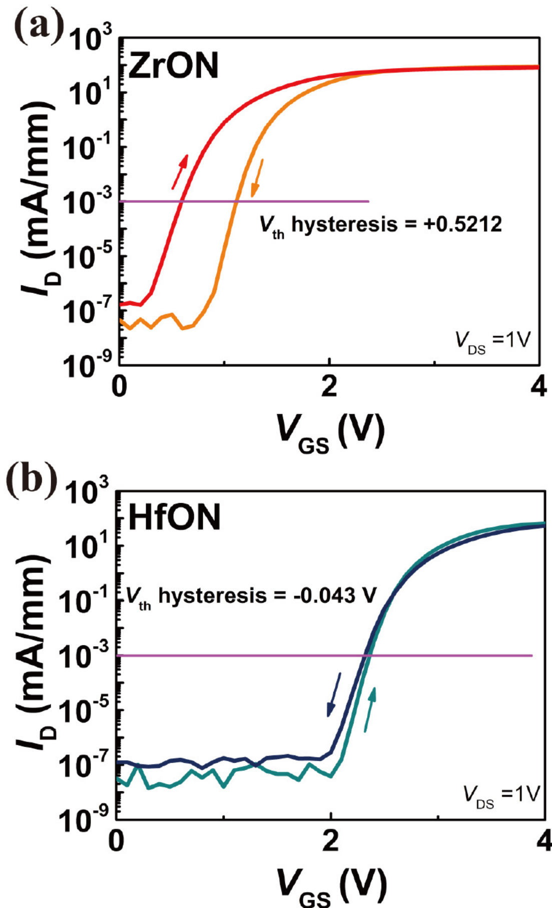

FIGURE 6. Up sweep and down DC sweep of FEG-HEMTs with (a) ZrON and (b) HfON as charge trapping layers.

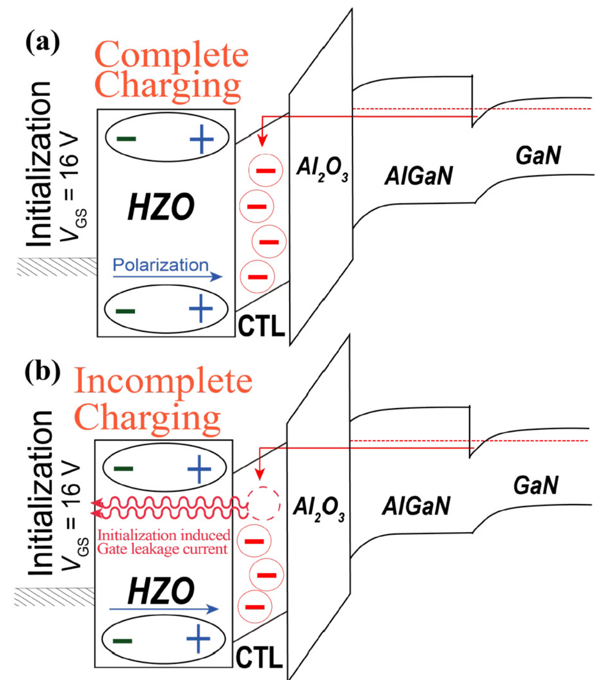

FIGURE 7. Schematic band diagram of (a) complete charging and (b) incomplete charging during the initialization process.

The HfON sample exhibits an overall larger V_{th} shift which verifies the aforementioned larger ΔE_C and relatively higher crystalline temperature. Furthermore, the reduced gate leakage current of the HfON sample at high gate biases also benefits the charging process at high initialization voltages.

Figure 6 shows the V_{th} hysteresis loops of the E-mode FEG-HEMT devices with HfON and ZrON as the charge trapping layer. The V_{th} hysteresis measurement was performed using a continuous double DC sweep, with the gate voltage traced from 0 V to 16 V and then 16 V back to 0 V. The V_{th} of the up-sweep and down-sweep curves were both set at $I_D = 1$ μA/mm. To illustrate the V_{th} hysteresis region better, Figure 6 only shows the V_G in the range from 0 V to 4 V. The FEG-HEMT with HfON as the CTL showed a much lower V_{th} hysteresis ($\Delta V_{th} = -43$ mV) than the one with ZrON ($\Delta V_{th} = +521$ mV). This result was due to the reduced gate leakage during the initialization as mentioned above. A larger gate leakage current during initialization means that a portion of the electrons wasn't fully trapped in the CTL and leaked at high gate voltage (Fig. 7). Fig. 7(b) illustrates a schematic band diagram of the origin of the incomplete charging, which causes threshold voltage instability. During the down sweep process, the charge trapping was further completed due to the lower gate voltage of the down sweep procedure. This is why in addition to the larger V_{th} hysteresis of the ZrON CTL sample, the V_{th} hysteresis also showed a positive value. On the other hand, the HfON CTL sample showed a significant reduction of V_{th} hysteresis, and the V_{th} hysteresis was negative. The result indicates a more fully charged initialization process. The negative V_{th} hysteresis of the HfON CTL sample could be the result of electron detrapping in the CTL which occurred due to the lower gate applied voltage during the down sweep cycle. This negative V_{th} hysteresis exhibits charge retention characteristics of the FEG-HEMT. Nonetheless, the negative V_{th} shift of the HfON CTL sample is small and negligible, showing excellent charge trapping abilities.

C. PBTI AND NBTI STRESS TESTS

To further investigate the V_{th} stability, both PBTI (positive bias threshold voltage instability) and NBTI (negative bias threshold voltage instability) tests were conducted to demonstrate the charging characteristics under different gate bias stresses. Figure 8 shows the PBTI characteristics of all the devices after the initialization. The devices showed positive V_{th} shifts of 2.09, 3.17, 1.72, 2.25, 3.27, and 2.51 V at 1000 seconds for the devices with HfN, HfO_2, HfON, ZrN, ZrO_2, and ZrON as CTL, respectively. The PBTI measurement demonstrates further signs of incomplete charging in the HfO_2 and ZrO_2 CTL samples, showing the largest V_{th} shift over time. With the help of nitride incorporation, the oxynitride CTLs were able to charge more completely

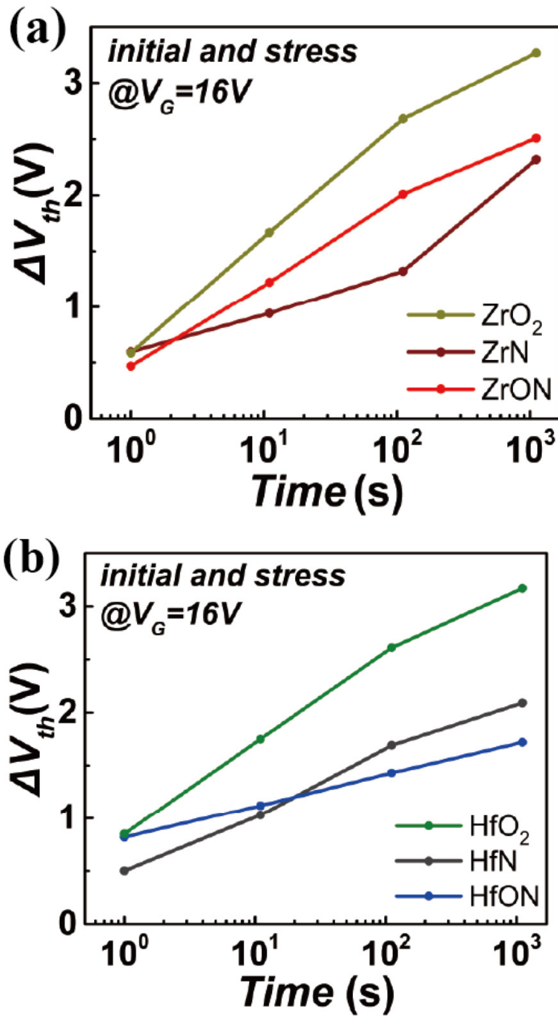

FIGURE 8. PBTI results of FEG-HEMTs after initialization with (a) Zr-based and (b) Hf-based dielectrics as the charge trapping layers.

during the initialization process. This result is mainly due to the reduction of the electron leakage mentioned before. As for the NBTI test (Fig. 9), the devices were stressed at $V_G = -5$V for 100 seconds. Due to unintentional ringing or intentionally applying off-state bias to prevent false turn on, an NBTI test was also conducted to show the V_{th} stability of the devices. The reason for choosing a stress bias of $V_G = -5$ V is because the devices had a V_{th} of approximately -5 V before the initialization. Negative threshold voltage shift percentages ($\Delta V_{th,NBTI}/\Delta V_{th,initialization}$) of 48.37, 42.68, 32, 64.7, 50.35, and 49.23 % at 100 seconds were observed for the devices with HfN, HfO_2, HfON, ZrN, ZrO_2, and ZrON as CTL, respectively. The HfON CTL sample, which possesses better charge confinement, shows an overall reduction of negative threshold voltage shift. From the results shown above, the FEG-HEMT that adopts HfON as CTL shows the highest V_{th} stability under various DC measurements such as DC up and down sweeps as well as NBTI and PBTI measurements.

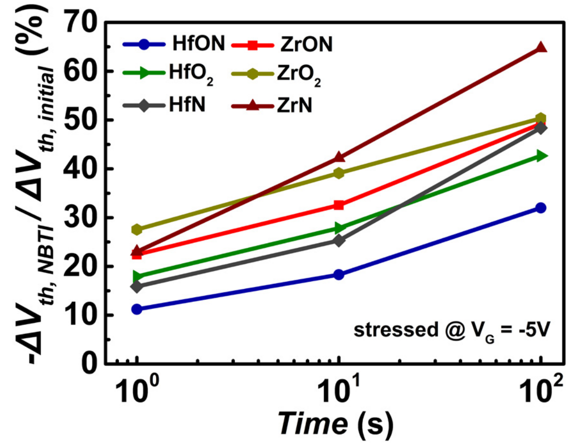

FIGURE 9. Negative threshold voltage shift percentages of FEG-HEMTs ($\Delta V_{th,NBTI}/\Delta V_{th,initialization}$) in a 100 second NBTI test.

IV. CONCLUSION

In this work, the effects of nitrogen incorporation in Hf-based and Zr-based charge trapping oxide layers are investigated through the behaviors of the threshold voltage shifts of the FEG-HEMTs. FEG-HEMT which employed nitrogen incorporated HfO_2 (HfON) as the charge trapping layer showed the largest V_{th} shift (+7.56 V) after initialization, resulting in an E-mode operation with higher V_{th}. From the band alignment simulation, the HfON material showed the largest conduction band offset and the smallest band gap, which was most suitable for electron confinement. Owing to the nitrogen incorporation, the gate leakage (at $V_G = 16$ V) of the HfON sample was further reduced by an order of magnitude when compared to the sample with ZrON as the CTL layer, leading to a more complete charging process during initialization. Moreover, V_{th} stability is investigated through a double DC sweep, a 1000 second PBTI test, and a 100 second NBTI test. The FEG-HEMT with HfON as the charge trapping layer showed a negligible V_{th} hysteresis (-43mV) and the highest V_{th} stability in both the PBTI and NBTI measurements.

REFERENCES

[1] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.
[2] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002, doi: 10.1109/jproc.2002.1021567.
[3] C.-H. Wu *et al.*, "High V_{th} enhancement mode GaN power devices with high $I_{D,max}$ using hybrid ferroelectric charge trap gate stack," in *VLSI Symp. Tech. Dig.*, Jun. 2017, pp. T60–T61, doi: 10.23919/vlsit.2017.7998201.
[4] C.-H. Wu *et al.*, "High-performance normally-OFF GaN MIS-HEMTs using hybrid ferroelectric charge trap gate stack (FEG-HEMT) for power device applications," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 991–994, Jul. 2018, doi: 10.1109/led.2018.2825645.
[5] Z. Feng *et al.*, "Normally-Off- β $-Ga_2O_3$ power MOSFET with ferroelectric charge storage gate stack structure," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 333–336, Mar. 2020, doi: 10.1109/LED.2020.2970066.

[6] H. Takeuchi, D. Ha, and T. King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry," *J. Vac. Sci. Technol. A*, vol. 22, no. 4, pp. 1337–1341, Jul. 2004, doi: 10.1116/1.1705593.

[7] K. Torii *et al.*, "Dielectric breakdown mechanism of HfSiON/SiO_2/gate dielectric," in *Dig. Tech. Paper Symp. VLSI Technol.*, Jun. 2004, pp. 112–113, doi: 10.1109/VLSIT.2004.1345423.

[8] J.-X. Chen, J.-P. Xu, L. Liu, and P.-T. Lai, "Performance improvements of metal–oxide–nitride–oxide–silicon nonvolatile memory with ZrO_2 charge-trapping layer by using nitrogen incorporation," *Appl. Phys. Exp.*, vol. 6, no. 8, Aug. 2013, Art. no. 84202, doi: 10.7567/apex.6.084202.

[9] H. Momida *et al.*, "Effects of nitrogen atom doping on dielectric constants of Hf-based gate oxides," *Appl. Phys. Exp.*, vol. 88, no. 11, Apr. 2006, Art. no. 112903, doi: 10.1063/1.2184991.

[10] K.-J. Choi, J.-H. Kim, S.-G. Yoon, and W.-C. Shin, "Structural and electrical properties of HfO_xN_y and HfO_2 gate dielectrics in TaN gated nMOSCAP and nMOSFET devices," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. Process. Meas. Phenom.*, vol. 22, pp. 1755–1758, Aug. 2004, doi: 10.1116/1.1771664.

[11] N. Umezawa *et al.*, "First-principles studies of the intrinsic effect of nitrogen atoms on reduction in gate leakage current through Hf-based high-k dielectrics," *Appl. Phys. Lett.*, vol. 86, no. 14, Mar. 2005, Art. no. 143507, doi: 10.1063/1.1899232.

[12] E. Kojima *et al.*, "Effect of incorporation of nitrogen atoms in Al_2O_3 gate dielectric of wide-bandgap-semiconductor MOSFET on gate leakage current and negative fixed charge," *Appl. Phys. Exp.*, vol. 11, no. 6, Jun. 2018, Art. no. 61501, doi: 10.7567/apex.11.061501.

[13] J.-J. Huang, Y.-J. Tsai, M.-C. Tsai, L.-T. Huang, M.-H. Lee, and M.-J. Chen, "Impact of nitrogen depth profiles on the electrical properties of crystalline high-*K* gate dielectrics," *Appl. Surf. Sci.*, vol. 324, pp. 662–668, Jan. 2015, doi: 10.1016/j.apsusc.2014.11.009.

[14] W.-J. Maeng, J.-W. Lee, J.-M. Myoung, and H. Kim, "Comparative studies of atomic layer deposition and plasma-enhanced atomic layer deposition Ta_2O_5 and the effects on electrical properties of in situ nitridation," *Jpn. J. Appl. Phys.*, vol. 46, pp. 3224–3228, May 2007, doi: 10.1143/jjap.46.3224.

[15] S.-C. Liu, B.-Y. Chen, Y.-C. Lin, T.-E. Hsieh, H.-C. Wang, and E. Y. Chang, "GaN MIS-HEMTs with nitrogen passivation for power device applications," *IEEE Electron Device Lett.*, vol. 35, no. 10, pp. 1001–1003, Oct. 2014, doi: 10.1109/led.2014.2345130.

[16] J. F. Kang *et al.*, "Scalability and reliability characteristics of CVD HfO_2 gate dielectrics with HfN electrodes for advanced CMOS applications," *J. Electrochem. Soc.*, vol. 154, pp. H927–H932, Nov. 2007, doi: 10.1149/1.2775163.

[17] M.-H. Cho *et al.*, "Dielectric characteristics of Al_2O_3–HfO_2 nanolaminates on Si (100)," *Appl. Phys. Lett.*, vol. 81, no. 6, pp. 1071–1073, Aug. 2002, doi: 10.1063/1.1499223.

[18] C. Lai *et al.*, "Very low voltage SiO2/HfON/HfAlO/TaN memory with fast speed and good retention," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2006, pp. 44–45, doi: 10.1109/VLSIT.2006.1705208.

[19] G. He, L. D. Zhang, M. Liu, J. P. Zhang, X. Wang, and C. M. Zhen, "Thickness-modulated optical dielectric constants and band alignments of HfO_x N_y gate dielectrics," *J. Appl. Phys.*, vol. 105, no. 1, Jan. 2009, Art. no. 14109, doi: 10.1063/1.3062792.

[20] H. J. Yang *et al.*, "Comparison of MONOS memory device integrity when using $Hf_{1-x-y}N_xO_y$ trapping layers with different N compositions," *IEEE Trans Electron Devices*, vol. 55, no. 6, pp. 1417–1423, Jun. 2008, doi: 10.1109/TED.2008.920973.

[21] Z. Feng *et al.*, "The band structure change of $Hf_{0.5}Zr_{0.5}O_2$/Ge system upon post deposition annealing," *Appl. Surf. Sci.*, vol. 488, pp. 778–782, Sep. 2019, doi: 10.1016/j.apsusc.2019.05.282.

[22] R. A. Street, "Disorder effects on deep trapping in amorphous semiconductors," *Philos. Mag. Lett. B*, vol. 49, no. 1, pp. L15–L20, Jan. 1984, doi: 10.1080/13642818408246494.

[23] W. Zhu *et al.*, "HfO_2 and HfAlO for CMOS: Thermal stability and current transport," in *IEDM Tech. Dig.*, vol. 74, pp. 1–4, Feb. 2001, doi: 10.1109/IEDM.2001.979541.

[24] G. Xu and Q. Xu, "Thermal stability of HfON, HfSiON and HfTaON gate dielectrics," in *Proc. 9th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, Oct. 2008, pp. 1284–1287, doi: 10.1109/ICSICT.2008.4734776.