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Cryogenic CMOS RF Device Modeling for Scalable Quantum Computer Design

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ABSTRACT This paper presents experimental RF characterizations and modeling on the nano-scale multi-finger gate MOSFETs of the HLMC 40 nm low-power CMOS technology. Both the resistive and capacitive components in the equivalent circuit model for the RF MOSFET devices are calibrated based on temperature-dependent S-parameter measurements (0.25 – 40 GHz) from 298 K to 6 K. By integrating the intrinsic device model and the extrinsic parasitic parameters, a generic cryogenic device RF model is developed to capture the cutoff frequency and high-frequency performance of NMOS and PMOS transistors with varied device configurations. The establishment of validated database as functions of device size, temperature, and frequency responses lays a solid foundation for practical large-scale cryo-CMOS RF circuit design and optimization.

INDEX TERMS Cryogenic electronics, RF MOSFET, S-parameter measurement, cutoff frequency.

I. INTRODUCTION

Quantum computers have demonstrated great advantages over classical binary computer in dealing with quantum algorithm-based problems [1]–[3]. In the state-of-the-art quantum processor architecture, the generation of qubits is achieved at deep cryogenic temperatures ($T < 1$ K) while the control and readout modules are placed adjacent to the quantum processor to reduce thermal noise and communication delay [4]. Accordingly, recent progress has been focused on the design of cryo-CMOS integrated circuits and transceivers to realize the qubit manipulation, conversion, and error correction [5]–[7]. In this context, although earlier work managed to explore the cryogenic DC transfer characteristics of MOSFETs and evaluate the variation of temperature-related parameters with statistical analysis [8], the lack of a reliable cryo-CMOS compact model, which can cover the operations of superconductor/silicon-based qubits in the radiofrequency (RF) band (typically 2 – 20 GHz), has restricted current cryogenic RF circuit designs only rely on insufficient experimental data of limited devices at a certain temperature point (4.2 K) [9]–[11]. Therefore, in order to implement large-scale integrated circuits suitable for full-fledged quantum computing applications, it is of great importance to characterize the RF performance of transistors with varied gate geometries and setup a generic cryo-CMOS RF compact model valid over the entire temperature and frequency ranges.

To address such challenges, previous work [12] studied several on-chip microwave passive components at 4.2 K. Furthermore, [13] and [14] attempted to develop the small-signal equivalent circuit model of the FD-SOI devices at cryogenic temperatures, yet the transconductance

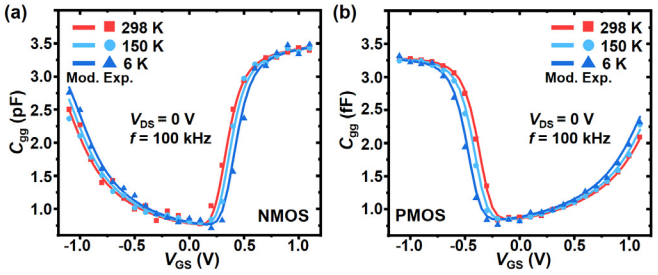

FIGURE 1. Experimental data (dots) and cryo-BSIM model fitting (solid lines) of C_{gg} versus V_{GS}. (a) NMOS and (b) PMOS with $W = 10$ μm, $L = 1$ μm, and $N_f = 27$.

and equivalent *RC* components were directly derived from the experimental values (i.e., which varied from device to device). Alternatively, a more general approach to build a cryo-CMOS RF compact model is by augmenting the intrinsic device compact model with external sub-circuit parasitic components [17]. In this paper, we investigate the temperature-dependent S-parameter of various NMOS/PMOS transistors with different gate sizes, and extend the modified cryogenic compact model [15] into the high-frequency region so as to include all device layout-associated *RC* parameters. Our proposed BSIM-based cryogenic CMOS RF compact model hence enables highly-efficient design and analysis of analog integrated circuit modules suitable for full-fledged quantum computing applications.

II. EXPERIMENT

The experiments discussed in this work were conducted on the standard RF test wafer of the HLMC 40-nm technology node by using a Lakeshore cryogenic probe station accompanied with the high-precision Keysight B1500A semiconductor device analyzer and Keysight 5227A Vector Network Analyzer (VNA). Following the standard CMOS modeling process flow, we firstly carried out low-frequency (100 kHz) *C-V* measurements on the specialized MOSCAP test structures to setup the initial process parameters in the commonly-used BSIM-4 model (i.e., the built-in model for most SPICE simulators), as illustrated in Fig. 1. It is found that the extracted oxide thickness (TOXE, TOXP, DTOX) and dielectric constant (EPSROX) remain unchanged from 298 K to 6 K, whereas the gradual horizontal shift of the total gate capacitance C_{gg} - V_{GS} curves indicate the increase of the threshold voltage (V_{th}) at lower temperatures. Afterwards, temperature-dependent DC and S-parameter measurements were performed on 36 multi-finger gate NMOS and PMOS transistors (i.e., all devices are of the ground-signal-ground (GSG) pad structures) across the device size chart (Fig. 2a), and the original recorded data are summarized in Figs. 2b-e which serve as the platform for the device modeling study. From one set of the data exemplified in Figs. 3a, it is seen that the static I_{DS}-V_{DS} performances of both the NMOS and PMOS ($W = 1$ μm, $L = 0.04$ μm, $N_f = 32$) transistors improve substantially with reduced sub-threshold swings (SS), enhanced trans-conductances (g_m), and negligible leakage currents

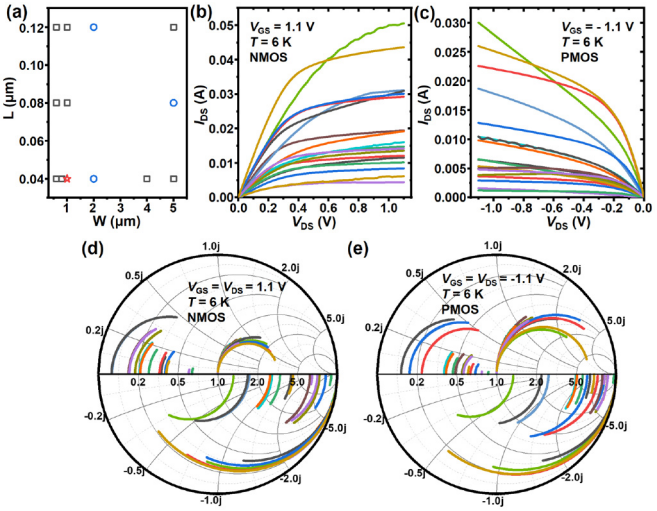

FIGURE 2. (a) 36 Multi-finger gate transistors measured in this work covering the device size chart of the HLMC 40LP technology. (b)-(c) Cryogenic DC characterizations of the 18 NMOS and PMOS transistors. (d)-(e) Experimental Smith chart data of the same 18 NMOS and PMOS devices at $T = 6$ K and frequency range of [0.25, 40 GHz].

(I_{leak}) when the base temperature decreases from 298 K to 6 K [15].

In the meantime, after excluding parasitic components from the instrument/cables and the on-chip interconnections /GSG pads by applying the standard Short-Open-Load-Through (SOLT) method (by using the standard GGB CS-5 calibration substrate) and Open-Short de-embedding technique at each temperature point [17], the well-calibrated cryogenic S-parameter diagrams of the NMOS and PMOS under the fixed bias condition of ($|V_{GS}|$, $|V_{DS}|$ = (1.1 V, 1.1 V) are presented in Fig. 3b. In accordance with the temperature-dependent I_{DS}-V_{DS} curves, the magnitude of S_{21} (i.e., it correlates positively with the transconductance g_m), which represents the forward transmission properties of the transistor, has an incremented value at 6 K as compared to that at 298K. In contrast, the S_{22} curves exhibit a much less temperature sensitive trait, indicating a slight reduction of the output impedance as the temperature drops [16]. Likewise, the reflection coefficient S_{11} stays almost constant in the [6 K, 298 K] region, and such feature guarantees good input impedance matching regardless of temperature fluctuation for cryogenic RF circuit design. From the aforementioned DC/RF characterizations, we have created a reliable database for the following parameter extraction and cryogenic device modeling.

III. MODEL DESCRIPTION AND DISCUSSION

When MOSFETs operate in the low-frequency range, their static characteristics are mainly dictated by the intrinsic electrical parameters within the Source/Drain/Gate/Body terminals. On the other hand, as the working frequency enters the GHz domain, the peculiar device-related layout structures would bring about additional parasitic *RC* components which play an indispensable role in determining the input/output impedance matching, poles/zeros position, and

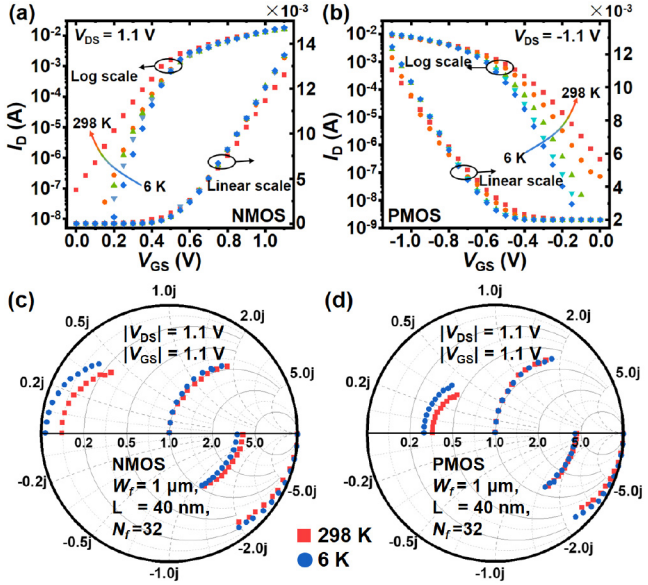

FIGURE 3. **Temperature-dependent (a) DC transfer characteristics and (b) RF S-parameters of two nano-scale NMOS and PMOS transistors with device size of $W = 1$ μm, $L = 0.04$ μm, and $N_f = 32$. For the DC measurement, V_{DS} is kept at 50 mV while the gate voltage $|V_{DS}|$ is swept consecutively from 0 V to 1.1 V with a step size of 1mV. For the high-frequency experiments, S_{21} and S_{12} curves are transferred from polar plots to Smith chart with appropriate scaling for convenient comparison. The applied frequency is tuned from 0.25 GHz to 40 GHz, and the supplied voltages are fixed at $V_{DS} = V_{GS} = 1.1$ V.**

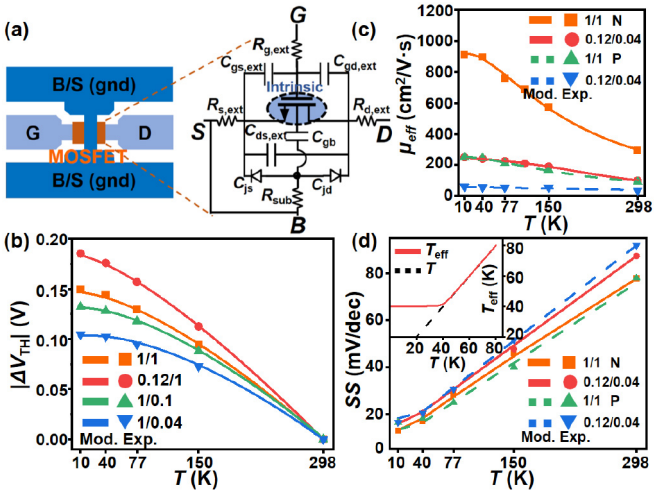

FIGURE 4. **(a) Equivalent RF circuit of nano-scale MOSFETs, which includes both the intrinsic device DC model and additional layout-dependent parasitic resistive/capacitive parameters important for the high-frequency operation. Cryogenic (b) threshold voltage V_{th} model, (c) mobility μ_{eff} model, and (d) subthreshold swing model. Inset: Effective temperature T_{eff} model.**

the RF figures-of-merit (FoM) of the designed circuit. In this regard, the equivalent circuit for the RF transistor used in this work consists of the intrinsic MOSFET model and the layout-dependent resistance/ capacitance (Fig. 4a), so that the quiescent operation point, RF cryogenic gate/substrate -dependent effects, and the temperature-sensitive variables are taken into account to elucidate the overall device performance with respect to temperature, frequency, and device structure.

A. CRYOGENIC INTRINSIC MOSFET DC MODELING

Considering that the DC characterizations of MOSFETs primarily depend on threshold voltage ($V_{\rm th}$), channel mobility ($\mu_{\rm eff}$), and sub-threshold swing, we have quantitatively investigated the gate geometry-dependent threshold voltage and scattering-induced channel mobility based on the physical model, and added such temperature-related correction terms in the BSIM-4 Verilog-A codes to establish the cryo-CMOS device compact model [15]. Following the same device physics principle, we briefly recapture the main modeling procedure for the design of the intrinsic device model in this section.

Firstly, because the carrier freeze-out effect de-activates the ionized dopant densities at cryogenic temperatures (i.e., for NMOS transistor, its p-type substrate carrier density is given by $N_A^-(T) = N_A \times f(E_A, T)$, where $f(E_A, T)$ is the Fermi–Dirac ionization probability), it would inevitably broaden the depletion width $W_{\rm D}$ (T) at the Source/Drain-Body junction regions, thereafter modifying the effective channel length and width. Consequently, such temperature-driven gate geometry effect on the threshold voltage can be formulated as

$$\Delta V_{\rm th1}(T) = +\frac{qN_{\rm A}W_{\rm D\,max}(T)}{C_{\rm ox}}\left(\frac{\xi W_{\rm D\,max}(T)}{W}\right)\left(1-\frac{T}{298}\right) \quad (1)$$

$$\Delta V_{\rm th2}(T) = -\frac{qN_{\rm A}W_{\rm D\,max}(T)}{C_{\rm ox}}\left(\frac{x_j}{L}\right)\left(\sqrt{1+\frac{2W_{\rm D\,max}(T)}{x_j}}-1\right) \times\left(1-\frac{T}{298}\right) \quad (2)$$

where $W_{D,m}(T) = \sqrt{4\varepsilon_{si}\varphi_{fp}/(qN_A^-(T))}$ is the maximum depletion width, ϵ_{Si} is the permittivity of Si, φ_{fp} is the surface potential, q is the electron charge, $\xi = \pi/10$ is a process parameter, and x_j is the Source/Drain depth. Since the Source and Body terminals are always grounded in the GSG structure (Fig. 4a), the substrate body bias effect is absent, and the overall threshold voltage expression is given by

$$V_{\rm th}(T) = V_{\rm th0}(T) + Z\cdot\Delta V_{{\rm th},W}(T) + K\cdot\Delta V_{{\rm th},L}(T) \quad (3)$$

where $V_{\rm th0}(T) = V_{\rm FB}(T) + 2\varphi_{fp}(T)$ reflects the temperature-induced band bending. By using the same fitting parameters $(Z, K) = (1, 0.14)$, the consistency between the simulation results and the experimental data in all devices attests the universality of the proposed model (Fig. 4b).

In view of the effective channel mobility, we have provided a semi-empirical model based on the Matthiessen's rule [15]

$$\mu_{eff}(T) = \frac{\mu_0\left(T/298\right)^{-1.2}}{(2\lambda_0/L+1)\cdot\left[1+\theta_1\left(T/298\right)^{-1.2}\left(1+\theta_2 E_{eff}\right)\right]} \quad (4)$$

where μ_0 is the long-channel low-field mobility at room temperature, λ_0 is the low-field mean free path, $E_{\rm eff}$ is the

TABLE 1. Fitting parameters used in intrinsic device model.

Parameter	Description	Values
Z, K	Fitting parameters characterizing in the V_{TH} model	$Z = 1$ $K = 0.14$
T_0	Critical temperature in the SS model	$T_0 = 40$
D	Smoothing parameter in the SS model	$D = 10$

effective normal field associated with the surface roughness scattering, and θ_1 and θ_2 are size-dependent fitting parameters related to the Coulomb scattering. As shown in Fig. 4c, the dominant Coulomb and surface roughness scattering mechanisms constrain the enhancement of the channel mobility at lower temperatures (even with receding thermionic phonon scattering), and the additional dimension-induced ballistic transport restriction term $(2\lambda_0/L + 1)^{-1}$ results in a greatly-suppressed μ_{eff} amplitude in the short-channel device as compared with the long-channel counterpart.

Besides, in order to describe the saturation of the subthreshold swing at deep cryogenic temperatures, an effective temperature term has been introduced in the conventional SS equation as

$$SS = n(T) \cdot \ln 10 \cdot \frac{k_B T_{\text{eff}}}{q}$$
$$T_{\text{eff}} = \frac{T + T_0 + \sqrt{(T - T_0)^2 + D}}{2} \quad (5)$$

where k_B is the Boltzmann constant, $n(T)$ is interfacial trap-related correction term, D is the smoothing parameter, and T_0 is the critical temperature at which the SS slope tends to saturate. It is worth mentioning that the fitted T_0 is around 40 K for all transistors (inset of Fig. 4d), which suggests the non-linear SS evolution behavior is due to the same energy band tail-induced carrier density saturation mechanism [16].

After detailing the physical origins of the above electrical parameters, we have integrated the relevant temperature-dependent equations into the BSIM-4 framework and adjusted the model parameters in the model card (i.e., key fitting parameters are listed in Table 1 for general audience). Consequently, the modified cryogenic intrinsic compact model can accurately depict the transfer characteristics of transistors (e.g., the $\mu_{\text{eff}}(T)$ and $V_{\text{th}}(T)$ in the trans-conductance simulations are updated with Eqs. (3) and (4)), as shown in Fig. 5.

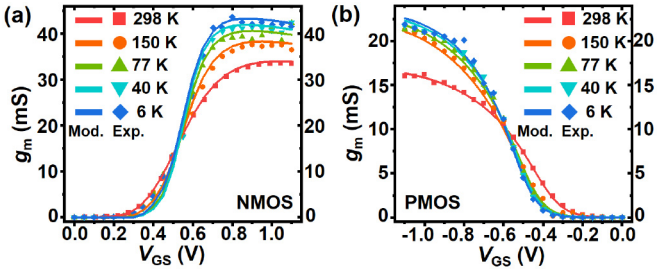

FIGURE 5. Validation of the modified cryogenic intrinsic device model on (a) NMOS and (b) PMOS transistors with the same device structures of $W = 1$ μm, $L = 40$ nm, and $N_f = 32$. The temperature-dependent trans-conductance g_m results (dots) in the saturation region can be well-fitted by the compact model (solid lines).

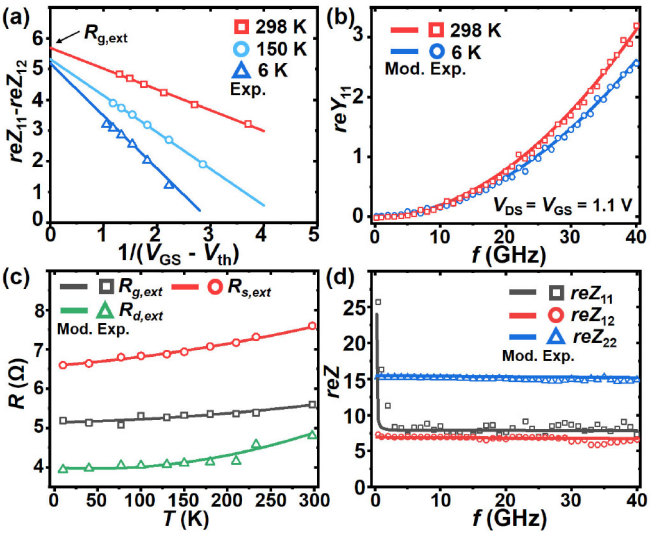

FIGURE 6. (a) Extraction of $R_{g,ext}$ by linear regression of the reZ_{11}-reZ_{12} versus $1/(V_{GS} - V_{th})$ dataset at $V_{DS} = 0$ V. (b) Experimental data and RF model fitting of reY_{11} in saturation region at 298 K and 6 K, respectively. (c) Temperature dependence of the resistive components $R_{g,ext}$, $R_{d,ext}$, and $R_{s,ext}$ of the transistor. (d) Frequency-dependent Z parameters at 6 K with $V_{DS} = 0$ V and $V_{GS} = 1.1$ V.

B. CRYOGENIC LAYOUT-DEPENDENT MOSFET RF MODELING

On the basis of Fig. 4a, the parasitic components important for RF device modeling contain the extrinsic layout-dependent resistances (i.e., the gate electrode resistance $R_{g,ext}$ and terminal resistances $R_{d,ext}$, $R_{s,ext}$), the equivalent substrate resistance R_{sub}, the extrinsic parasitic capacitances $C_{gs,ext}$, $C_{gd,ext}$ and $C_{ds,ext}$ (i.e., metal routing capacitances connected to MOS transistors), gate-to-body capacitance C_{gb}, and the junction capacitance C_{js} and C_{jd}. At the same time, we need to point out that the Source and Drain terminal resistances $R_{d,ext}$ and $R_{s,ext}$ outside the intrinsic MOSFET structure have been considered in the RF simulation, since the internal R_d and R_s inside the intrinsic model only influence the static I-V curves [25].

Subsequently, we have adopted the Cold-FET method to quantify the corresponding frequency and temperature dependences of extrinsic resistors. Guided by the standard process flow developed in [18], the channel bias is always set at $V_{DS} = 0$ V in order to exclude the intrinsic transistor contribution and simplify the equivalent circuit. Next, the gate electrode resistance $R_{g,ext}$ can be attained from the intercept of the linear regression between the reZ_{11}-reZ_{12} curve and the $1/(V_{GS} - V_{th})$ data points as shown in Fig. 6a. The accurate extraction of the parasitic the gate electrode resistance $R_{g,ext}$ ensures the precise modeling of the temperature-dependent input admittance

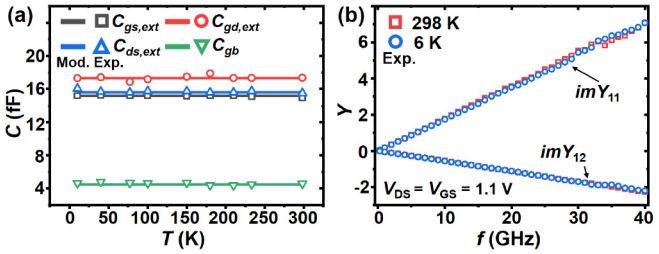

FIGURE 7. (a) Temperature-independent capacitive parameters $C_{gs,ext}$, $C_{gd,ext}$, $C_{ds,ext}$, and C_{gb} are deduced from Y-parameters at $V_{GS} = V_{DS} = 0$ V. (b) Experiment data of imY_{11} and imY_{12} in saturation region at 298 K and 6 K.

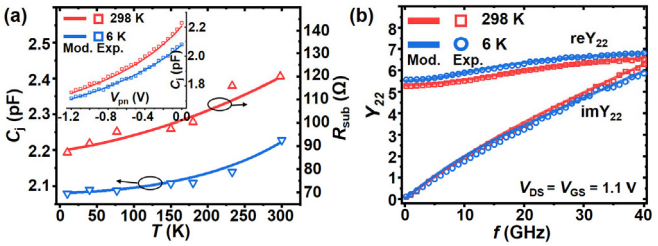

FIGURE 8. (a) Experimental data and fitting results of temperature-dependent substrate components R_{sub} and C_j. Inset: junction capacitance C_j as a function of V_{pn} at 298 K and 6 K. The C-V data of C_j are obtained from diode test structures that mimic the junction capacitance in MOSFETs. (b) Experiment data (dots) and RF model (solid lines) of Y_{22} in saturation region at 298 K and 6 K.

$reY_{11} = Z_{22}/(Z_{11}Z_{22} - Z_{12}Z_{21})$ of the RF transistor device (Fig. 6b). Here, it is noted that the Z-parameters, which are converted from the original S-parameter data [19], do not show any degradation with frequency under different gate voltages. Therefore, the amplitudes of $R_{g,ext}$, $R_{d,ext} = reZ_{22} - reZ_{12}$ and $R_{s,ext} = reZ_{12}$ all remain almost constant in the examined frequency region at each temperature point. Meanwhile, according to the HLMC 40-nm CMOS technology process, both the degenerately-doped poly-silicon gate and silicide Source/Drain configurations will lead to a metallic-like R-T behavior [20]–[23], that is the gate and terminal resistances become smaller with the decrease of temperature, as displayed in Fig. 6c.

Accordingly, an empirical second-order polynomial temperature-correction term $T_{eff,R_\square} = A \times (T - 298)^2 + B \times (T - 298) + 1$ has been introduced to depict these terminal-associated $R_\square(T) = R_\square(298\text{ K}).T_{eff,R_\square}$ curves in which the size-independent coefficients A and B are solely decided by the materials [24], and this modified resistance model also ensures the precise modeling of the frequency-dependent Z parameters of the RF transistor device (Fig. 6d).

In addition to resistances, the extrinsic capacitive parameters ($C_{gs,ext}$, $C_{gd,ext}$, $C_{ds,ext}$, and C_{gb}) in the RF equivalent circuit diagram were acquired from S-matrix under the zero DC bias condition (i.e., $V_{GS} = V_{DS} = 0$ V) following the transformations of $C_{gs,ext} = (imY_{11} + imY_{12})/2\pi f$, $C_{gd,ext} = -imY_{12}/2\pi f$, $C_{ds,ext} = (imY_{12} + imY_{22})/2\pi f$, and $C_{gb} = (imY_{11} + 2imY_{12})/2\pi f$, respectively [24], [25]. These gate-related capacitors, along with relevant Y-parameters, all exhibit negligible variation (i.e., $(C_{\square,T} - C_{\square,298K})/C_{\square,298K} < 5\%$) across the entire temperature (6 – 300 K) and frequency (0.25 – 40 GHz) ranges (Fig. 7).

Moreover, considering the substrate components of the nano-scale transistor determine the output characteristics Y_{22} through the substrate-coupling effects at high frequencies [25], the equivalent substrate resistance R_{sub}, which includes the diffusive resistances in the Source/Drain/bulk wells and the surrounding metal connections between neighboring fingers, is modeled by the 1-R network [27]. Experimentally, this parameter can be converted from $R_{sub} = reY_{sub}/(imY_{sub})^2$ (where the explicit form of Y_{sub} is given in the Appendix) at $V_{GS} = V_{DS} = 0$ V in the intermediate frequency region (i.e., [0.25 GHz, 10 GHz]) [25], [27]. Fig. 8a (red triangles) discloses that the derived R_{sub} data-points tend to decrease as the devices are successively cooled down, possibly benefiting from the degenerate doping of the Source/Drain regions and the parallel-configured metal connections of low-resistivity [28]–[30]. As a result, its temperature-dependent signature can also be captured by the same $R_{sub}(T) = R_{sub}(298\text{ K}).T_{eff,Rsub}$ expression.

Similarly, the diffusion-type C_{js} and C_{jd} (i.e., $C_{js} = C_{jd}$ because of the symmetric structure of MOSFET) experience a monotonic decrease when the temperature drops from 298 K to 6 K, where the experiment data of C_{js} are obtained from specialized test structures. Owning to the incomplete ionization of dopants in the bulk well at low temperatures, the depletion width $W_D(T) = \sqrt{2\varepsilon_{Si}\varphi_{bi}(T)/qN_A^-(T)}$ is progressively broadened because of the de-activated $N_A(T)$ and an enlarged built-in potential $\varphi_{bi}(T) = kT/q \cdot \ln(N_A^-(T) \cdot N_D/n_i(T)^2)$ (where $n_i(T) = \sqrt{N_C N_V}\exp(-E_g/2kT)$ is the intrinsic carrier density [31], [32]) of the Source/Drain-Body junction would regulate the junction capacitance based on the semi-empirical model as:

$$C_j(T) = C_{j0}[1 + \zeta(T - 298)]/\sqrt{1 - V_{pn}/\varphi_{bi}(T)} \quad (6)$$

where $C_{j0} = \varepsilon_{Si}/W_D(T)$, ζ is the fitting parameter affiliated with the temperature correction term, and V_{pn} is the applied voltage. Consequently, as emphasized in Fig. 8, the fitted R_{sub}, C_j, and Y_{22} curves match well with the experimental data in reference to temperature, bias voltage, and frequency (specific fitting parameters and expressions are listed in Table 2 for general audience), hence justifying the underlying device physics of the cryogenic transistors.

C. RF FIGURES OF MERIT

After combining the aforementioned DC/RF electrical parameters into the cryogenic CMOS compact model, we are able to investigate the cutoff frequency f_t (i.e., the main RF FoM of MOSFETs). Specifically, the amplitude of f_t extrapolated from the measured current gain $||H_{21}| - T$ spectrum (i.e., $|H_{21}(f_t)| = 0$ dB) unveils negative correlations with temperature and gate length, as highlighted in Fig. 9. Recall

TABLE 2. Fitting parameters in extrinsic device model.

Parameter	Description	Fitted Expression
$T_{\text{eff,Rg}}$	Temperature coefficient in the $R_{\text{g,ext}}$ model	$T_{\text{eff,Rg}} = 7.16\times10^{-7}\cdot T^2+7.16\times10^{-5}\cdot T+0.91$
$T_{\text{eff,Rd/s}}$	Temperature coefficients for $R_{\text{d,ext}}$ and $R_{\text{s,ext}}$	$T_{\text{eff,Rd/s}} = 6.6\times10^{-7}\cdot T^2+2.24\times10^{-4}\cdot T+0.87$
$T_{\text{eff,Rsub}}$	Temperature coefficient in the $R_{\text{sub,ext}}$ model	$T_{\text{eff,Rsub}} = 2\times10^{-4}\cdot T^2+4.75\times10^{-2}\cdot T+0.87$
ζ	Fitting parameter in the C_{j} model	1.015×10^{-3}

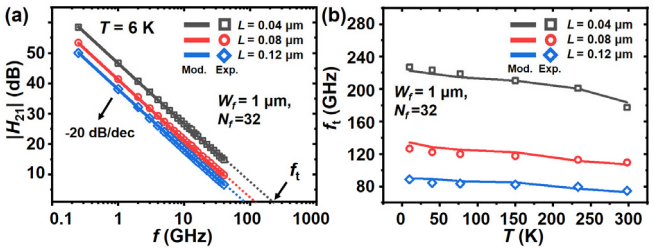

FIGURE 9. (a) Current gain $|H_{21}|$ parameter of MOSFETs with fixed (W, N_f) = (1 μm, 32) but varied channel length (L = 0.04 μm, 0.08 μm, and 0.12 μm) in the frequency spectrum chart. The cutoff frequency is obtained by extrapolating the $|H_{21}| - f$ slope until $|H_{21}| = 0$ dB. (b) Temperature-dependent cutoff frequency of the three devices studied in (a). The $f_t(T)$ values experience a more pronounced enhancement in the L = 0.04 μm device owning to the temperature-induced short channel effect, and the simulation results are in good agreement with the experimental data.

the explicit expression f_t as [33]

$$f_t(T) \approx \frac{g_m(T)}{2\pi\left[C_{gs}\left(1+\frac{R_d(T)+R_s(T)}{r_o}\right)+C_{gd}\left(1+\left(R_d(T)+R_s(T)\right)\left(g_m(T)+1/r_o\right)\right]} \tag{7}$$

where $g_m(T)$ is obtained from the intrinsic device model (Fig. 5), and r_0 is the small-signal output impedance of the MOSFET device, it is thus obvious that both the enhanced transconductance and the diminished parasitic resistance promote the cutoff frequency at lower temperatures, and the resulting HSPICE simulations are in good agreement with the experimental data in the [0.25 GHz, 40 GHz] domain (Fig. 9a). More importantly, the visualized f_t-T evolution trend (Fig. 9b) shows a strong device size-dependent feature, namely the attained f_t of the (W, L, N_f) = (1 μm, 0.04 μm, 32) device improves by a factor of 28% from 298 K (177.4 GHz) to 6 K (227.1 GHz), whereas the degree of the $f_t(T)$ enhancement does not exceed 20% in transistors with same (W, N_f) but longer channel length. In fact, since the low-temperature depletion region broadening not only shrinks the effective channel length, but also reduces the amount of space charge that requires the gate-voltage control, such temperature-induced effect is more evident in short-channel MOSFETs to alleviate the $V_{th}(T)$ shift issue

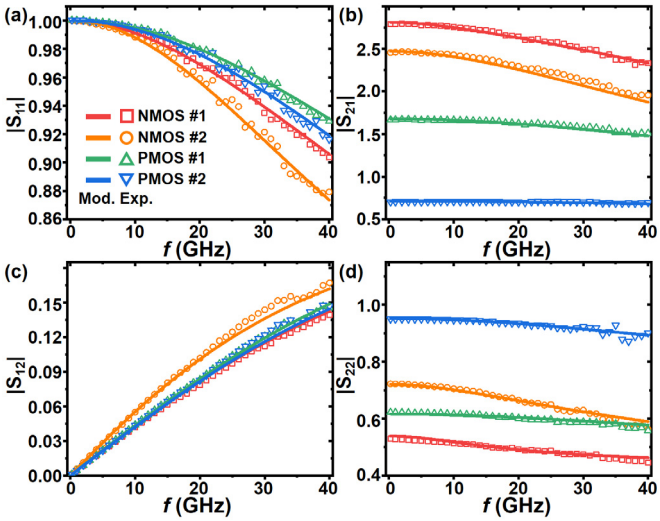

FIGURE 10. Cryogenic MOSFET RF compact model verifications on the magnitudes of (a) S_{11}. (b) S_{21}. (c) S_{12}. (d) S_{22}. The gate geometry of NMOS #1 is (W, L, N_f) = (1 μm, 0.04 μm, 32), NMOS #2 has (W, L, N_f) = (1 μm, 0.08 μm, 32), PMOS #1 has (W, L, N_f) = (1 μm, 0.04 μm, 32), and PMOS #2 structure is (W, L, N_f) = (0.6 μm, 0.12 μm, 32). The DC bias is fixed as $|V_{GS}| = |V_{DS}| = 1.1$ V.

(i.e., $\Delta V_{th} = V_{th}(6\text{ K}) - V_{th}(298\text{ K})$ is found to be 0.1 V and 0.13 V for devices with L = 0.04 μm and 0.12 μm respectively, and relevant ΔV_{th} (T, L) model is elaborated in [15]). Under such circumstances, the increased voltage headroom ($V_{GS} - V_{th}$) would yield a boosted $g_m(T)$ factor which in turn accounts for the highest f_t(6 K)-to-f_t(298 K) ratio in the 0.04 μm-long NMOS transistor.

D. CRYOGENIC RF MODEL VERIFICATION

Finally, by further incorporating the quantified temperature-dependent characteristics of channel mobility, threshold voltage, and RC components into the macro model framework, we have managed to extend the RF device model and related PDK library into the 6 K region. As illustrated in Fig. 10, by applying the cryogenic RF device compact model (i.e., where one set of the key fitting parameters are used in the core physical model), the simulated S-parameters of four different MOSFETs are highly consistent with the experiment results at low temperatures. Likewise, Fig. 11 confirms that the Smith chart simulation curves fit well with the measured data of both NMOS and PMOS devices at T = 6 K, 150 K and 298 K, again demonstrating the validity of the universal device modeling process utilized in this work.

IV. CONCLUSION

In conclusion, by mapping the DC and RF characteristics of nano-scale MOSFETs with sufficient experimental data, we have created a reliable database for cryogenic device modeling. Based on the equivalent RF circuit model, the temperature and frequency-dependent behaviors of each parasitic component have been quantified, and the inclusion of temperature-driven gate geometry effect enables the precise

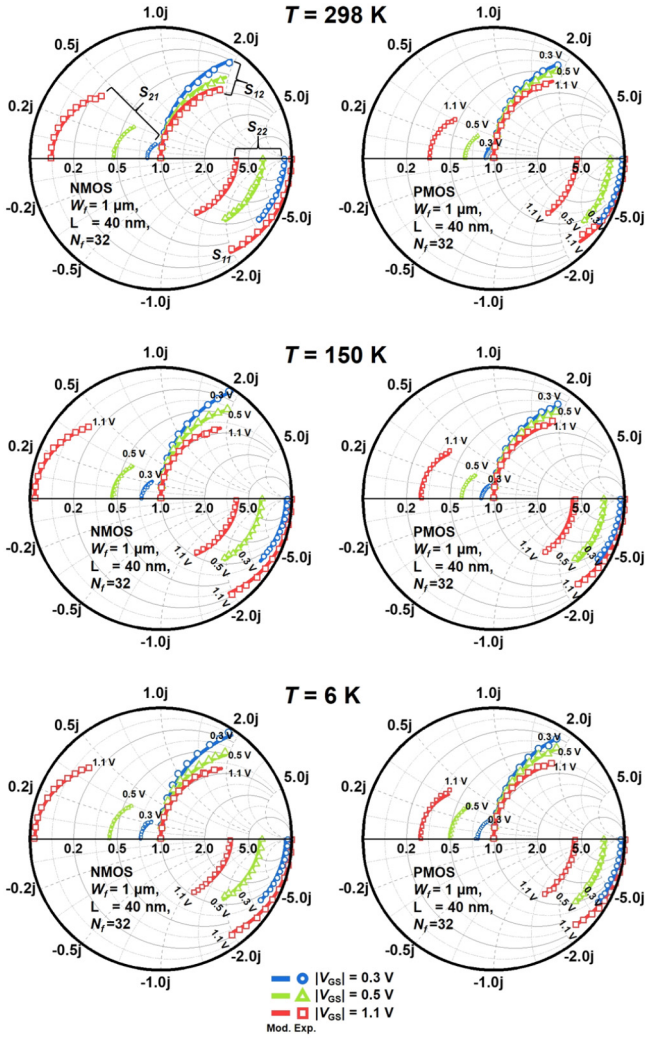

FIGURE 11. Cryogenic MOSFET RF compact model validation on the S-matrix charts of NMOS and PMOS devices with (W, L, N_f) = (1 μm, 0.04 μm, 32). The proposed model can accurately represent the measured S-matrix characteristics in the Smith charts at T = 298 K, 150 K and 6 K. The NMOS and PMOS devices are under different DC bias conditions of ($|V_{GS}|$, $|V_{DS}|$) = (0.3/0.5/1.1 V, 1.1 V).

portrait of the S-matrix across the device size chart. With a further comprehensive study on the device noise analysis at low temperatures, the device physics-enabled generic methodology presented in this work also provide a dependable guidance which facilitates the optimization of cryogenic RF circuit design.

APPENDIX

Transformations between the Y-parameters and Y_{sub}:

$$re\mathrm{Y}_{\mathrm{sub}} = re\mathrm{Y}_{22} - R_{\mathrm{g}}(\omega C_{\mathrm{gd}})^2 - 1/\mathrm{R}_{\mathrm{ds}}$$
$$im\mathrm{Y}_{\mathrm{sub}} = im\mathrm{Y}_{22} - \mathrm{j}\omega C_{\mathrm{gd}}$$
$$R_{\mathrm{sub}} = re\mathrm{Y}_{\mathrm{sub}}/(im\mathrm{Y}_{\mathrm{sub}})^2$$

Transformations between the S-, Y-, and Z-parameters are shown as follows:

S-parameters to Y-parameters conversion

$$Y_{11} = \frac{1}{Z_0}\frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$
$$Y_{12} = \frac{1}{Z_0}\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$
$$Y_{21} = \frac{1}{Z_0}\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$
$$Y_{22} = \frac{1}{Z_0}\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$

S-parameters to Z-parameters conversion

$$Z_{11} = Z_0 \cdot \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{12} = Z_0 \cdot \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{21} = Z_0 \cdot \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{22} = Z_0 \cdot \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}.$$

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