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Reliability Study of 1T1C FeRAM Arrays With $Hf_{0.5}Zr_{0.5}O_2$ Thickness Scaling

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ABSTRACT We have reported that film thickness scaling of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$(HZO) allows hafnium-based one- transistor and one-capacitor (1T1C) ferroelectric random-access memory (FeRAM) to obtain higher cycling tolerance for hard breakdown with lower voltage operation in prior reports. This paper is an extension of the previous works including a review of recent works on FeRAM-related devices from a film thickness scaling point of view. We experimentally verified the cycling tolerance advantage of film thickness scaling by 1T1C FeRAM array with different HZO thicknesses of 8 nm and 10 nm using different small capacitors areas (0.20, 0.40, and 1.00 μm^2) at practical operation conditions for the first time, demonstrating higher reliability at the 8-nm sample with smaller capacitance area. To support the result, time zero dielectric breakdown (TZDB) and time dependent dielectric breakdown (TDDB) were conducted for both 8-nm and 10a-nm samples.

INDEX TERMS Capacitor, ferroelectric random-access memory, hafnium oxide, thickness scaling, zirconium oxide.

I. INTRODUCTION

In recent years, there has been an increase in demand for low-power and high-density embedded memory devices that support cache memory applications. In 2011, ferroelectricity of Si-doped HfO_2 ($HfSiO_2$) was discovered, revealing that a polar-orthorhombic phase in the crystalized $HfSiO_2$ film enables ferroelectricity [1], [2]. HfO_2-based ferroelectric devices have been reported extensively owing to their low energy consumption during active and stand-by operation and compatibility with the CMOS logic fabrication process [3]. Various types of ferroelectric devices have been suggested including ferroelectric field-effect transistors (FeFETs), one-transistor and one-capacitor ferroelectric random-access memories (1T1C FeRAMs), and ferroelectric tunnel junctions (FTJs). To switch the polarity of a ferroelectric film, it is necessary to apply a voltage greater than the coercive field; reducing the ferroelectric film thickness will contribute to lowering the applied voltage. Table 1 presents a comparison of the basic parameters of the FeFET, FTJ, and 1T1C FeRAM with their ferroelectric materials, including thickness.

In the case of FeFETs, a high-density memory array with nondestructive readout operation and support for multibit-level memory has been reported [4]. However, the insulating layer that is easily generated on the Si surface causes charge trapping, leading to dielectric breakdown, which in turn degrades cycling tolerance. The ferroelectric film thickness is optimized considering the ferroelectricity of the ferroelectric layer and dielectric breakdown of the insulator caused by divided voltage [5]–[7]. FTJs allow nondestructive readout operation with a two-terminal structure as resistive random access memories (ReRAMs) that consist of

TABLE 1. Feature comparison.

Device	FeFET	FTJ	1T1C FeRAM (FE-type)		
	[4]	[8]	[12]	[16]	[17]
Nondestructive read	✔	✔			
Low write voltage (≦ 2.0V)				✔	✔
Endurance (> 10^6)			✔	✔	✔
Retention (85°C 10years)	✔		✔	✔	✔
Array operation	✔		✔		✔
Material	Si:HfO_2	Si:HfO_2	Zr:HfO_2	Zr:HfO_2	Zr:HfO_2
Thickness	7- 9 nm	5 - 7 nm	10 nm	4 nm	8 nm

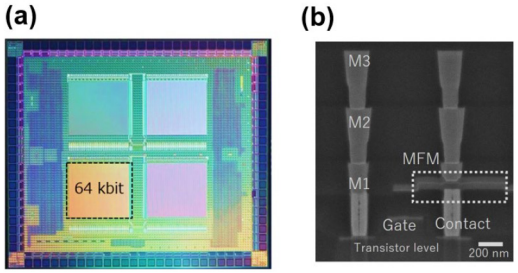

FIGURE 1. (a) Optical micrograph of the FE-typed 1T1C FeRAM with 4 mats consisting of different sizes of MFM capacitors, (b) Cross-sectional SEM image of a 1T1C memory cell with a capacitance area of 1.00 μm^2 [12].

metal/ferroelectric/metal (MFM). An intermediate interfacial layer is usually fabricated as a tunneling layer on the metal electrodes [8]–[10]. Compared with other ReRAMs, these devices have the potential to be high-density and low-power neuromorphic devices owing to their high resistance during the multiply-accumulate operation. The thickness of the ferroelectric film is optimized to control the modulation of the barrier height through the ferroelectric materials and the intermediate interfacial layer while taking the tunneling current into account.

In terms of 1T1C FeRAMs, many researchers have reported that MFM capacitor exhibits high cycling tolerance for hard breakdown owing to the good interfacial property between the ferroelectric layer and metal electrodes [11]–[13]. In addition, anti-ferroelectric type (AFE-type) 1T1C FeRAMs comprising tetragonal phase dominant HfO_2-based ferroelectric material have been proposed. The remanent polarization of the AFE-type 1T1C FeRAMs becomes smaller than that of ferroelectric type 1T1C FeRAMs, but low operation voltage with high endurance would be obtained [14], [15]. On the other hand, film thickness scaling allows ferroelectric type (FE-type) 1T1C FeRAMs to reduce the operating voltage more flexibly compared with FeFETs or FTJs, owing to the thickness optimization between the ferroelectric layer and insulation layer. The strategy of low-voltage operation using film thickness scaling was comprehensively reported, revealing a 1.2 V operation with 4-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ (HZO) using a large single capacitor [16].

We have reported a 64 kbit FE-type 1T1C FeRAM with higher cycling tolerance for hard breakdown with lower voltage operation via HZO film thickness scaling [17], [18]. In this study, we present an extension of the previous work on investigating film thickness scaling and experimentally demonstrating its effect by array-level endurance analysis for the first time. Furthermore, time zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) on single large capacitors with 10-nm-thick HZO (10-nm) and 8-nm-thick HZO (8-nm) samples were conducted to support the result.

II. EXPERIMENT

A. DEVICE FABRICATION

A 64 kbit FE-type 1T1C FeRAM array was integrated by using 130-nm CMOS technology [12]. The structure of a capacitor under bitline (CUB) was adopted to the memory array. Planer type of MFM capacitors comprising PVD-TiN/ALD- $Hf_{0.5}Zr_{0.5}O_2$/CVD-TiN were stacked on the contact plug of the planer transistor. Two different HZO samples with thickness values of 8 nm and 10 nm were prepared to investigate array-level film thickness scaling. The HZO thickness was confirmed by ellipsometer measurement. Rapid thermal annealing (RTA) at 600 °C was performed on both the HZO samples to obtain a significant ferroelectric property with high remanent polarization (2Pr) from a memory window point of view. If insufficient thermal budget is applied to the capacitors, the film would contain more anti-ferroelectric or amorphas domains, resulting in lower remanent polarization. The RTA did not degrade the characteristics of the CMOS transistors post back-end-of-line (BEOL) process [13]. Fig. 1 shows a device structure of the test chip for optical micrograph in Fig. 1 (a) and cross-sectional scanning electron microscopy image of a memory cell which has a capacitor of size 1.00 μm^2 in Fig. 1 (b). Four different mats, which had 64 kbits MFM capacitors, were mounted on the same chip with each capacitor in the memory cell having a size of 0.06, 0.20, 0.40, and 1.00 μm^2, respectively. The intrinsic ferroelectricity and TDDB investigations of the MFM capacitors were electrically investigated using a single large MFM capacitor with an area of 1,000 μm^2 and was composed of 1,000 capacitors (each of area 1 μm^2) connected in parallel for both the 10-nm and 8-nm samples.

B. VALIDATION OF 1T1C FERAM ARRAY

Fig. 2 (a) shows a schematic figure of the 1T1C FeRAM array with a sense amplifier (SA), which is simplified to explain an operation principle. The capacitance of MFM (C_{FE}) was controlled by applying the voltage of a word line (WL), bitline (BL), and plate line (PL). Fig. 2 (b) illustrates the definition of C_{FE} as C0 (when reading data0) or C1 (when reading data1). Thus, higher voltage change (ΔV_{BL})

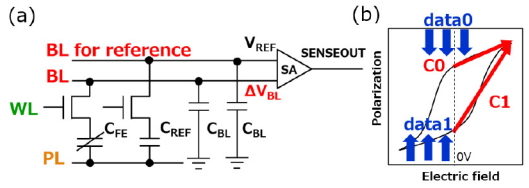

FIGURE 2. (a) Schematic illustration simplified to a 1T1C memory cell connected to SA with a reference capacitor. (b) Definition of the C_{FE} as C0 (when reading data0) or C1 (when reading data1) [13].

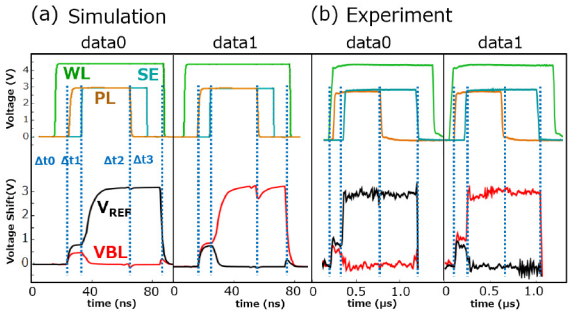

FIGURE 3. Validation result of a read operation for a 1T1C FeRAM memory cell for reading data0 and reading data1. (a) Timing diagrams of the simulation results (b) Experimental waveforms [13].

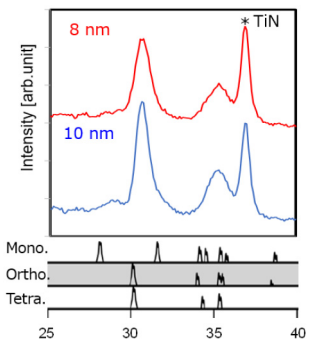

FIGURE 4. GIXRD spectra of the MFM capacitors on 8-nm and 10-nm HZO samples.

is obtained when reading data1 according to C_{FE}. The reference voltage (V_{REF}) can be modified by externally applying a voltage or internally generating a voltage using the reference capacitance (C_{REF}).

Fig. 3 demonstrates the timing diagrams of a step pulse sensing scheme for data0 and data1 on the 1T1C memory cells: (a) simulation results and (b) experimental waveforms. A high value of ΔV_{BL} or V_{REF} was successfully activated as simulation results when reading data0 or data1.

III. RESULTS AND DISCUSSION

A. FERROELECTRICITY OF THE FILM

Fig. 4 demonstrates the presence of ferroelectric orthorhombic phases in both the 10-nm and 8-nm samples via grazing-incidence X-ray diffraction (GIXRD). The intensities related to the ferroelectric orthorhombic phases were similar in both cases at around 30°, while a slightly higher

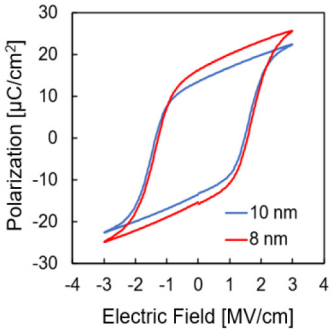

FIGURE 5. P-E characteristics of the 8-nm (red) and 10-nm (blue) samples using single large MFM capacitors at 1 kHz after 100 cycles over an area of 1,000 μm^2.

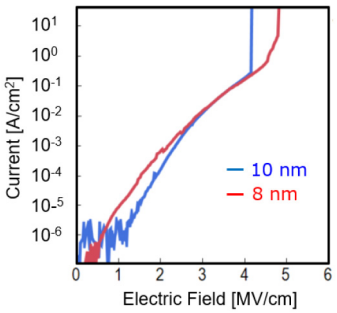

FIGURE 6. J–E characteristics (2 V/s) of the 8-nm (red) and 10-nm (blue) samples using pristine single large MFM capacitors of area 1,000 μm^2 each and comprising 1,000 capacitors (each of area 1 μm^2) connected in parallel.

intensity of the monoclinic related phase was observed for the 10-nm samples at around 28°. Fig. 5 shows the remanent polarization of the MFM for both samples that are characterized by polarization versus voltage measurements with a maximum applied electric field of 3 MV/cm. The ferroelectric hysteresis indicates the presence of a ferroelectric orthorhombic phase in each case. A slightly higher remanent polarization ($2P_r$, ~32 $\mu C/cm^2$) was observed on the 8-nm sample than on the 10-nm ($2P_r$, ~27 $\mu C/cm^2$) sample, which is in agreement with the GIXRD results.

B. RELIABILITY CHARACTERIZATION USING A SINGLE CAPACITOR

Reliability analyses were conducted on the intrinsic ferroelectric films of 8-nm and 10-nm samples using MFM capacitors with a total area of 1,000 μm^2 each. The electric breakdown electric field (E_{BD}) was 4.8 MV/cm for the 8-nm sample, while 4.2 MV/cm on the 10-nm sample based on J–E measurements (Fig. 6). This phenomenon can be explained by a similar theory with regard to the metal/oxide/silicon (MOS) structure, which shows better breakdown tolerance on thinner SiO_2 from lower electron energy for a given field [16], [20].

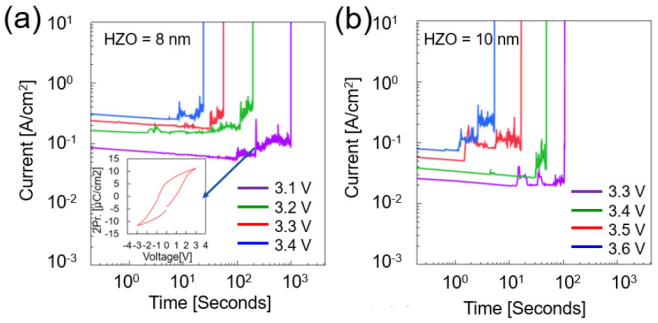

FIGURE 7. Current–time trace measurements of the (a) 8-nm and (b) 10-nm samples using pristine single large MFM capacitors of area 1,000 μm^2 each and comprising 1,000 capacitors (each of area 1 μm^2) connected in parallel. The inset in (a) describes the P–E characteristics post soft breakdown during the current–time trace measurement on another device under the same test conditions.

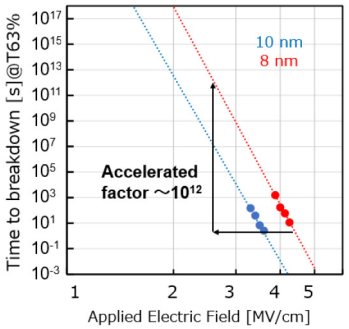

FIGURE 8. The t_{BD} at 63% (T_{63}) versus electric field in a log–log graph for both 8-nm (red) and 10-nm (blue) samples. A total of 22 devices were tested for stress for each sample. Weibull slopes of 1.01 and 1.00 were used for the 8-nm and 10-nm samples plots, respectively.

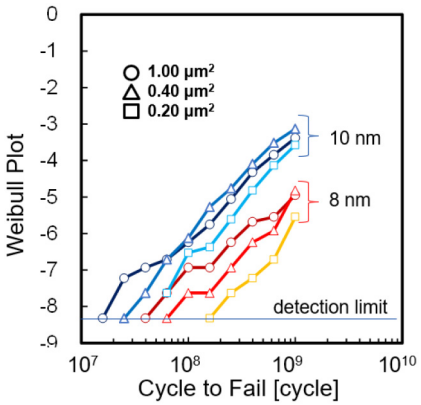

FIGURE 9. Weibull fitting plot as a function of the number of cycles to failure for 4 kbits of the 8-nm and 10-nm samples at a capacitance area in a memory cell of 0.20, 0.40 and 1.00 μm^2 with a same stress electric field of 4.4 MV/cm on both samples.

The TDDB characteristics of the MFM capacitor were obtained by current–time trace test (Fig. 7). Constant voltage stress values of 3.3 V (3.3 MV/cm), 3.4 V (3.4 MV/cm), 3.5 V (3.5 MV/cm), and 3.6 V (3.6 MV/cm) were applied to the 10-nm samples, while stress values of 3.1 V (3.9 MV/cm), 3.2 V (4.0 MV/cm), 3.3 V (4.1 MV/cm), and 3.4 V (4.3 MV/cm) were applied to the 8-nm samples. The current was gradually decreased with time, and soft breakdown was observed before hard breakdown through the film. This phenomenon can be explained by the generation of trap sites in the film, where the generated defects create a percolation path along the trap sites [21]. The P–E characteristics post soft breakdown were examined to confirm the ferroelectricity, with the result that clear remanent polarization was obtained (see inset of Fig. 7(a)). Therefore, the hard breakdown time (t_{BD}) of the film was extracted as the lifetime at which the current flow exceeds 10 A/cm^2, resulting in lower t_{BD} at higher applied voltages. The t_{BD} at 63% (T_{63}) versus electric field for samples of both thicknesses were plotted in a log–log graph (Fig. 8). The t_{BD} follows a power-law fit ($t_{BD} \propto V^{-n}$) for both samples, as commonly accepted [22]. The t_{BD} of the 8-nm sample was longer than that of the 10-nm sample, which is in good agreement with the value of E_{BD} in Fig. 6 while maintaining parallelism. The accelerated factor of the t_{BD} from 3.5 V (4.4 MV/cm) to 2.0 V (2.5 MV/cm) for the 8-nm sample was extracted at approximately 10^{12}, as shown in Fig. 8. Considering these effects, film thickness scaling results in a reliable hard breakdown when operating at 2.0 V using a 1T1C FeRAM array.

C. RELIABILITY CHARACTERIZATION FOR 1T1C FERAM ARRAY

The properties of the 1T1C FeRAM array using 8-nm and 10-nm samples consisting of TiN/HZO/TiN capacitors were previously reported in [17], [18]. The RBERs due to hard breakdown were investigated on both 8-nm and 10-nm samples using 4 kbits for capacitors with different capacitance areas of 0.20, 0.40, and 1.00 μm^2 in a memory cell, as shown in Fig. 9. Cycling stress was applied with 4.4 MV/cm, 100 ns, and 85 °C as an accelerated condition. The cycle to failure of the earliest bit on the 8-nm sample was longer than that of the 10-nm sample in any capacitor size, which is in good agreement with the TDDB results in Fig. 8. The area dependence on the cycle to failure was clearly observed following the Poisson distribution [23]. The area dependence converged as the number of cycles increased, implying that the failure mechanism changed with increased cycling. One possible explanation for this phenomenon is that as the number of cycles increased, too many trap sites were generated in the film, obscuring the dependence on the area. The cycling tolerance for hard breakdown at an RBER of 1 ppm on the 8-nm sample was predicted under the operating conditions of 2.0 V and 100 ns at 85 °C at a capacitor area of 0.20 μm^2 in the memory cell, as shown in Fig. 10. Considering the accelerated factor extracted from the TDDB results in Fig. 8, the value was projected to be 3.2×10^{18}. Lower cycling tolerance for hard breakdown was obviously predicted for the 10-nm sample using the data on Fig. 8 and Fig. 9 with a same method. (Not shown)

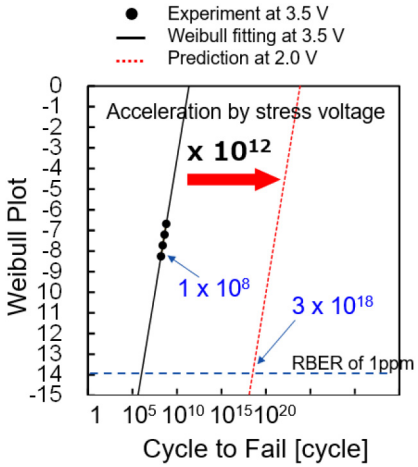

FIGURE 10. **Weibull fitting plot as a function of the number of cycles to failure for the 8-nm-thick sample at a capacitance area in a memory cell of 0.20 μm^2. The black line shows a fitting curve based on the experimental results at an operating voltage of 3.5 V. The red line shows a projection at 2.0 V using accelerated factor extracted from Fig. 8 [16].**

For further reliability analyses, the retention and fatigue characteristics of the MFM capacitors need to be investigated. We characterized the retention characteristics using a single large capacitor in a previous study [17] and obtained negligibly small changes in polarization. In terms of the fatigue characteristics, the remanent polarization was observed to degrade by 30% during 10^9 cycles owing to the domain pinning in the MFM film [17]. For practical endurance behavior of 1T1C FeRAMs, we need to consider the degradation due to fatigue; nonetheless, enlarging the remanent polarization or increasing the sensitivity of SA would solve the problem.

IV. CONCLUSION

We investigated the recent studies on various HfO_2-based ferroelectric devices in terms of film thickness, suggesting that the 1T1C FeRAM has a potential for higher cycling tolerance for hard breakdown and lower operating voltage by film thickness scaling technology. To ensure the benefits of the film thickness scaling, we investigated the reliability of MFM films with $Hf_{0.5}Zr_{0.5}O_2$ thicknesses of 10-nm and 8-nm. A higher E_{BD} was observed for TZDB measurements on the 8-nm sample, and longer t_{BD} at the same stress electric field was observed for TDDB measurements, which are in good agreement with the results of previous works [17], [18]. Furthermore, we experimentally verified the cycling tolerance advantage of film thickness scaling by 1T1C FeRAM array with different HZO thicknesses of 8 nm and 10 nm using different small capacitor areas (0.20, 0.40, and 1.00 μm^2) for the first time, demonstrating a cycling tolerance value higher than 10^{18} for hard break-down at an operating voltage of 2.0 V and operating speed of 100 ns at 85 °C on the 8-nm sample with consistent HZO thickness and capacitance area dependence. It allows 1T1C FeRAM to further lower the operating voltage or improve the cycling tolerance using a ferroelectric layer that is thinner than 8 nm. Although the higher thermal budget is required to obtain ferroelectricity on a thinner HZO [16], this CUB structure has the advantage of increased thermal budget. However, the increased leakage current of capacitors would limit film thickness scaling and prevent the ideal voltage from being applied to the capacitors, which are shared with the plate lines or bit lines. A continuous feasibility study about the reliability of the 1T1C FeRAM array, such as fatigue and retention characteristics, would therefore be required for practical application of various nonvolatile memory; this investigation will be conducted in a future study.

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