Received 17 March 2022; revised 18 May 2022 and 16 June 2022; accepted 20 June 2022. Date of publication 22 June 2022; date of current version 11 July 2022. The review of this article was arranged by Editor M. T. A. Rahimo.

Digital Object Identifier 10.1109/JEDS.2022.3185526

Channel Design Optimization for 1.2-kV 4H-SiC MOSFET Achieving Inherent Unipolar Diode 3rd Quadrant Operation

DONGYOUNG KIM (Student Member, IEEE), NICK YUN (Student Member, IEEE), SEUNG YUP JANG (Member, IEEE), ADAM J. MORGAN (Member, IEEE), AND WOONGJE SUNG (Member, IEEE)

College of Nanoscale Science and Engineering, State University of New York Polytechnic Institute, Albany, NY 12203, USA

CORRESPONDING AUTHOR: D. KIM (e-mail: kimd1@sunypoly.edu)

This work was supported in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, the Vehicle Technologies Program Office under Award DE-EE0008710.

ABSTRACT 1.2 kV 4H-SiC MOSFETs operating with a low knee voltage and forward voltage drop under third quadrant mode are proposed and experimentally demonstrated by using optimized accumulation mode channels to eliminate external SiC SBDs in power converter applications. By removing epitaxial regrowth process step, the overall fabrication process for the proposed MOSFET is more concise and manageable. Channel design parameters, such as channel doping concentration, channel length, and different gate oxides were investigated to achieve low knee voltage and forward voltage drop under third quadrant operation mode ensuring high breakdown voltages. To understand the impact of channel potential (barrier) on the current conduction behavior as well as leakage current during the blocking mode, 2D simulations were conducted. In addition, the reverse recovery characteristics and switching characteristics are discussed. Based on the optimized channel design, the promising devices for high density power electronics are proposed.

INDEX TERMS SiC, MOSFETs, channel length, channel diode, channel doping, gate oxide, third quadrant, channel potential.

I. INTRODUCTION

SiC Schottky Barrier Diodes (SBDs) have been used in parallel with SiC MOSFETs as a freewheeling diode in power converter applications because the inherent PN body diode of the MOSFET has relatively high forward voltage drop, considerable reverse recovery current, and suffers from the expansion of stacking faults over the lifetime of the device [1]. However, an additional external diode requires extra space within a multi-chip package or power module, and adds undesirable parasitic inductance to the power loop during commutation events of the power converter. Alternatively, when the unipolar diode structure is integrated within the MOSFET, a significant reduction in wafer area is achieved by sharing active and edge termination areas. Monolithic integration of Schottky or JBS diode in a SiC MOSFET structure (JBSFET) and SiC MOSFET integrating the unipolar internal inverse channel diode were reported earlier [2]–[5], respectively. However, JBSFET from [2] has higher specific on-resistance due to the larger cell pitch from the portion of JBS diode when compared with standalone MOSFET. For [5], the fabrication of the proposed MOSFET requires a very thin and heavily doped epitaxial regrowth process, which may result in a complicated process.

In this paper, eliminating the regrowth process, 4H-SiC MOSFETs with inherent unipolar diode are proposed by controlling channel design parameters: channel doping, channel length, and gate oxide. MOSFETs with various channel doping concentrations, channel lengths, and gate oxides were successfully fabricated and investigated. In order to further clarify the effect of channel potential, Sentaurus 2D

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

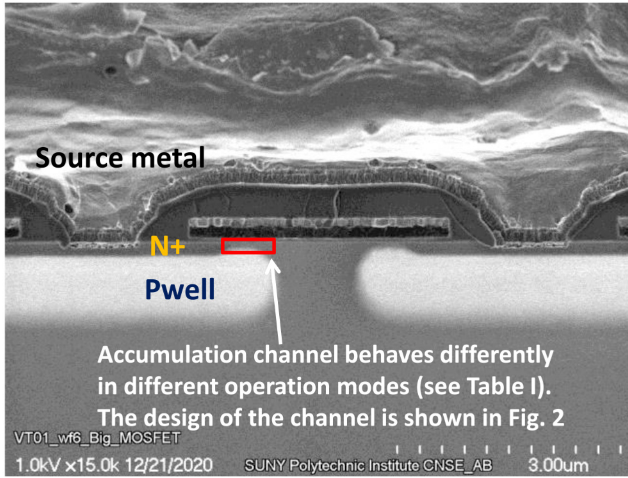


FIGURE 1. The cross-sectional SEM image of 1.2 kV accumulation channel mode MOSFETs.

TABLE 1. Operation modes of 1.2 kV MOSFET with channel diode.

Operation modes	Vgs	Vds	
Forward conduction	> Vth (15 ~ 20V)	~ 1V	Strong accumulation of electrons when Vgs > Vth; channel is formed.
Forward blocking	0V	> 1200V	Channel is closed due to the ***potential barrier*** formed by depletion region extended from Pwell.
3Q conduction (channel diode)	0V	>~ -3V	***Potential barrier*** becomes lower due to Vds < 0V allowing current conduction. Vds should be larger than approximately -3V in order to prevent bipolar operation of the PN body diode.

TCAD was implemented and utilized. In addition, the reverse recovery characteristics and switching characteristics are discussed.

II. DEVICE CONCEPT

Fig. 1 shows the cross-sectional SEM image of the 1.2 kV MOSFET with accumulation mode channel [6]. The proposed accumulation mode channel needs to be optimized to satisfy low on-resistance, unipolar operation in the 3rd quadrant (3Q) mode, and low leakage in the blocking mode, as shown in Table 1. Fig. 2 (a) shows designed implant profiles for the JFET and P-well implantation using process simulation from Synopsys [7]. The net doping was calculated based on Fig. 2 (a), as shown in Fig. 12 (b). Accumulation mode channel was formed by only using JFET and P-well implants [6]. The doping and depth of accumulation channel were determined by JFET implants.

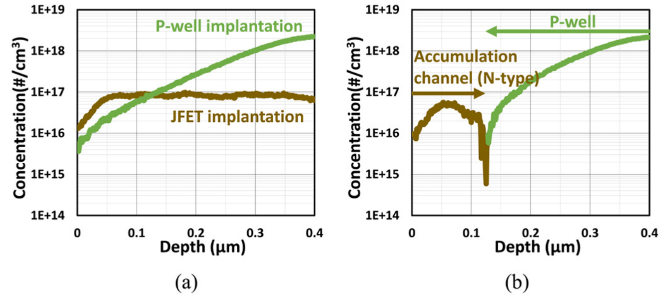
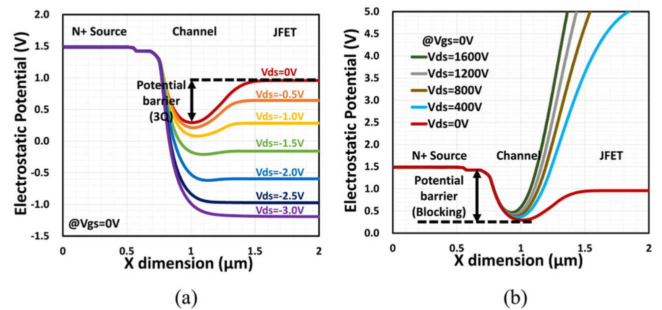


FIGURE 2. (a) Designed implant profiles for JFET and P-well implantation using SPROCESS. (b) Net doping profile.



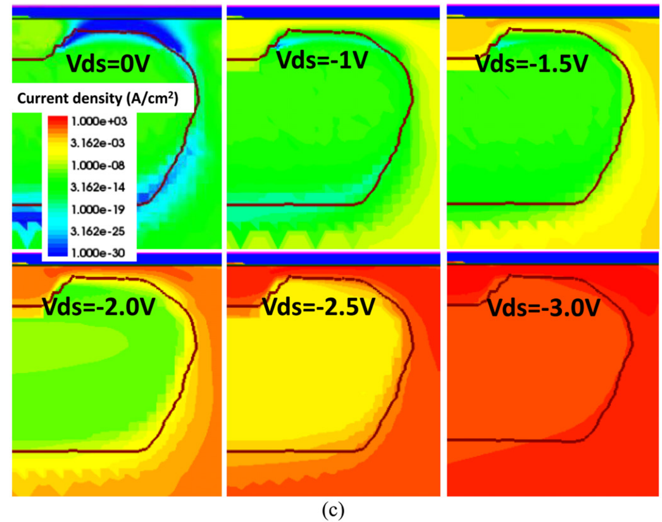


FIGURE 3. Simulated electrostatic potential at channel region of MOSFETs with accumulation mode channel under (a) third quadrant mode, (b) forward blocking mode, and (c) the cross-sectional view of simulated current density for accumulation mode channel MOSFETs at various drain voltages (Vgs = 0V).

The key aspect to consider for a MOSFET with channel diode is the potential barrier in the channel region. Fig. 3 (a) and (b) show simulated electrostatic potential at the channel region under third quadrant conduction mode and forward blocking mode, respectively. When potential barrier between the channel and JFET region is overcome by applying negative drain-source voltage (V_{ds}), current flows through the channel region even before the conduction of the PN body diode. The low potential barrier allows low knee voltage, providing the decrease of forward voltage drop during the

3Q operation. On the other hand, under the forward blocking mode, potential barrier between N+ source and channel region determines the blocking behaviors of MOSFETs. High positive drain voltage makes the potential barrier formed in the channel low (in magnitude) and thin (in width). In order to suppress leakage current from the channel region, a high and wide channel potential is required. A specific channel design would result in a trade-off relationship between third quadrant conduction mode and forward blocking mode. Therefore, an optimized channel design is required to provide both low knee voltage and high breakdown voltage with low leakage current. The channel potential is governed by various parameters such as channel doping, channel length, and gate oxide, which will be discussed in the next chapter.

Fig. 3 (c) shows cross-sectional views of simulated current density in the accumulation mode channel at various drain voltages. At V_{ds} of 0 V, channel is closed, resulting in insignificant current flow. At V_{ds} of ≤ -1.0 V, current starts flowing through the channel regions. As the V_{ds} decreases, so too does the current density due to the channel region becoming fully open, providing high conduction behavior. The PN body diode also turns on at V_{ds} of approximately -3.0 V and current flows through both the channel and body diode. Depending on the channel potential, knee voltage of MOSFETs under third quadrant mode is altered, resulting in a change of the forward voltage drop. MOSFETs with low channel potential provide low knee voltage, which in turn enables then high current to flow through the channel region. Thus, MOSFETs with low knee voltage (attributed to a low channel potential) enable high reverse conduction currents to be commutated through the MOSFET before the operation of the PN body diode kicks in and begins to dominate reverse conduction behavior. However, extremely low knee voltage causes high leakage current in the forward blocking mode due to low channel potential. Therefore, it is important to optimize channel parameters to achieve low leakage current while maintaining low forward voltage drop during the 3rd quadrant behavior.

III. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated at Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, USA [8], [9]. A 10 μm thick drift layer with N- epi doping concentration of about 8×10^{15} cm^{-3} on a 6-inch, N+ 4H-SiC substrate was used for the fabrication of 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were implemented to make P-well/P+ body/JTE, and JFET/N+ source, respectively. The average doping concentrations in the JFET region of $5 \times 10^{16}, 7 \times 10^{16}$, and 9×10^{16} cm^{-3} were used to investigate the effect of the channel doping concentration on the operation of MOSFET with channel diode; the resultant effective channel doping are 3, 5, and $7{\times}10^{16}$ cm^{-3}, respectively. After implantation steps, a 1650 °C 10-min activation anneal with a carbon cap was conducted. To investigate the impact of gate oxide, MOSFETs with 3 different gate oxides were fabricated; 25 nm deposited- 50 nm deposited-, and 50 nm thermally grown- gate oxides. For the deposited gate oxide of 50 (25) nm, 2 nm thermal oxide was grown and then high temperature oxide (HTO) of 48 (23) nm was deposited. After the formation of gate oxide, a post oxidation anneal (POA) in N_2O ambient was implemented for high channel mobility. The N-type polysilicon was deposited and patterned for the formation of the gate. Afterwards, inter-layer dielectric (ILD) was deposited, patterned, and etched to make ohmic contact regions. Nickel (Ni) was deposited on the front side, followed by RTA for the self-aligned silicidation process. Next, unsilicided Ni metals were removed and annealed by a 2-min RTA at 965 °C for the front side ohmic contact. Backside metal contact was also deposited using Ni, followed by the same RTA process. A 4 μm thick Ti/TiN/Al metal stack was deposited as the source and the gate metal. Silicon nitride and polyimide were used for passivation on the frontside. Finally, a solderable metal stack was deposited on the backside. No substrate thinning process was adopted.

TABLE 2. Device description of the fabricated 4H-SiC MOSFETS.

	Gox thickness	Channel doping (#/cm^3)	L_{ch} (μm)
D1	Thermal (50nm)	**3×10^{16}**	0.5
D2	Thermal (50nm)	**5×10^{16}**	0.5
D3	Thermal (50nm)	**7×10^{16}**	0.5
D4	Thermal (50nm)	3×10^{16}	**1.0**
D5	Thermal (50nm)	3×10^{16}	**0.4**
D6	Thermal (50nm)	3×10^{16}	**0.3**
D7	**Deposited (50nm)**	3×10^{16}	0.5
D8	**Deposited (25nm)**	3×10^{16}	0.5

*G_{ox}=gate oxide, L_{ch}=channel length.

IV. RESULTS AND DISCUSSION: OPTIMIZATION OF CHANNEL POTENTIAL

A. CHANNEL DOPING CONCENTRATION

Table 2 shows the description of the fabricated 4H-SiC MOSFETs to optimize the accumulation channel. Fig. 4 shows the cross-sectional SEM image of MOSFETs with channel length (L_{ch}) of 0.5 μm and channel doping of 3×10^{16} cm^{-3}. Fig. 5 shows the designed implant profile for different channel doping concentrations. Although channel depth is one of the important factors in channel potential, in this case, the effect of channel depth was included in that of channel doping. In other words, the channel depth is determined by various doping concentrations with fixed P-well profile.

Measured forward conduction behaviors of the fabricated 1.2 kV MOSFETs with different channel doping (L_{ch} of 0.5 μm) are shown in Fig. 6 (a). MOSFETs were measured at gate-source biases of 0 to 20 V with 10 V steps. The increase of channel doping provides better conduction behaviors. In terms of channel doping of 3, 5, and 7×10^{16} cm^{-3}, the resultant $R_{on,sp}$ is 4.54, 4, and 3.83 mΩ-cm^2, respectively

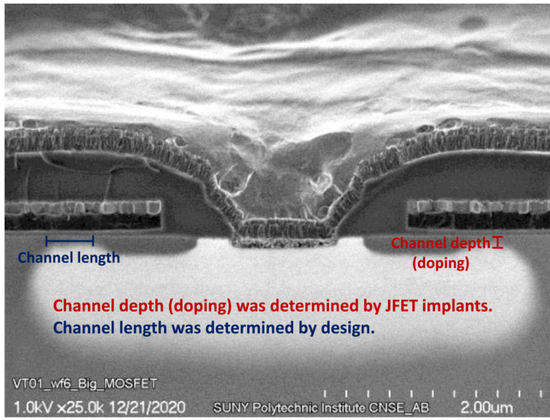


FIGURE 4. **The cross-sectional SEM image of 1.2 kV accumulation channel mode MOSFETs with channel length of 0.5 μm and channel doping of 3×10^{16} cm^{-3}.**

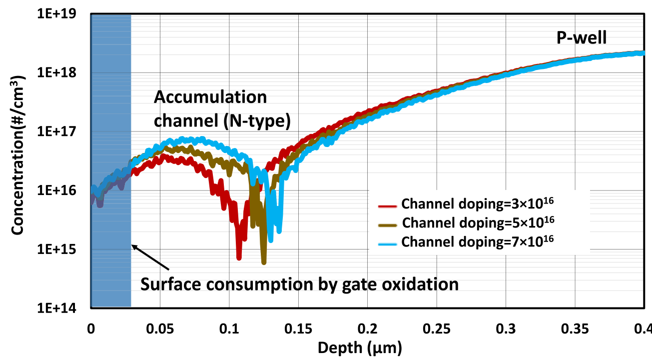


FIGURE 5. **Designed implant profiles for channel region and P-well for different channel doping using SPROCESS.**

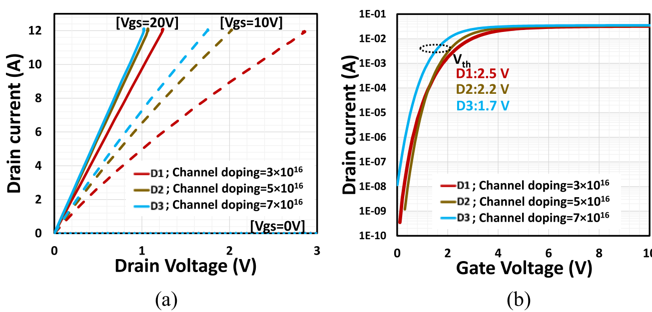


FIGURE 6. **(a) Measured output and (b) transfer characteristics of MOSFETs with different channel doping.**

(specific on-resistance was extracted from output characteristics at V_{gs} of 20 V and V_{ds} of 0.1 V). Increased JFET doping and thus channel doping reduces the channel resistance as well as the JFET resistance. Fig. 6 (b) shows transfer characteristics of MOSFETs with different channel doping. For D1, D2, and D3, V_{th} is 2.5, 2.2, and 1.7 V, respectively (V_{th} was extracted at V_{ds} of 0.1 V and I_{ds} of 5 mA).

Measured third quadrant behaviors and forward blocking mode of MOSFETs with various channel doping are shown in Fig. 7 (a) and (b), respectively. L_{ch} of 0.5 μm

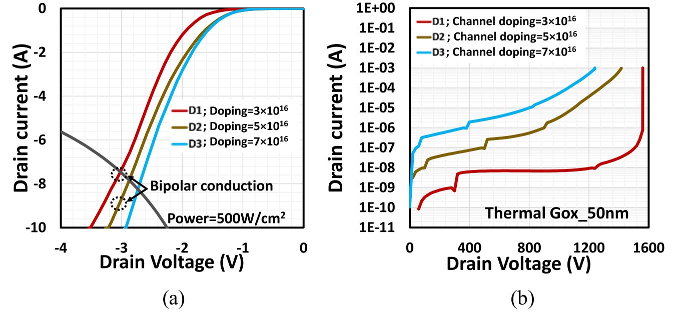


FIGURE 7. **(a) Measured third quadrant behaviors and (b) forward blocking mode at V_{gs} of 0 V of MOSFETs various channel doping.**

was used to examine the impact of channel doping. Due to the accumulation mode channel, MOSFETs provide current conduction with a knee voltage of 1∼1.5 V under third quadrant mode as shown in Fig. 7 (a); the criteria of usable unipolar channel diode current was defined at power density of 500 W/cm^2 [10], [11]. The high channel doping results in the reduction in the knee voltage and the forward voltage drop under third quadrant behaviors due to the decrease of channel potential. However, low channel potential results in high leakage current, contributing to low breakdown voltage, as shown in Fig. 7 (b). The criteria to determine whether the low leakage current or high leakage current is 1 μA at V_{ds} of 1200 V. Channel doping of 3×10^{16} cm^{-3} for L_{ch} of 0.5 μm provides high breakdown voltages with low leakage current. Although channel doping of 5×10^{16} cm^{-3} have high leakage current, it allows blocking of >1.2 kV. However, it is difficult for channel doping of 7×10^{16} cm^{-3} to be used in SiC MOSFETs with a 1.2 kV rating due to low breakdown voltage. It is discovered that the optimized channel doping allows MOSFETs to provide the low knee voltage and high conduction behaviors under third quadrant mode with high breakdown voltage.

In order to elucidate the decreasing slope of the current under the third quadrant after operating the PN body diode, Sentaurus 2D TCAD simulation was conducted. Fig. 8 (a) shows the simulated current density of MOSFETs with low and high P contact resistance at V_{ds} of −1.5 V and −4.5 V, which are before and after operating PN body diode, respectively. Fig. 8(b) shows the drain current density of MOSFETs with low and high P contact resistance. Before PN body diode operation, drain current density is identical regardless of P contact resistance. However, MOSFETs with low P contact resistance allow current density to be high after the PN body diode turns on. Fig. 8 (c) shows the electron current density from N contact and P contact of MOSFETs with low and high P contact resistance. Not only is higher channel current density (i.e., current density from N contact) observed, but also higher body diode current density (i.e., current density from P contact) are achieved in MOSFETs with low P contact resistance when compared to MOSFETs with high P contact resistance, as shown in Fig. 8 (a) and (c). When the PN body diode turns on, the potential barrier in

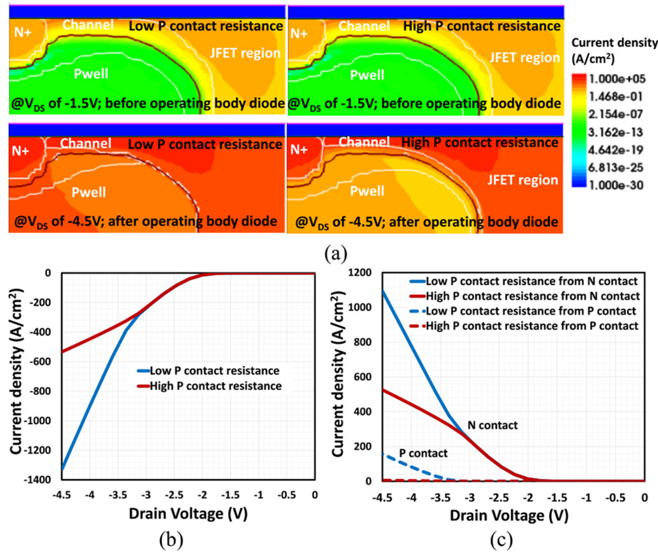


FIGURE 8. (a) Simulated current density at V_{ds} of −1.5 V and −4.5 V, (b) drain current density, and (c) electron current density from N contact and P contact of MOSFETs with low and high P contact resistance.

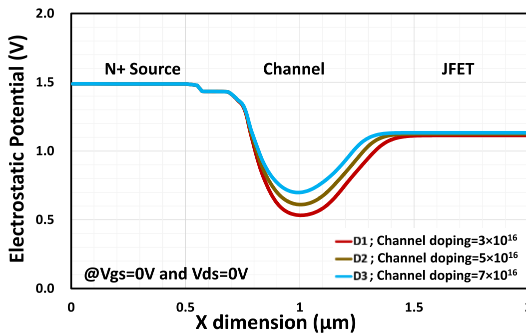


FIGURE 9. Simulated electrostatic potential at channel region of MOSFETs with various channel doping.

the channel is adjusted depending on P contact resistance, resulting in the change of electron conduction.

Fig. 9 shows simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region of MOSFETs with various channel doping. It can be seen that built-in potential between channel and JFET decreases for the operation of third quadrant when the channel doping increases. Moreover, the width of potential barrier decreases with the increase of the channel doping. It clearly shows there is trade-off relationship between third quadrant mode and blocking mode.

Fig. 10 (a) shows measured output characteristics of MOSFETs with channel doping of 7×10^{16} cm^{-3} at different temperatures. At room temperature, MOSFETs provide better conduction behaviors. This is because operation at high temperature results in a reduction in the mobility, reducing the overall current conduction between drain and source. Fig. 10 (b) summarizes experimental $R_{on,sp}$ at different temperatures and channel doping concentrations. Regardless of

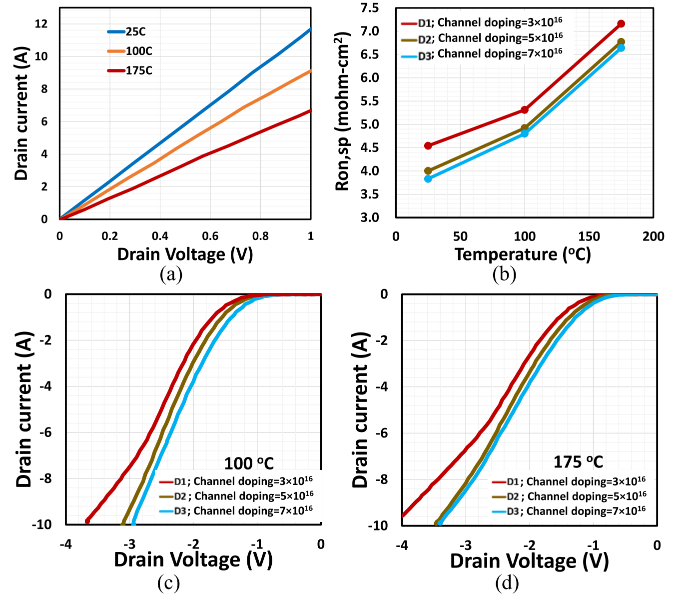


FIGURE 10. (a) Measured output characteristics of MOSFETs with channel doping of 7×10^{16} cm^{-3} at different temperatures, (b) summary of experimental $R_{on,sp}$ at different temperatures, and measured third quadrant behaviors at (c) 100 °C, and (d) 175 °C.

channel doping, $R_{on,sp}$ increase with temperature. Fig. 10 (c) and (d) show measured third quadrant behaviors at 100 °C and 175 °C. The high temperature results in the decrease of knee voltage, but the forward voltage drop increases due to the reduction in the mobility. Regardless of operating temperature, high channel doping provides better third quadrant behaviors.

B. CHANNEL LENGTH

Various L_{ch} (1.0, 0.5, 0.4, and 0.3 μm) were designed to examine the impact of L_{ch} on channel diode behavior. Due to the decrease of channel resistance, shorter L_{ch} provides better conduction behaviors, resulting in lower specific on-resistance ($R_{on,sp}$). For L_{ch} of 0.3, 0.4, 0.5, and 1.0 μm, the resultant $R_{on,sp}$ is 4.02, 4.27, 4.54, and 6.54 mΩ-cm^2, respectively. Transfer characteristics of MOSFETs with different L_{ch} are shown in Fig. 11 (a). For L_{ch} of 0.3, 0.4, 0.5, and 1.0 μm, V_{th} is 1.9, 2.2, 2.5, and 3.4 V, respectively (V_{th} was extracted at V_{ds} of 0.1 V and I_{ds} of 5 mA).

Measured third quadrant behaviors of MOSFETs with different L_{ch} are shown in Fig. 11 (b). At power density of 500 W/cm^2, D1, D5, and D6 operate in the unipolar mode only using electron current. Shorter L_{ch} provides the low knee voltage, resulting in better conduction behaviors. This is because shorter L_{ch} forms thinner and lower potential barrier in the channel region. In contrast to shorter L_{ch}, D4 turns on body diode from −2.7 V. It is observed that due to unoptimized contact resistance of P+, the current slope is reduced when the operation of the body diode begins [12]; Fig. 11 (b).

Fig. 11 (c) shows measured forward blocking mode of MOSFETs with various L_{ch}. Shorter L_{ch} (D5 and D6) has

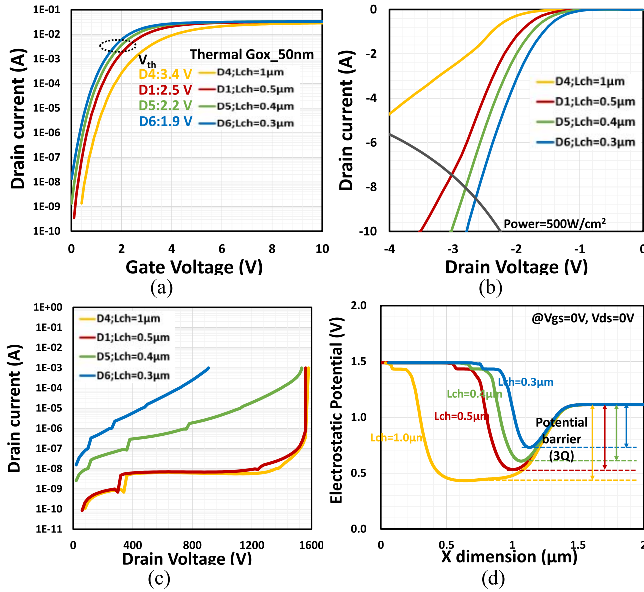


FIGURE 11. **(a) Measured transfer characteristics, (b) third quadrant behaviors, (c) forward blocking mode at V_{gs} of 0 V, and (d) simulated electrostatic potential at channel region of MOSFETs with various channel lengths.**

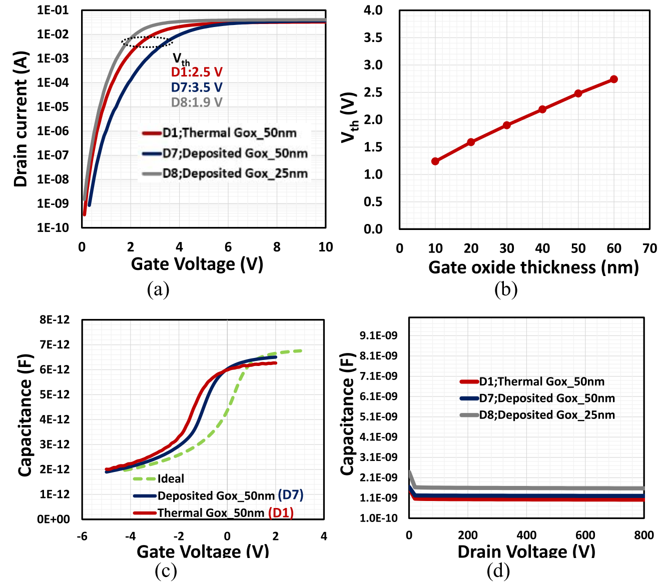


FIGURE 12. **(a) Measured transfer characteristics of MOSFETs with different gate oxides, (b) simulated V_{th} of MOSFETs with thermal gate oxide of 50nm, (c) measured capacitance-voltage (C-V) characteristics of MOS capacitor with different gate oxides, and (d) measured input capacitances of MOSFETs with different gate oxides.**

high leakage current and low breakdown voltage under blocking behaviors. Due to low channel potential, leakage current flows through the channel under high drain voltage, reaching high leakage current before avalanche breakdown occurs. However, D1 and D4 provide high breakdown voltage with low leakage current, since L_{ch} of $> 0.5\ \mu m$ forms a sufficiently high channel potential that suppresses current conduction in the channel under high drain voltage. When the potential barrier in the channel supports high voltage, breakdown voltage is then governed by avalanche phenomenon at the end of the P-well region or edge termination, not leakage current.

Simulated electrostatic potential at the channel region of MOSFETs with different L_{ch} is shown in Fig. 11 (d). In the same manner of channel doping, L_{ch} shows trade-off relationship between barrier for third quadrant and blocking mode. However, the potential between N+ source and channel for blocking mode is affected by not only barrier height, but also barrier thickness. Long L_{ch} provides thicker and higher potential barrier, providing low leakage current under blocking mode. For the improvement of trade-off relationship between third quadrant and blocking mode, an appropriate channel length (e.g., D1) is required to operate MOSFETs that utilize the channel diode.

C. GATE OXIDE

For the optimization of channel potential, MOSFETs with different thicknesses and types of gate oxide were fabricated. Different gate voltages were applied with different thicknesses of gate oxide; 50 nm (20 V) and 25 nm (12 V). Regardless of the gate oxide condition, conduction behaviors are almost identical. For D1, D7, and D8, the resultant $R_{on,sp}$ is 4.54, 4.73, and 4.57 mΩ-cm^2, respectively.

Transfer characteristics of MOSFETs with different gate oxides are shown in Fig. 12 (a). D8 shows a reduced V_{th} because of the increased specific oxide capacitance (C_{ox}). Fig. 12 (b) shows simulated V_{th} of MOSFETs with thermal gate oxide of 50nm. It shows that V_{th} increases with gate oxide thickness. D1 has lower V_{th} when compared with D7 which might be originated from larger positive fixed charge. Fig. 12 (c) shows capacitance–voltage (C–V) characteristics of MOS capacitor with different gate oxides. It is shown that thermal gate oxide was more shifted in C-V measurement due to larger positive fixed charge. The measured D_{it} for thermal and deposited gate oxide at E_C-E of 0.125 eV is approximately 4×10^{11} cm^{-2}eV^{-1} and 3×10^{11} cm^{-2}eV^{-1}, respectively. Fig. 12 (d) shows measured input capacitances of MOSFETs with different gate oxides. Since input capacitances are largely affected by gate oxide thickness, a gate oxide thickness of 25 nm causes higher input capacitances when compared with MOSFETs with a gate oxide thickness of 50 nm.

Fig. 13 (a) shows measured third quadrant behaviors of the fabricated 4H-SiC MOSFETs with different gate oxides. Different gate oxides provide different third quadrant behavior, when accounting for the same channel doping and L_{ch} conditions across MOSFETs. The difference of third quadrant conduction behavior originates from the potential barrier in the channel region. D1 has low knee voltage due to larger fixed charge, resulting in the decrease in the channel potential. Although different gate oxides produce different knee voltages under third quadrant behaviors, blocking behavior

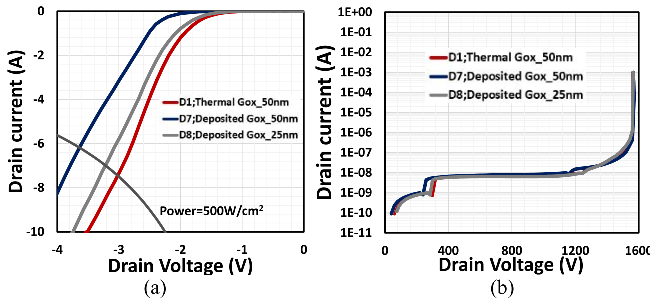


FIGURE 13. (a) Measured third quadrant behaviors and (b) forward blocking mode at V_{gs} of 0 V of MOSFETs with L_{ch} of 0.5 μm with different gate oxides.

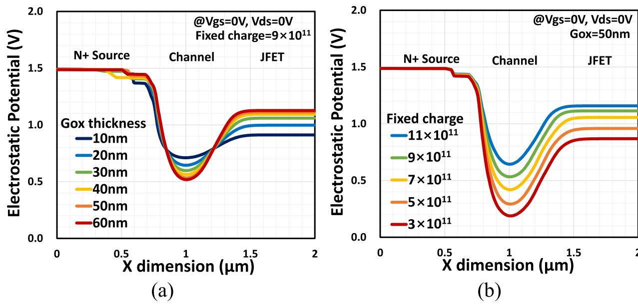


FIGURE 14. Simulated electrostatic potential at channel region of MOSFETs with (a) different gate oxide thickness, (b) different fixed charge in gate oxide.

remains identical as shown in Fig. 13 (b). This is because despite D1 having the lowest knee voltage, these MOSFETs still maintain a high enough channel potential to block high drain voltage (>1.5 kV).

In order to clarify channel potential, Sentaurus 2D TCAD simulation was conducted. The thinner gate oxides result in lower channel potential, as shown in Fig. 14 (a). However, in contrast to channel length and doping variations, thinner gate oxide maintains the width of the potential barrier. As a result, the reduced thickness of gate oxide can improve the trade-off relationship between 3Q conduction and blocking behaviors. Moreover, fixed charge in the gate oxide determines the change in the channel potential, as shown in Fig. 14 (b). A larger fixed charge causes low potential barrier. The fixed charge found within the gate oxide differs depending on the process or recipe used to form it. In this case, thermal gate oxide possesses a larger fixed charge when compared with deposited gate oxide, and as a result has a lower channel potential barrier, providing better conduction behavior under third quadrant mode.

Fig. 15 compares various approaches discussed earlier with respect to simulated channel potentials in the blocking mode and 3Q mode of operations. Fig. 16 plots the blocking potential barrier divided by potential barrier for the 3Q operation. It is clearly discovered that the gate oxide thickness serves as effective knob to control the blocking channel potential keeping smaller change in the channel potential during 3Q operation. In other words, the change of

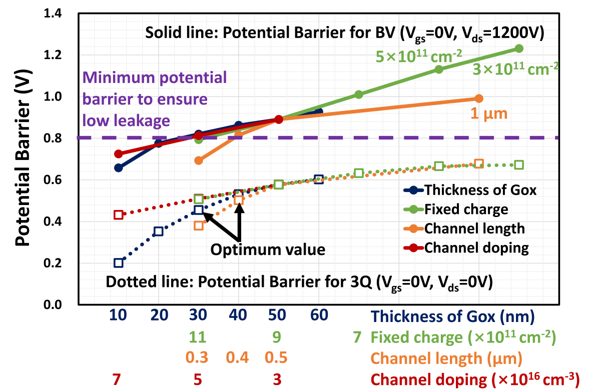


FIGURE 15. Summary of the simulated channel potential for 3Q and blocking behaviors.

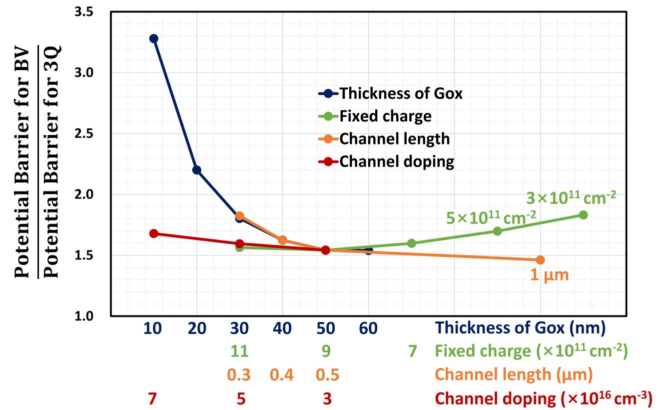


FIGURE 16. Summary of the plot when potential barrier of BV divided by potential barrier of 3Q.

gate oxide and channel length have better trade-off relationship between 3Q and blocking behaviors. Moreover, the change of gate oxide thickness is the better way to improve the trade-off relationship as the width of potential barrier is identical regardless of the thickness. However, it should be noted that a certain level of the blocking channel potential should be maintained to suppress the leakage current (The channel potential for BV of > ∼0.8 V is required to obtain high BV with the low leakage current; The channel potential value of 0.8 V is selected to ensure the leakage current does not exceed 100 μA at 1200 V.).

V. RESULTS AND DISCUSSION: DYNAMIC CHARACTERISTICS

A. REVERSE RECOVERY CHARACTERISTICS

Fig. 17 (a) shows the simulated test circuit for the reverse recovery characteristics. MOSFET 'B' in Fig. 17 (a) is used as a freewheeling diode to evaluate the reverse recovery characteristics. Fig. 17 (b) shows the simulated reverse recovery characteristics of MOSFETs with different channel lengths. MOSFETs with short channel provide a small reverse recovery charge (Q_{RR}); For L_{ch} of 0.3 μm, 0.5 μm, and 1.0 μm,

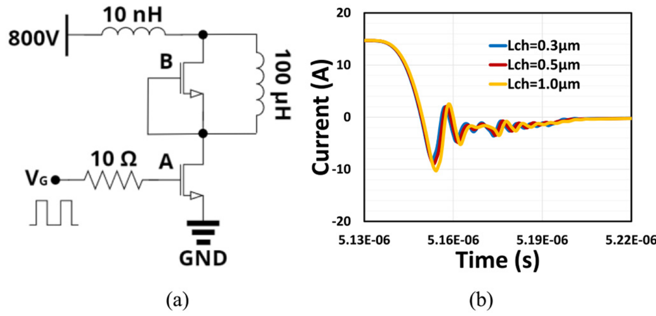


FIGURE 17. (a) Test circuit for reverse recovery characteristics and (b) simulated reverse recovery characteristics of MOSFETs with different channel lengths.

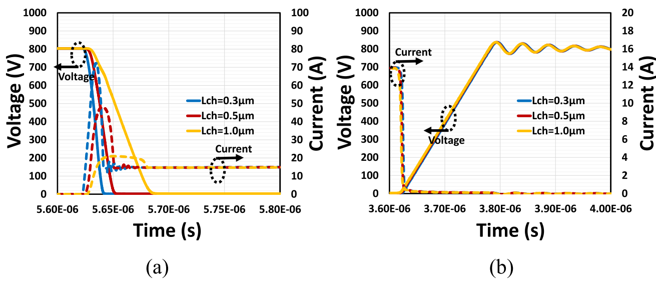


FIGURE 18. Simulated switching waveforms of MOSFETs with different channel lengths in (a) turn-on and (b) turn-off.

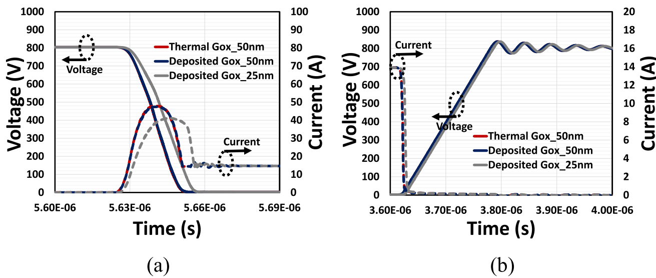


FIGURE 19. Simulated switching waveforms of MOSFETs with different gate oxides in (a) turn-on and (b) turn-off.

Q_{RR} of 0.97 μC/cm^2, 1.06 μC/cm^2, and 1.24 μC/cm^2 were extracted, respectively. MOSFETs with the low knee voltage under third quadrant behaviors offer a small Q_{RR}.

B. SWITCHING CHARACTERISTICS

Fig. 18 (a) and (b) show simulated switching waveforms of MOSFETs with different channel lengths in turn-on and turn-off, respectively. The MOSFETs with L_{ch} of 0.3 μm have the fastest turn-on switching transient due to the largest transconductance [13]. For L_{ch} of 0.3 μm, 0.5 μm, and 1.0 μm, energy loss for turn-on transient of 173 μJ, 298 μJ, and 335 μJ were calculated as shown in Table 3. The switching energy for turn-on transient is calculated at 10% V_{gs} to 10% V_{ds}. The energy loss for turn-off transient is almost identical regardless of channel length.

Fig. 19 shows simulated switching waveforms of MOSFETs with different gate oxides. The MOSFETs with

TABLE 3. Summary of experimental and simulated results.

	D1	D2	D3	D4	D5	D6	D7	D8
$R_{on,sp}$ [mΩ-cm^2]	4.54	4.00	3.83	6.54	4.27	4.02	4.73	4.57
V_{th} [V]	2.5	2.2	1.7	3.4	2.2	1.9	3.5	1.9
BV [kV]	1.56	1.42	1.24	1.58	1.53	0.91	1.56	1.56
$I_{leakage}$	9.2 nA	37 μA	0.5 mA	5.7 nA	19 μA	N/A	14.8 nA	8.4 nA
$-V_F$ [V]	3.51	3.21	2.92	5.9	3.02	2.78	4.26	3.74
Q_{RR} [μC/cm^2]	1.06	-	-	1.24	-	0.97	-	-
Eon [μJ]	298	-	-	335	-	173	299	305
Eoff [μJ]	32.7	-	-	32.3	-	33.2	32.6	34.8

*$R_{on,sp}$ was extracted at V_{gs} of 20V (12V for 25nm) and V_{ds} of 0.1V.
V_{th} was extracted at V_{ds} of 0.1V and I_{ds} of 5mA.
BV was extracted at I_{ds} of 1mA.
$I_{leakage}$ was extracted at V_{ds} of 1200V.
V_F was extracted at Ids of -10A.
E_{on} was extracted at 10% V_{gs} to 10% V_{ds}.
E_{off} was extracted at 90% V_{gs} to 90% V_{ds}.

gate oxide of 25 nm have a slow turn-on switching transient due to the large C_{ISS}. However, energy loss for turn-on transient was almost identical; For thermal 50 nm, deposited 50 nm, and deposited 25 nm, energy loss for turn-on transient of 298 μJ, 299 μJ, and 305 μJ were calculated as shown in Table 3. This is because a small inrush current compensates for the slow switching speed in MOSFETs with 25 nm. The energy loss for turn-off transient is also almost identical regardless of gate oxide; For thermal 50 nm, deposited 50 nm, and deposited 25 nm, 32.7 μJ, 32.6 μJ, and 34.8 μJ were extracted as shown in Table 3.

Table 3 summaries the experimental and simulated results. It turns out that short channel length improves switching characteristics as well as reverse recovery characteristics. However, MOSFETs with thin gate oxide cause increased input capacitance, resulting in a slow switching speed. The optimum way for channel diode is the optimization of channel length by reducing the channel length.

VI. CONCLUSION

1.2 kV SiC MOSFETs achieving a low knee voltage, as well as low forward voltage drop, under third quadrant mode of operation are proposed and experimentally demonstrated. This paper provides MOSFET designers with a more manageable fabrication process by removing the regrowth process. Also, the optimization of channel potential was investigated in terms of trade-off between blocking mode and third quadrant behaviors. The reduced L_{ch} or increased channel doping results in the reduction in channel potential, contributing to the decrease of knee voltage under third quadrant mode. Moreover, shorter L_{ch} or increased channel doping provide low $R_{on,sp}$ due to low channel resistance or JFET resistance. Too shorter L_{ch} and high channel doping result in low breakdown voltage due to high leakage current from channel, but L_{ch} of 0.5 μm (channel doping of 3×10^{16} cm^{-3}) have high breakdown voltage with extremely low leakage current. The effect of thickness and

fixed charge of gate oxide for channel potential was also discussed. It is demonstrated thinner thickness and larger fixed charge provide better third quadrant behaviors due to the low channel potential. 1.2kV MOSFETs with channel diode are successfully fabricated using the optimization of channel doping, L_{ch}, and gate oxide. Moreover, the simulated reverse recovery characteristics and switching characteristics are discussed. MOSFETs with short channel length improve not only reverse recovery characteristics but also switching characteristics. Consequently, the optimized 4H-SiC MOSFETs with channel diode are a promising and suitable power semiconductor device for power electronics.

ACKNOWLEDGMENT

The authors would like to thank Department of Energy (DOE) for supporting this project. The authors acknowledge the fabrication of the devices by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA., and SEM images by Alexander Bialy in metrology department at SUNY Polytechnic Institute.

REFERENCES

[1] X. Jiang *et al.*, "Investigation on degradation of SiC MOSFET under surge current stress of body diode," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 77–89, Mar. 2020, doi: 10.1109/JESTPE.2019.2952214.

[2] W. Sung and B. J. Baliga, "On developing one-chip integration of 1.2 kV SiC MOSFET and JBS diode (JBSFET)," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8206–8212, Oct. 2017, doi: 10.1109/TIE.2017.2696515

[3] F.-J. Hsu *et al.*, "High efficiency high reliability SiC MOSFET with monolithically integrated Schottky rectifier," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, May/Jun. 2017, pp. 45–48, doi: 10.23919/ISPSD.2017.7988889.

[4] S. Hino *et al.*, "Demonstration of SiC-MOSFET embedding Schottky barrier diode for inactivation of parasitic body diode," *Mater. Sci. Forum*, vol. 897, pp. 477–482, May 2017. [Online]. Available: https://doi.org/10.4028/www.scientific.net/MSF.897.477

[5] M. Uchida *et al.*, "Novel SiC power MOSFET with integrated unipolar internal inverse MOS-channel diode," in *Proc. Int. Electron Devices Meeting (IEDE)*, Dec. 2011, pp. 1–4, doi: 10.1109/IEDM.2011.6131620.

[6] W. Sung, K. Han, and B. J. Baliga, "A comparative study of channel designs for SiC MOSFETs: Accumulation mode channel vs. inversion mode channel," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, May/Jun. 2017, pp. 375–378, doi: 10.23919/ISPSD.2017.7988996.

[7] *SentaurusTM Process User Guide, Ver. K-2015.06*, Synopsys Inc., Mountain View, CA, USA, Jun. 2015.

[8] N. Yun *et al.*, "Developing 13-kV 4H-SiC MOSFETs: Significance of implant straggle, channel design, and MOS process on static performance," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4346–4353, Oct. 2020, doi: 10.1109/TED.2020.3017150.

[9] D. Kim, N. Yun, S. Y. Jang, A. J. Morgan, and W. Sung, "An inclusive structural analysis on the design of 1.2kV 4H-SiC planar MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 804–812, 2021, doi: 10.1109/JEDS.2021.3109605.

[10] "Cree 1200V Product C2M0080120D, Rev. D." Sep. 2019. [Online]. Available: www.wolfspeed.com

[11] Onsemi 1200V Product NTH4L080N120SC1, Rev.2." May 2022. [Online]. Available: www.onsemi.com

[12] K. Han and B. J. Baliga, "Comprehensive physics of third quadrant characteristics for accumulation- and inversion-channel 1.2-kV 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3916–3921, Sep. 2019, doi: 10.1109/TED.2019.2929733.

[13] K. Han, A. Kanale, B. J. Baliga, and S. Bhattacharya, "Static, dynamic, and short-circuit performance of 1.2 KV 4H-SiC MOSFETs with various channel lengths," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 47–52, doi: 10.1109/WiPDA46397.2019.8998803.