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Investigation of SiGe/Si Bilayer Inverted-T Channel Gate-All-Around Field-Effect-Transistor With Self-Induced Ferroelectric Ge Doped HfO_2

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ABSTRACT We investigated the ferroelectric properties of self-induced $HfGeO_x$ in a HfO_2 film deposited on a SiGe substrate and analyzed a novel ferroelectric inverted T channel gate-all-around (IT-GAA) with a Si/SiGe bilayer channel and self-induced ferroelectric Hf germanate. The proposed ferroelectric IT-GAAFET with short-channel (gate length = 60 nm) exhibited a steep average subthreshold slope of 53 mV/dec, a drain-induced barrier lowering of only 1.7 mV/V, and a high on-off current ratio of 1.7×10^7. The proposed ferroelectric IT-GAA field-effect transistor can be a candidate for the sub-N3 technology node and ultralow-power, high-performance applications.

INDEX TERMS ITFET, GAAFET, Hf-germanate, negative capacitance (NC), ferroelectric, short channel effect (SCE).

I. INTRODUCTION

Recently, Gate-all-around field-effect transistors (GAAFETs), including those with nanosheet [1]–[3] and nanowire [4]–[6] channel structures, are promising candidates to replace FinFETs in the sub-N3 technology node because of their excellent electrostatic characteristics (especially their short-channel effects (SCEs)). Inverted T (IT) channel FETs, which have ultra-thin vertical and horizontal body channels, have been proposed as an alternative to FinFETs [7], [8]. Although they are fabricated on silicon-on-insulator (SOI) wafers, leakage currents can still degrade the OFF-state electrical properties because of weak inversion in the ungated part of the channel. We proposed a novel channel structure for GAAFETs in which the IT channel is suspended, and the gate metal is wrapped around the channel. The multi-corner concave polygonal IT channel provides excellent gate control, and the suspended channel resolves the leakage problem. On the other hand, the ferroelectric FETs that use HfO_2-based ferroelectric films (mostly $Hf_{0.5}Zr_{0.5}O_2$) as the gate oxide, which achieve a subthreshold swing (SS) of less than 60 mV/dec because of the negative capacitance (NC) effect [9]–[11], have been addressed promising for ultra-low power consumption applications [11]. It had been reported that incorporating cation dopants such as Zr, Si, Ge, La, or Y a HfO_2 would be possible to possess ferroelectricity [12]. A study explored a self-induced Ge-doped ferroelectric HfO_2 process with a $TiN/Al_2O_3/HfO_2/Ge$ gate stack to spontaneously form a crystallized Hf germanate ($HfGeO_x$) by doping Ge atom from Ge substrate in thermal processes [13]. Similarly, germanate may form along with the HfO_2 films deposited on SiGe substrates [14]. Hence, in this study, we first investigated the self-induced Ge-doped process of the HfO_2 films deposited on the SiGe substrate and its ferroelectricity by using grazing incidence X-ray diffraction (GI-XRD), X-ray photoelectron spectroscopy (XPS), and P–V characteristics. During the thermal process for doping the Ge atom into the HfO_2 film, the Ge desorption would happen in the form of GeO gas. Reference [13] To ensure the Ge desorption could let the Ge atom stay in the HfO2 film and do not

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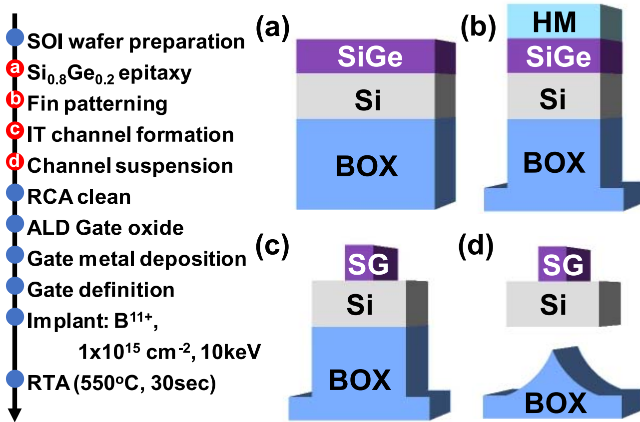

FIGURE 1. IT-GAAFET fabrication process flow. (a) Epitaxial SiGe growth. (b) Fin patterning and overetching of buried oxide. (c) Selective isotropic etching of SiGe. (d) Wet etching of buried oxide.

further diffuse into the gate metal, the same gate stack as [13] of TaN/Al_2O_3/HfO2 is adopted, inserting a layer of Al_2O_3 as a blocking layer. Afterward, we demonstrate the ferroelectric IT-GAAFET by selectively etching on SiGe/Si bilayer channel and implementing a self-induced Ge-doped ferroelectric HfO_2 process. Our results reveal the proposed device has well suppression on the SCEs and exhibits extremely steep SS_{avg}.

II. DEVICE FABRICATION

Fig. 1 presents the fabrication of the ferroelectric IT-GAAFET and the critical steps. First, the monocrystalline Si layer of an 8-in p-type SOI wafer is thinned to 20 nm, and a 15-nm-thick epitaxial $Si_{0.8}Ge_{0.2}$ layer is grown (Fig. 1(a)). Next, the active region with a 40-nm-wide channel mask is defined through e-beam lithography (EBL), and the pattern is transferred using anisotropic reactive ion etching (RIE) with slight over-etching to buried oxide (Fig. 1b). Before the hard mask is stripped, the SiGe layer is selectively shrunk using isotropic wet etching [15], [16] to form the IT channel (Fig. 1(c)). Afterward, the channel is suspended in an HF solution (Fig. 1(d)). After RCA cleaning, a stack of 4-nm-thick HfO_2 and 2-nm-thick Al_2O_3 is deposited as the gate dielectric oxide layer through atomic layer deposition (ALD). Then, a 120-nm TaN gate metal is deposited through sputtering, followed by gate patterning through EBL and RIE. Subsequently, the source and drain regions are self-aligned Boron implanted with Boron at a dosage of 1×10^{15} cm^{-2} and energy of 10 keV. In the final step, dopant activation and gate oxide crystallization are achieved simultaneously through rapid thermal annealing (RTA) at 550 °C for 30 s in ambient nitrogen. Fig. 2(a) presents a transmission electron microscopy (TEM) image of the fabricated ferroelectric IT-GAAFET. The IT channel has a bilayer structure consisting of the SiGe upper-layer and Si lower-layer. The SiGe upper-layer has a width of 17.3 nm and a height of 14.2 nm; the Si lower-layer has a width of 41.7 nm and a height of 18.1 nm. Fig. 2 (b) presents an

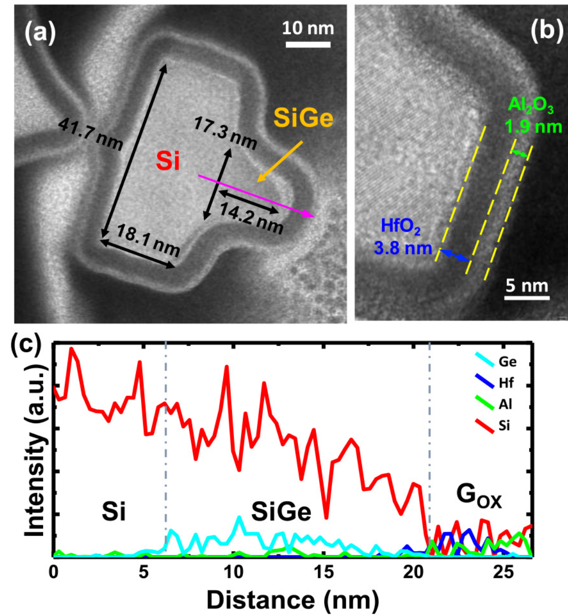

FIGURE 2. (a) TEM image of ferroelectric IT-GAAFET with an upper layer width of 17.3 nm and lower layer width of 41.7 nm. (b) TEM image of gate stack. (c) Energy-dispersive X-ray spectroscopy line scan of scanning line in (a).

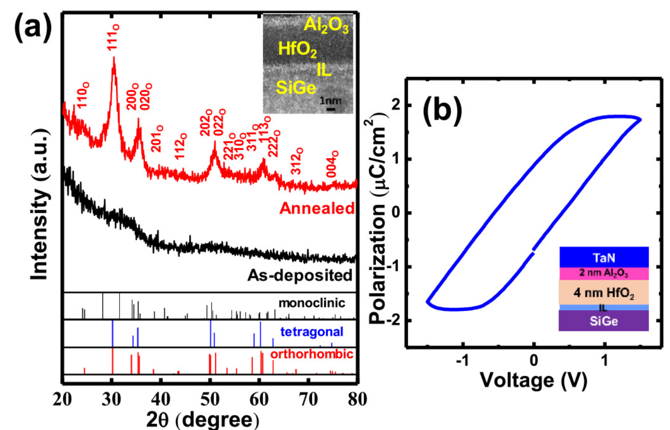

FIGURE 3. (a) GI-XRD spectra of Al_2O_3/HfO_2/SiGe gate stack indicating an orthorhombic phase after annealing. (b) P–V characteristic measured on a TaN/2-nm Al_2O_3/4-nm HfO_2/SiGe MIS capacitor.

enlarged TEM image of the gate oxide. Fig. 2 (c) shows the energy-dispersive X-ray spectroscopy (EDS) line scan at the cut-line in Fig. 2(a), revealing the element composition of the bilayer IT channel and the gate oxide.

III. RESULTS AND DISCUSSION

The crystallinity and the polarization were examined to identify the ferroelectric properties of the TaN/Al2O3/HfO2/SiGe gate stack for ferroelectric IT-GAAFET, as shown in Fig. 3. Fig. 3(a) shows the GI-XRD results of the Al_2O_3/HfO_2/SiGe gate stack; the structure is also demonstrated in the inset cross-sectional TEM image. The spectrum exhibits identical peaks as an orthorhombic phase (o-phase) with space group $Pbc2_1$ does after the sample was annealed. Fig. 3(b and inset) show the P-V of the metal-insulator-semiconductor (MIS)

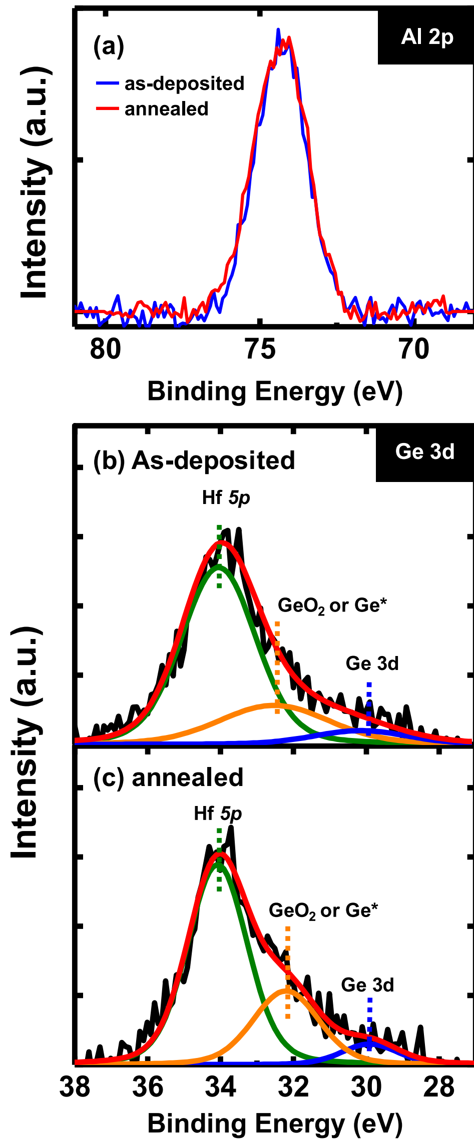

FIGURE 4. (a) Al *2p* core-level spectra of the as-deposited and annealed Al_2O_3/HfO_2/SiGe stacks. Ge *3d* core-level spectra of the (a) as-deposited and (b) annealed Al_2O_3/HfO_2/SiGe stacks after stripping off the Al_2O_3 layer by Ar^+ ion bombardment.

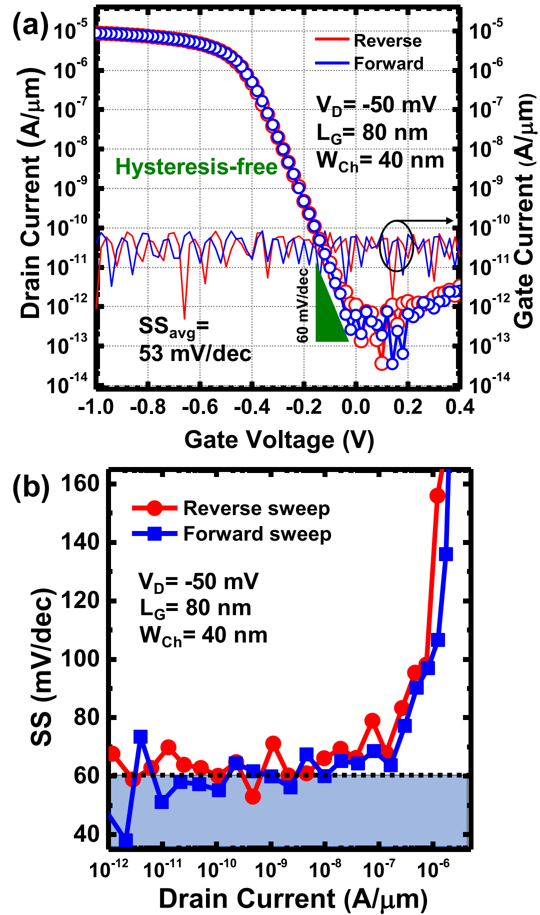

FIGURE 5. (a) Doubly swept I_D-V_G and I_G-V_G curves of ferroelectric IT-GAAFET with W_{Ch}/L_G = 40 nm/ 80 nm at V_D = −50 mV and (b) SS versus I_D.

capacitor and the schematic of the capacitor. A hysteresis P-V curve with two remanent polarization (2Pr) values of approximately 1.5 μC/cm^2 was observed in the MIS capacitor. The detected polarization characteristic in the HfO2-based capacitor was attributed to the non-centrosymmetric o-phase, as shown in Fig. 3(a) [17].

To determine which element was incorporated into the HfO_2 and dominated the transition into o-phase, the chemical bonding states of the Al_2O_3/HfO_2/SiGe gate stack (same sample as that used in GI-XRD analysis) were investigated through XPS measurement. The XPS results were calibrated by fixing the C 1S peak at binding energy (BE) of 284.8 eV to compensate for the charge-induced energy shift due to X-ray exposure [18]. Fig. 4(a) shows the Al *2p* core-level spectra with both as-deposited and annealed Al_2O_3/HfO_2/SiGe gate stack samples. There is no peak shift of the Al *2p* spectrum after the sample was annealed, concluding that no further binding of Al was formed with other elements after annealing. As a result, Al has no attribution to the o-phase stabilization of HfO_2. Furthermore, an Ar^+ ion bombardment was applied on the stack to strip off the upper Al_2O_3 layer for focusing the subsequent XPS investigation in the ferroelectric HfO_2. Fig. 4(b) and 4(c) show the Ge *3d* core-level spectra with as-deposited and annealed stacks after stripping off the Al_2O_3 layer. The peaks at binding energies of approximately 30 and 34 eV were attributed to the Ge atom from the SiGe substrate and Hf *5p* from the HfO_2, respectively [19]. The peak intensity of the Ge-oxide bond state (orange line) increased and slightly shifted to the right shift after annealing, indicating that more Hf-germanate formed because it has a binding energy of 0.45 eV less than that of GeO_2 [20]. Ge desorption occurred during the RTA process, and the Ge bonded to HfO_2, forming $HfGeO_x$. The Ge stabilized the transition of the HfO_2 into the ferroelectric o-phase.

Fig. 5(a) shows transfer drain current (I_D)-gate voltage (V_G) curves, including both forward and reverse sweeps of

the ferroelectric IT-GAAFET with a gate length (L_G) of 80 nm and channel width (W_{Ch}) of 40 nm at drain voltage $V_D = -0.05$ V; I_D was normalized using the top footprint of 40 nm. All electrical characteristics were determined using Keithley 4200A at room temperature. The IT-GAAFET exhibited a steep SS in a wide range of drain currents and was free from hysteresis. The average SS calculated by one devade of I_D increasing had a minimum of 53 mV/dec. The gate current (I_G) is also presented in Fig. 5(a). I_G shows near the measure limitation under the entire measuring range, including forward and reverse sweeps. Fig. 5(b) presents the SS versus I_D, where SS was extracted from every adjacent measured point. The device exhibited an SS of less than 60 mV/dec (the Boltzmann limitation at room temperature) throughout the entire subthreshold region (I_D of less than 10^{-7} A/μm). The sub-60 mV/dec SS value was attributed to the NC effect resulting from the ferroelectric Ge:HfO_2 gate capacitance.

Because of the fabrication process, only the HfO_2 that covering the SiGe upper-layer of the IT channel exhibited ferroelectricity. Even that, the ferroelectric IT-GAAFET still shows an outstanding subthreshold characteristic. In previous studies of hysteresis-free NC devices, sub-60 SS only exists in a few measured points or a small range of I_D [9]–[11]. Because only when the NC effect happens in the weak inversion region would the arising surface-potential amplification dramatically decrease SS [21]. However, in this study, the concave polygonal IT channel with eight corners provided excellent gate control ability because of the high electric field at the corners [7], which dominated the SS when surface potential amplification was not significant.

Fig. 6 shows the I_D-V_G characteristics of a short channel ferroelectric IT-GAAFET with $L_G = 60$ nm and $W_{Ch} = 40$ nm at various drain voltages (V_D) and the corresponding I_D-V_D curves. The device exhibited SS_{avg} of 59.1 mV/dec, V_T of -0.29 V, drain-induced barrier lowering (DIBL) of 1.7 mV/V, on current (I_{ON}) of 65.5 μA/μm, and on-off current ratio (I_{ON}/I_{OFF}) of 1.7×10^7. I_{ON} is extracted at $V_D = -1$ V and over-drive voltage ($V_{OV} = V_G - V_T$) = -0.5 V; I_{OFF} was extracted at $V_D = -1$ V and $V_G = 0$ V. The results indicate that the IT-GAA channel can suppress SCEs and has adequate output.

Fig. 7 shows the TCAD simulation of Si/SiGe bilayer IT-GAAFET. The hole current density at $V_D = -0.1$ V and $V_G = -1$ V reveals that the SiGe upper-layer conducts a higher current density than the Si lower-layer. After integrating the current density of the two layers of the channel, we found that the two layers have almost equal contributions to the total current even though the SiGe upper-layer has a smaller cross-sectional area. The phenomenon is due to the SiGe upper-layer acting like a quantum well that confines the hole carrier. Since the SiGe upper-layer has a smaller dimension than the Si lower-layer and there is also a valence band energy offset at the Si/SiGe interface. The simulation result also explains why even though only the HfO_2 covering the SiGe upper-layer could exhibit ferroelectricity, the overall characteristic still presents a steep SS_{avg} of 53 mV/dec.

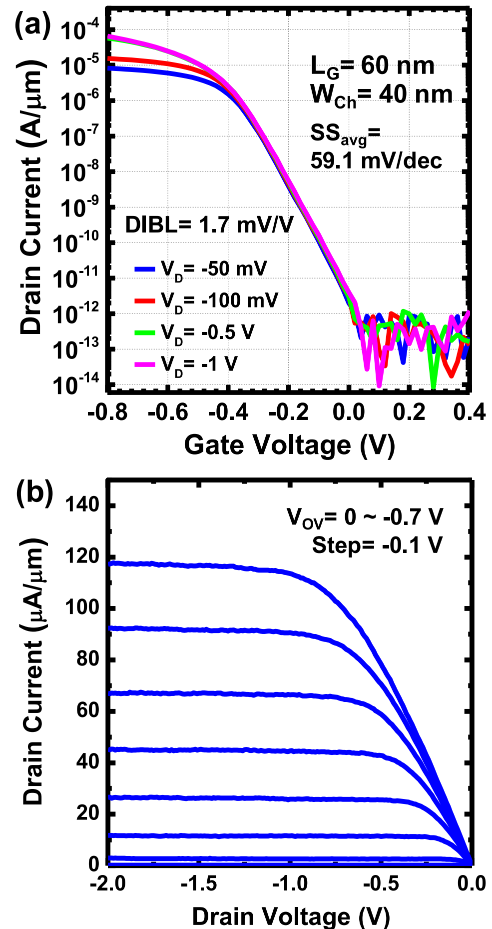

FIGURE 6. (a) I_D-V_G curves of ferroelectric IT-GAAFET with W_{Ch}/L_G = 40 nm/60 nm at $V_D = -50$ mV, -100 mV, -0.5 V, and -1 V. (b) I_D-V_D curves at $V_{OV} = 0 \sim -0.7$ V.

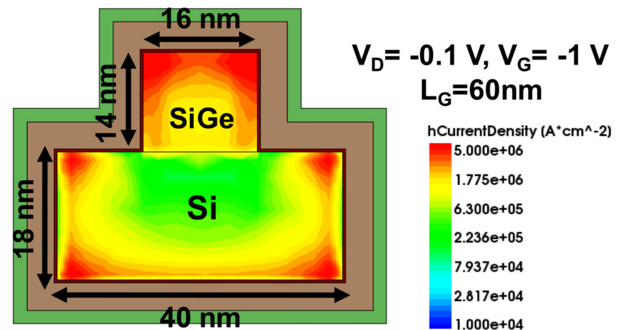

FIGURE 7. TCAD simulation plot of hole current density in the channel of SiGe/Si bilayer IT-GAAFET at $V_D = -0.1$ V and $V_G = -1$ V.

TABLE 1. Key device characteristics comparison with previous GAAFET studies.

	This work	SiGe GAAFET [4]	Si GAAFET [5]	Ge GAAFET [6]
Channel structure	Inverted-T	nanosheet	rectangular nanowire	circular nanowire
Channel material	$Si_{0.8}Ge_{0.2}$(upper) +Si(lower)	$Si_{0.4}Ge_{0.6}$	Si	Ge
Channel dimension (nm×nm)	16×14(upper) + 40×18(lower)	100×5	15×11	diameter = 9(nm)
L_G (nm)	60	55	70	40
I_{ON}/I_{OFF}	1.7×10^7 @V_D=-1V	~9×10^6 @V_D=-0.5V	~6×10^8 @V_D=-0.7V	~1×10^5 @V_D=-0.5V
SS_{lin} (mV/dec)	59.1	65	60	75.1
SS_{sat} (mV/dec)	60	67	60	81
DIBL (mV/V)	free	free	~25	27

Table 1 summarizes the comparison of several key characteristics with the previous GAAFET studies. Compared to other GAAFETs with a close L_G, the proposed SiGe/Si bilayer IT-GAAFET shows lower DIBL, SS, and high I_{ON}/I_{OFF} even with a larger channel dimension. It is possible to further lower the I_{OFF} by scaling the channel dimension, implying that the proposed ferroelectric IT-GAAFET is highly potential for the low-power-consumption application.

IV. CONCLUSION

In this study, we have studied the ferroelectric properties of crystallized $HfGeO_x$ formed in the interface between HfO_2 and SiGe substrate; and demonstrated the Si/SiGe bilayer channel ferroelectric IT-GAAFET using the self-induced ferroelectric $HfGeO_x$. Due to the high current contribution of SiGe upper-layer and the NC effect brought from the self-induced ferroelectric $HfGeO_x$, a steep SS throughout the whole subthreshold region is introduced. With the help of IT structure, the SCEs are well suppressed. Compared with previous GAAFET studies, our work presents outstanding DIBL and SS even with a larger channel dimension, indicating the device is very potential and competitive. Also, the device is highly compatible with today's CMOS process and suitable for future high-performance and ultra-low power consumption applications.

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