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Model Implementation of Lorentzian Spectra for Circuit Noise Simulations in the Frequency Domain

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ABSTRACT This work presents a new method for the Verilog-A implementation of Lorentzian noise models, in a module called *VERILOR*, which can automatically generate either Lorentzian or 1/f-like noise spectra depending on the trap density and gate oxide area, for all bias conditions, in a one-step simulation. Based on statistical experimental data, we demonstrate the importance of Lorentzian noise modeling in contrast to classic frequency domain 1/f or time domain Random Telegraph Noise (RTN) modeling, in terms of PSD, total noise power, and device-to-device noise variability reproduction. Moreover, we validate the applicability of *VERILOR* in circuit simulators in both frequency and time domain, and how it can enable precise noise variability studies at a circuit level. Finally, fundamental digital and analog circuits such as the Ring Oscillator are used to showcase the usefulness and applicability of the *VERILOR* model in circuit noise simulations.

INDEX TERMS Circuit noise, GR noise, Lorentzian noise, low-frequency noise, noise variability, random telegraph noise, Tri-Gate Nanowire MOSFETs, Verilog-A, phase noise.

I. INTRODUCTION

With the incorporation of new materials and architectures, so as devices to keep pace with "More Moore" and "More than Moore" technology roadmaps, the enhancement of defect-related effects such as low frequency noise (LFN) [1], Random Telegraph Noise (RTN) [2] and Bias Temperature Instabilities (BTI) [3] are attracting more attention by the semiconductor device engineers and circuit designers. Apart from the increase of LFN level due to smaller area devices [4], other kinds of LFN, different from the 1/f trend, like Lorentzian spectra [5], have made their appearance due to defects that result from new materials and process techniques [4] or to the non-uniformity of oxide defects. The Lorentzian shape of power spectral density (PSD) may originate either from oxide trap-related RTN signals (leading to 1/f in large area oxides) or defects in the MOSFET channel region leading to the generation-recombination (GR) noise [4], [6]. Regarding the device-based performance, this peculiar LFN behavior has increased by a great extent the LFN variability [1], related to the significant trap number variations from device to device due to small area or GR centers, leading to further limitations in device performance and reliability [7]. Inevitably, these limitations concern the safe operation of a whole circuit, as it has been reported that LFN/RTN has a major impact on both digital and analog circuits [8]–[11]. More specifically, in the case of SRAMs, the presence of RTN limits the minimum supply voltage, V_{dd}, due to V_t shifts.

In addition, studies have shown that depending on the moment that a current jump due to RTN occurs, there might be a delay or even errors in the write operation [8]. Apart from digital circuits, RTN can degrade the accuracy of sensors like in the case of CMOS imagers in which RTN is responsible for the blinking and twinkling pixels in videos under low light conditions [12]. Finally, LFN has attracted the interest from the RF design community, as it can be up-converted to higher frequencies and thus affect the operation of MOSFETs in RF applications [13]. A characteristic example is the case of ring oscillators (RO), in which LFN is up-converted to phase noise around the oscillation frequency [14].

Since it is undoubtable that LFN, and especially RTN, can have severe impact on the reliable and safe operation of

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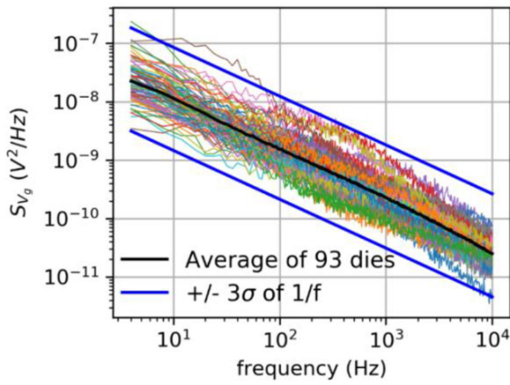

FIGURE 1. Measured input-referred gate voltage noise spectra on TriGate Nanowire MOSFETs, plotted together with the log-mean 1/f$^{\gamma}$ ($\gamma = 0.88$) spectrum and the $+-3\sigma$ 1/f spectra based on the 1/f variability modeling. (W_{eff} = 52 nm, L = 30 nm, |Vg| = 1 V, |Vd| = 30 mV) [16].

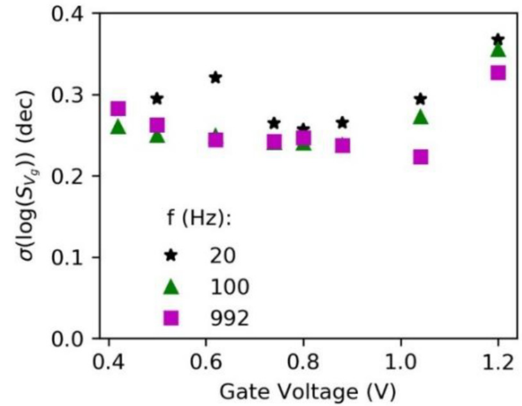

FIGURE 2. Standard deviation value of the input-referred gate voltage noise versus gate voltage for different frequencies: 20, 100, and 992 Hz.

circuits, its accurate modeling is crucial and indispensable. While various works have been presented on the time-domain modeling of the RTN effect for circuit simulators [8], [9], there are very few that concern the modeling of Lorentzian noise sources directly in the frequency domain [15]. The latter could, on one hand, significantly reduce the noise simulation time, and on the other hand enable a direct and accurate simulation of the PSD for circuits, where the noise is important to be studied in the frequency domain such in the case of oscillators or analog signal processing. Moreover, the pre-existing PSD modules in Verilog-A are limited to 1/f, noise data table and white noise, therefore the Lorentzian type of noise needs a dedicated module to be developed.

II. IMPORTANCE OF LORENTZIAN NOISE MODELING

As already mentioned, the miniaturization of the devices increases the probability of the existence of very few traps - in some cases just one- as opposed to large oxide areas where there are hundreds or thousands of defects. In this case the main LFN source stops being 1/f-like and instead appears a Lorentzian-like dependence: plateau at low frequencies and 1/f^2 dependence above a certain cut-off frequency f_c, as described in (1), where $S(0)$ is the plateau at 0 Hz.

$$S(f) = \frac{S(0)}{1 + (f/f_c)^2} \tag{1}$$

In many publications, RTN is modeled in the time domain. The advantage of this method is that the state of a circuit can be accessed at any time and so possible errors due to RTN can be examined. However, concerning variability studies or multiple RTN traps with huge spans of time constants, transient circuit simulations can take very long, while the situation becomes even more difficult when increasing the number of components in the circuit. To overcome time-consuming issues, but also be able to directly perform noise spectrum simulations, the need for RTN modeling in the frequency domain emerges. To do so, the authors of some publications use the LFN variability level, $\sigma(\log(S_{\mathrm{Id}}))$, extracted from experiments or models and add the $+/-3\sigma$ to the 1/f average spectrum [17], [18], in an effort to cover the extreme LFN level variations induced by RTN. By doing this, although the safe design of a circuit in terms of LFN is succeeded, the LFN level itself might be significantly overestimated or underestimated. To underline this phenomenon, we tested this methodology using our experimental data. The presented experimental results are from measurements performed on Tri-Gate Nanowire SOI p-channel FETs, fabricated by CEA-LETI [19]. They consist of a 145 nm thick buried oxide, a Si film of H = 11 nm and a 2 nm Equivalent Oxide Thickness (EOT) HfSiON gate dielectric with TiN metal gate. We show in Fig. 1 a set of 93 experimentally measured input-referred gate voltage noise spectra, S_{Vg}, at $|V_g| = 1$ V, along with the $+/-3\sigma$ limits added to the average 1/f, with $\sigma(\log(S_{\mathrm{Vg}}))$ extracted at 20 Hz. We chose a very small gate area device, $W_{\mathrm{eff}}/L = 52/40$ nm, so as to purposefully increase the noise variability and the probability of RTN traps appearance. The choice of the input-referred gate voltage noise $S_{\mathrm{Vg}} = S_{\mathrm{Id}}/g_m^2$, as opposed to S_{Id}, as a variability metric is to eliminate as much as possible the static parameter variations. As shown in Fig. 1, the $+/-3\sigma$ spectra fail to accurately estimate the maximum and minimum extreme conditions. In addition, when the 1/f is used to predict LFN variability, the frequency at which the standard deviation is extracted is important since, as it is shown in Fig. 2, σ is not necessarily constant with frequency nor gate bias, as this depends on the energy and spatial distribution of traps.

Moreover, for a better estimation of LFN variability, what is even more important than the value of the PSD at a certain frequency, is the total noise power of the fluctuations for each die calculated by integrating the PSD over the whole frequency range, as expressed in (2). For this reason, the probability density function (PDF) of the total noise power for both the experimental and the 1/f data for a bandwidth of 1 kHz has been calculated. The results are shown in Fig. 3.

$$\sigma_{Vg}^2 = \int_{f_{min}}^{f_{max}} S_{Vg}(f)df \tag{2}$$

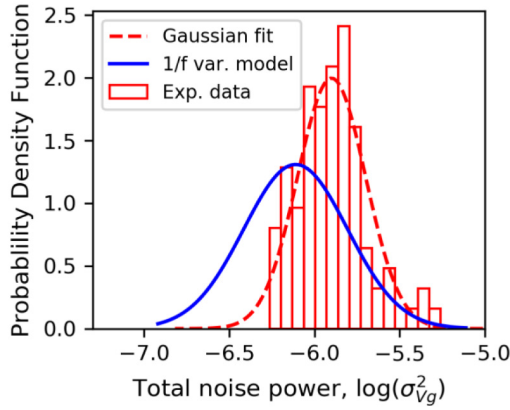

FIGURE 3. Probability Density of total noise power for: experimentally measured PSD (bars), Gaussian using <log(σ^2_{Vg})> and σ(log(σ^2_{Vg})) (dashed line) and 1/f-based generated PSD, using the <log(S_{Vg})> and σ(log(S_{Vg})) values at 10 Hz (solid line).

In Fig. 3, one can clearly observe that, although the total noise power of the experimental data follows a Gaussian distribution, the noise power distribution of the PSD data generated using the 1/f-based variability model cannot predict the experimental one. This indicates that for such downscaled devices a 1/f-based model fails to accurately describe neither the experimental LFN variability nor the noise power, as a consequence of the increased number of devices which exhibit Lorentzian spectra. Therefore, new modeling approaches should be developed which take into consideration the behavior of RTN and GR signals.

The difference in noise power shown in Fig. 3 can be nonetheless understood if we take as an example the expected noise power of a 1/f and a Lorentzian spectrum that coincide at 10Hz, a typical frequency for the extraction and modeling of characteristic noise levels, as shown in Fig. 4a. Combining (1) and (2), the Lorentzian spectrum integral can be calculated and expressed through (3). Similarly, for the 1/f type of noise whose spectral density is $S_{V_g}(f) = S_{V_g}(1)/f$, where $S_{V_g}(1)$ is the 1/f PSD value at f = 1 Hz, the spectrum integral is given by (4).

$$\sigma^2_{Vg,Lor} = S_{Vg}(0)f_c\left(\tan^{-1}\frac{f_{max}}{f_c} - \tan^{-1}\frac{f_{min}}{f_c}\right) \quad (3)$$

$$\sigma^2_{Vg,Flick} = S_{Vg}(1)ln(f_{max}/f_{min}) \quad (4)$$

Based on these equations, we extracted the total noise power for each type of spectra and for different bandwidths. The results are shown in Fig. 4b. It is worth noting that, while the Lorentzian PSD amplitude is 2 orders of magnitude below the 1/f spectrum at the lower and the higher edges of the bandwidth, the total noise power of the Lorentzian spectrum becomes significantly higher (1 order of magnitude), even for a bandwidth equal to its cut-off frequency, f_c. Of course, this behavior would be different if we had chosen a different plateau or f_c for the Lorentzian spectrum. This is another confirmation that the 1/f model fails to emulate the variability caused by Lorentzian spectra. In large

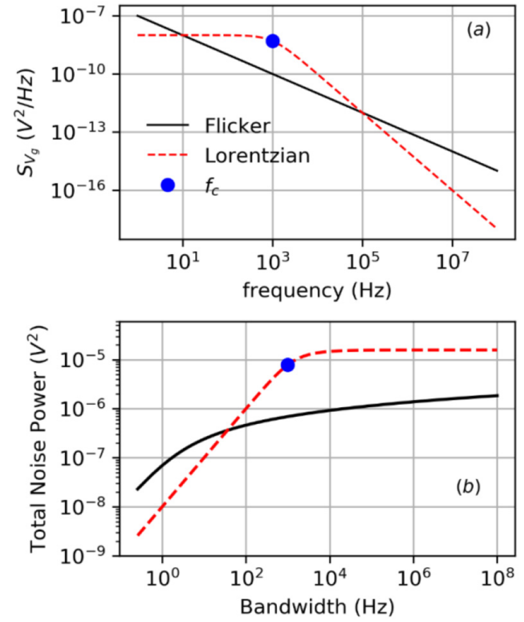

FIGURE 4. (a): 1/f and Lorentzian spectra, with f_c at 1 kHz, that coincide at 10 Hz, (b): total noise power of the spectra shown in (a) [16].

area devices, this disagreement is not a significant issue thanks to high number of traps, which eventually will produce a 1/f-like PSD, but when more downscaled devices are being used, in which the probability of single trap appearance is increased, no reliable estimation can be made concerning the safe operation or stability of circuits. Consequently, specific modeling of Lorentzian-type noise is needed that can describe accurately single trap or GR behavior. Of course, the combination of 1/f and Lorentzian noise can give even more realistic results for variability studies as both types of noise can be present.

III. LORENTZIAN-BASED STATISTICAL PSD GENERATOR

We proceed to emulate the experimental variability using a PSD level generator, that considers a Lorentzian noise spectrum for each RTN trap and calculates the overall noise of each die by adding the PSDs of each trap through (5a) [1], where $\Delta V_{t,k}$ is the electrostatic impact of each trap "k" on the threshold voltage. ΔV_t is expressed through (5b) [20], depending on the depth, x_t, of the trap inside the oxide, for which we considered uniform distribution. $N_{T,d}$ is the total number of traps for die "d" with N_T chosen for every die from a Poisson distribution with an average $\langle N_T\rangle = N_t W L t_{ox}\Delta E$, where N_t is the oxide trap density per volume per energy and ΔE the total energy bandgap. Eq. (5c) describes how A, the space mark ratio, and τ, the trap time constant are calculated using τ_c and τ_e (mean capture and emission time respectively) of each trap [20].

$$S_{Vg}(f)_d = \sum_{k=1}^{N_{T,d}} \frac{4\Delta V_{t,k}{}^2 A_k \tau_k}{1+(2\pi f\tau_k)^2} \quad (a)$$

$$\Delta V_{t,k} = \frac{q\left(1-\frac{x_{t,k}}{t_{ox}}\right)}{WLC_{ox}} \quad (b) \tag{5}$$

$$A_k = \frac{\tau_k}{\tau_{c,k}+\tau_{e,k}}, \qquad \tau_k = \left(\frac{1}{\tau_{c,k}}+\frac{1}{\tau_{e,k}}\right)^{-1} \quad (c)$$

Moreover, for the calculation of τ_c and τ_e we implemented a simplified SRH-like approach. Based on the SRH statistics and according to [21], a more general expression of τ_c and τ_e was developed for a single trap that also accounts for quantum confinement effects in the inversion layer. The new expressions are given below in (6), where σ is the trap's cross section, f_e is the escape frequency ($\approx 2x10^{13}$ Hz), ε_{ox} the oxide permittivity, Q_i the inversion charge at a specific V_g, Q_{it} the inversion charge when the Fermi level E_f crosses the trap energy E_t, Q_d the depletion charge and x_t the trap depth inside the oxide. Another reason to prefer these equations is that through the utilization of the Lambert-W function charge-based drain current model [22], Q_i can be easily calculated, regardless the type of MOSFET (Bulk, FinFET or FDSOI).

$$\tau_c = \frac{q}{\sigma f_e Q_i}\ , \quad \tau_e = \frac{q e^{\frac{x_t(Q_i+Q_d)}{kT\varepsilon_{ox}}}}{\sigma f_e Q_{it}} \tag{6}$$

In order for the randomization (energy and depth) of trap characteristics in terms of cross-section to be introduced in a simplified way, we use a bias-independent parameter τ_0, which is exponentially distributed between 1 ns and 1 ks so as very fast, very slow and all in-between traps to be accounted for. Consequently, (6) was modified and the expressions of the time constants for the Lorentzian PSD generator are given through (7):

$$\tau_{c,k}(V_g) = \tau_{0,k}\frac{Q_i(V_t)}{Q_i(V_g)}, \quad \tau_{e,k}(V_g) = \tau_{0,k}\frac{Q_i(V_t)}{Q_{it}} \tag{7}$$

It should be noted that for simplification reasons, x_t was not accounted for in the emission time calculation but only in the Lorentzian amplitude. In addition, for both capture and emission time constants, we used as a reference the inversion charge at V_t so as the ratio $Q_i(V_t)/Q_i$, to take realistic values of the operating conditions as the $Q_i(V_t)$ could be considered close to the average value of Q_i between weak and strong inversion. Finally, for the extraction of Q_{it}, which is a characteristic of a trap independent on V_g, a random uniformly distributed value is chosen between $\ln(Q_i(0))$ and $\ln(Q_i(1,2))$. We took the logarithm of Q_i to account for to the exponential dependence of Q_i on V_g in the sub-V_t region and thus equal probabilities to be given in the whole range of Q_i for the definition of Q_{it}. Finally, we considered the Q_i for a V_g range from 0 to 1.2 V with V_{dd} at 1 V, as a trap can be active for a range of around $\pm 3kT/q$ from its energy level.

IV. MODEL VALIDATION

One way to test how well a model follows the statistically varied experimental data is to compare the quantile-quantile

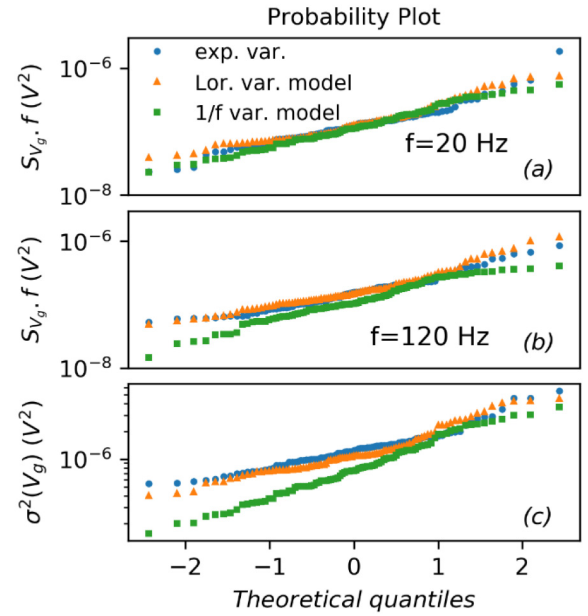

FIGURE 5. Q-Q plots of experimental PSDs, 1/f variability model and Lorentzian-based variability model at two frequencies (a): 20 Hz, (b): 120 Hz, (c): Q-Q plots total noise power for the different cases.

(Q-Q) plots. Q-Q plot is a graphical tool that allows assessing whether different sets of data obey the same distribution such as normal, uniform or exponential. For this reason, the set of data is plotted versus generated values that follow a known distribution, and if the result is a straight line, then the distribution of the dataset can be derived.

In many works, it has been proven that the distribution of noise spectral density follows the log-normal statistics and this is a direct consequence of the exponential distribution of the trap time constants [23], [24]. As a result, when referring to noise variability, statistical analysis of the $\log(S_{V_g})$ should be performed. For the construction of Q-Q plot, the values of PSD are sorted and plotted versus theoretical quantiles which in this case follow the log-normal distribution. We plotted the Q-Q plots of the experimental data, the ones derived from the 1/f model, whose σ was extracted at 20 Hz, and the data extracted by the Lorentzian-based model, explained in III, at two frequencies (20 and 120 Hz). The size of the dataset is 93 devices. The results are shown in Fig. 5(a,b), while the respective data for the total noise power are shown in Fig. 5(c).

From Fig. 5 one can observe that, although the 1/f variability extracted through Monte Carlo simulation, follows well the experimental data at 20 Hz, where we extracted the σ, it fails to do so at higher frequencies, i.e., 120 Hz, and its prediction is even worse regarding the total noise power, $\sigma^2_{V_g}$, estimated by (4). On the other hand, our model, using (5) and (7), can reproduce well the experimental variability in all cases, proving its usefulness and accuracy for circuit-level LFN simulations.

It should be noted that for the best prediction of the experimental variability using the Lorentzian-based model, we

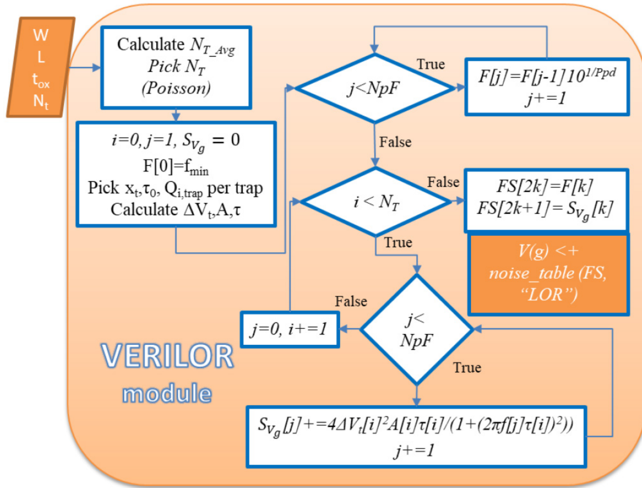

FIGURE 6. **Flowchart of the *VERILOR* module. *NpF:* total number of points in spectrum, *Ppd*: points per decade, f_{min}: starting frequency [16].**

needed to generate a handful of datasets in order to end up with this result, and this is mainly due to the small size of the dataset. This is also the reason why the experimental PSDs and noise power do not follow the linear trend for the log-normal distribution and deviate from this mostly in the extreme cases. Yet, the Lorentzian-based model has the potential to capture perfectly this behavior, allowing us to move on to its implementation in Verilog-A for accurate circuit-level LFN simulations.

V. MODEL IMPLEMENTATION IN VERILOG-A

Since there is no possibility to declare a noise source in Verilog-A through a PSD function different than 1/f (*flicker_noise*) or thermal (*white_noise*) noise, we developed our module using the third option: the *noise_table* function. Therefore, after the automatic creation of a table with frequency values, with a resolution and bandwidth that is user-controlled, the table of PSD values actually uses (5) and sums up the Lorentzian contributors from all active traps. The calculation of N_T, ΔV_t, A and τ follows the procedure described in Section III, like in [25], where a similar module was presented for RTN modeling in the time domain. In the end, the frequency (F) and PSD (S_{V_g}) tables are intertwined (odd/even indexes) together in a new table, *FS*, that is loaded in the *noise_table* function and inserted as a noise source at the MOSFET gate. The flowchart of our module, called *VERILOR*, [16], is shown in Fig. 6. It takes as inputs the gate oxide dimensions (W, L, t_{ox}) and the oxide trap density, N_t, per volume and energy and then, the procedure described in Section III follows. It should be clarified that the *VERILOR* implementation methodology is model-independent, meaning that any expression for the trap parameters ΔV_t, τ_c and τ_e can be utilized, including more advanced and physically accurate approaches like the ones presented in [26] and [27]. The development of a new RTN model is out of the scope of this work, which uses the expressions of (5) and (7) as a simplified model example that fits well the data, in order to focus on the Lorentzian noise implementation methodology for circuit simulations.

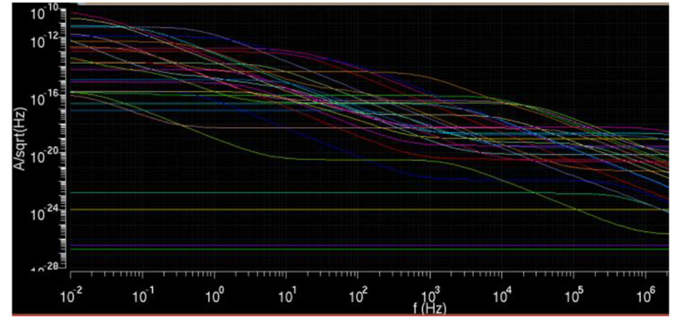

FIGURE 7. **Screenshot of noise variability (60 dies) simulation results in Cadence Spectre, using the *VERILOR* module. (W = 80nm/L = 30nm).**

The only limitation induced by Verilog-A in our case is that the size of the arrays has to be defined from the beginning and the dynamic change of their size is not possible. Consequently, regarding the frequency array, its size depends on the user's needs, concerning resolution and bandwidth. Similarly, for the arrays related to traps characteristics, a maximum number of traps must be considered so as different dimensions to be covered. In our case, we considered a maximum number of traps equal to 1000, a number that can however be automatically chosen by the SPICE simulator, as a function of W,L,t_{ox}. Fig. 7 shows how the *VERILOR* module can generate realistic LFN variability results in a circuit simulator like Cadence Spectre, using the physics-based approach of (5) and (7). By doing so, extreme cases of circuits operation can be predicted.

VI. VALIDATION OF VERILOR MODULE

Before pursuing to further device and circuit simulations with the *VERILOR* module, we first need to confirm the validity of our model and its Verilog-A implementation. For this reason, we simulated the LFN induced by three individual traps in a single device and for the same traps' characteristics, x_t, τ_0, Q_{it}, we calculated the resulted PSD using (5).

As demonstrated in Fig. 8, the *VERILOR*-generated spectrum is in full agreement with theory in terms of PSD shape confirming the successful implementation in Verilog-A. Moreover, in Fig. 9 we demonstrate that *VERILOR* can be used in combination with the *flicker_noise* module for simulation of both GR and 1/f noise sources for more realistic device and circuit simulations, when GR centers in the semiconductor co-exist with traps in the oxide.

For further validation of the module, we compared the PSD induced from one single trap using *VERILOR* with the one resulted from a RTN time-domain Verilog-A model [25]. In addition, for the time domain simulation case, we used the Transient Noise (TN) [28] module provided in Spectre, which considers the PSD defined in the model and produces a time domain variance that corresponds to the

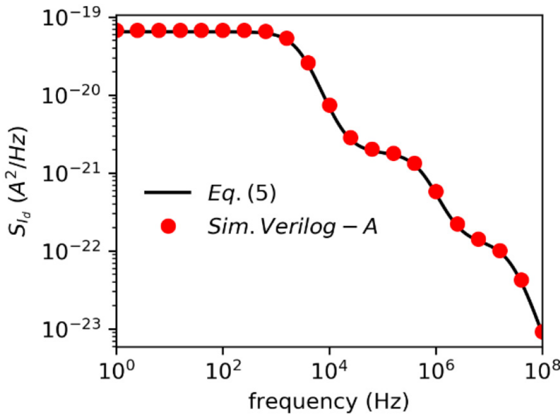

FIGURE 8. PSD comparison between the Lorentzian spectrum obtained by our Verilog-A model and the calculated one from (5) using the same parameters for 3 traps [16].

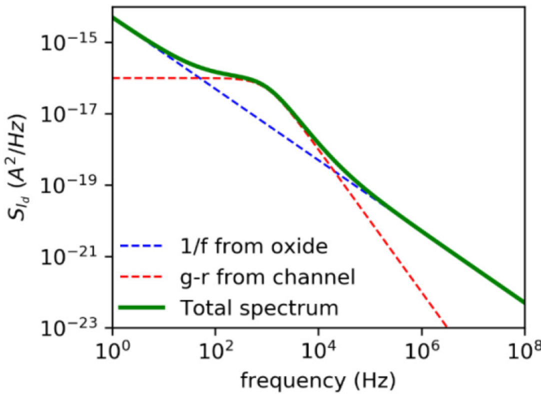

FIGURE 9. Example of GR noise added on top of 1/f, combining ***VERILOR*** with ***flicker_noise*** in Verilog-A [16].

PSD integral of a user-defined bandwidth. As shown in Fig. 10b, both methods lead to identical spectral density in the frequency domain, while in time domain both modules give the same signal variance and so, equal noise power (see Fig. 10a). Of course, *VERILOR*, as a frequency domain model, cannot generate the abrupt transitions of the RTN signal in the time domain, but only its RMS amplitude. Thus, when it comes to simulating RTN in circuits, if what matters is the RTN presence and amplitude and not particularly its sudden transition events, *VERILOR* can be combined with the simulator's Transient Noise module, to fairly reproduce the power of the RTN signal in the time domain. Therefore, the level of dynamic variability can be accurately predicted by *VERILOR*, even with no RTN module in the time domain. However, if the transition instants are important for the simulation, as is the case for predicting RTN-induced SRAM errors, one needs to include the time domain RTN generator within the *VERILOR* module. Moreover, the time domain module has a significantly lower simulation time (1.5s for the example of Fig. 10) than the TN-generated signal (3s when *NpF* is only 30) using *VERILOR*.

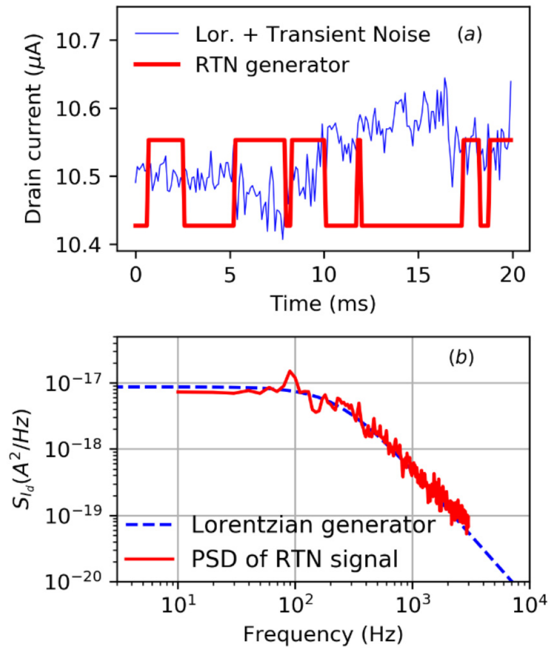

FIGURE 10. (a): Drain current transient signal of LambertW-based MOSFET from the RTN model [25] and the TN module, (b): Power spectral density from the RTN model [25] and ***VERILOR [16]***.

VII. SIMULATION EXAMPLES USING VERILOR

A. AREA SCALING

In order to observe the behavior of the *VERILOR* module with device area and number of traps, and finally conclude whether this module can correctly capture the well-established carrier number fluctuations (CNF) model [29] and the deviation from the 1/f PSDs in small area devices, we performed additional simulations for different gate areas and corresponding total number of traps. As it is demonstrated in Fig. 11a, *VERILOR* module can automatically reproduce Lorentzian-like spectra for highly scaled areas and 1/f-like for larger ones, confirming that indeed for uniform distribution of traps in large are devices, the overall simulated spectrum is 1/f. In fact, it coincides with the calculated CNF-based 1/f spectrum. On top of that, it is able to generate a 1/f noise level that is in total agreement with the area-normalized CNF model from weak to strong inversion, as depicted in Fig. 11b.

Since we proved that the *VERILOR* gives 1/f-like PSDs when the number of traps is high, it is interesting to compare the simulation time performance between a Flicker module and *VERILOR*. For this reason, we ran the modules with different number of traps, and we extracted the simulation time for each case.

As one can assume, and as shown in Fig. 12, the required CPU time using the Flicker module (around 20ms) is independent of N_T, since it takes as an input only the S_{Vfb} (flat-band voltage PSD) value. On the other hand, the simulation time for *VERILOR* is directly dependent on the number of traps because the model has to calculate each trap's RTN amplitude and kinetics. As a result, with the exception of a

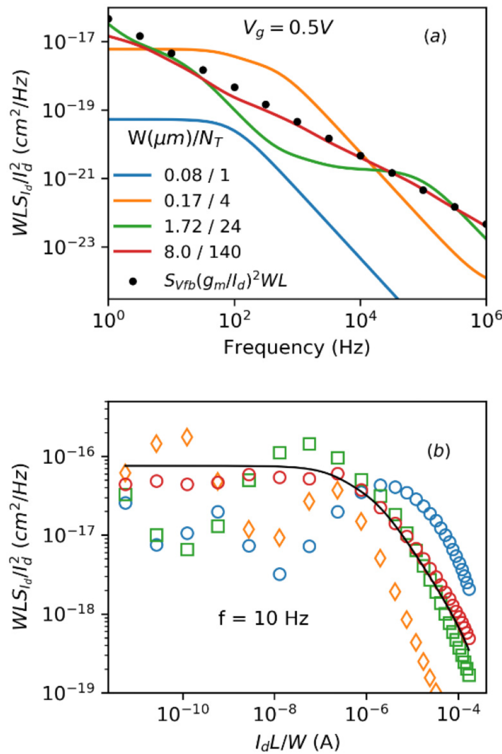

FIGURE 11. (a): Area-normalized PSD of drain current versus frequency at $V_g = 0.5$ V and (b): versus normalized drain current for f = 10 Hz, for 4 different W and corresponding N_T, along with CNF model. (L = 0.3 μm) [16].

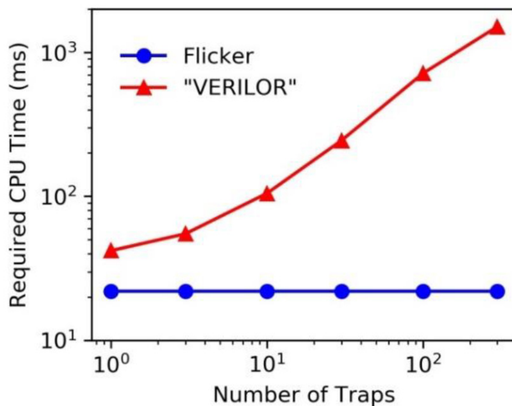

FIGURE 12. Required CPU time versus number of traps for Flicker (blue) and *VERILOR* (red) modules.

single trap case (two-level RTN study) where the *VERILOR* simulation time is quite close to the Flicker module, for a higher number of traps this duration increases exponentially with N_T. Nevertheless, since we proved that the *VERILOR*-generated PSD reaches a 1/f behavior for high numbers of traps in large geometries, the user could prioritize the use of the Flicker module above a certain number of traps. By doing so, similar results will be derived with less simulation time.

B. CMOS INVERTER

As an easy and direct way to verify that the *VERILOR* module can be successfully used in a circuit with many

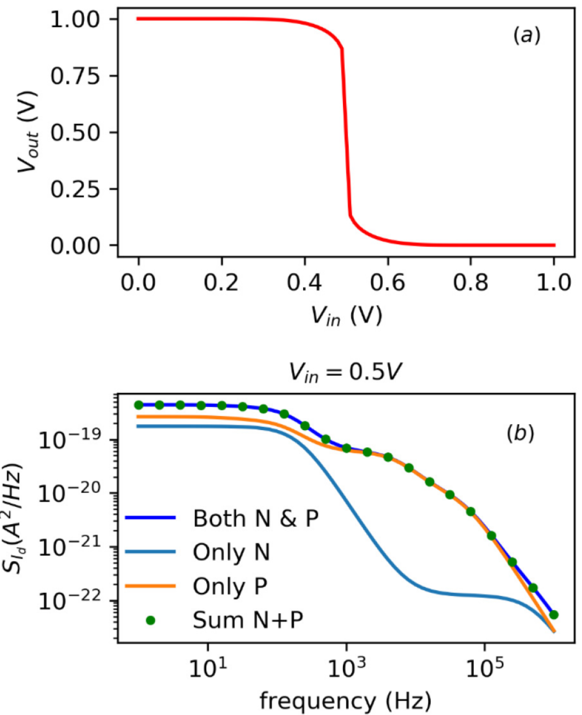

FIGURE 13. (a): I/O Inverter curve, (b): Output current PSD of LW-based CMOS inverter versus frequency for Vin = 0.5V and V_{dd} = 1V, along with separate noise contributions from each MOSFET, and their sum. (W/L = 80/30 nm) [16].

transistors, we implemented the module for both p- and n-type devices so as to design a LambertW-based CMOS inverter. The inverter's voltage transfer characteristic is shown in Fig. 13a. We chose each transistor to have different number of traps with different characteristics. Also, since we focused on a highly scaled-down geometry (W/L = 80/30 nm), only a handful of active traps was considered. Then, we compared the total output noise with the sum of the individual device spectra and the result can be seen in Fig. 13b. One can see that there is a total agreement between them confirming that the *VERILOR* module can be successfully used at a circuit level with a different distribution of traps per device.

C. RING OSCILLATOR'S PHASE NOISE

In circuits like oscillators, the LFN up-converts to phase noise [30] close to the oscillation frequency, f_0, making the frequency domain noise simulation crucial. Using the *VERILOR* module, we estimated the impact of Lorentzian noise on a 3-stage Ring Oscillator's (RO) phase noise. The RO's voltage output is shown in Fig. 14a. As can be seen in Fig. 14b, while 1/f up-converts to $1/f^3$ (−30dBc/dec), a Lorentzian spectrum up-converts to $1/f^2$ (−20dBc/dec) close to f_0 and then to $1/f^4$ (−40dBc/dec) after the Lorentzian's cut-off frequency, f_c. As a result, for a scenario where 1/f coincides with the Lorentzian at 1 Hz, the phase noise becomes significantly higher (≈20dBc) around f_c, while the corner frequency, i.e., where LFN meets the thermal noise

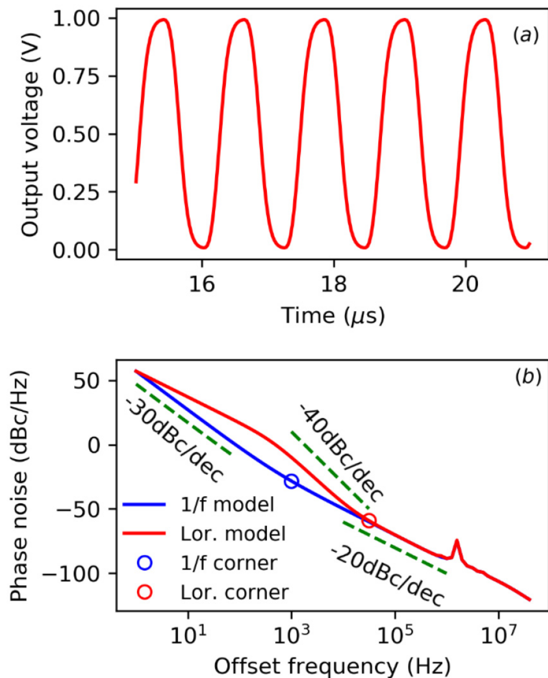

FIGURE 14. (a): RO's output voltage versus time, (b): Phase noise of LambertW-based 3-stage CMOS ring oscillator versus offset frequency for 1/f and Lorentzian noise [16].

level, from the "1/f corner" point, due to 1/f spectrum, is shifted upwards to the "Lor. corner", by more than one decade due to the Lorentzian spectrum.

This observation underlines the importance of Lorentzian noise modeling in RF/mixed signal circuits, where the operation bandwidth is a critical Figure of Merit. The opposite (lower phase noise and corner frequency) could also take place, if the Lorentzian, due to variability, had a lower plateau, leading to a more optimistic result compared to 1/f. Thus, it is important to remind (Fig. 11) how the *VERILOR* module can also reproduce the LFN variability effect in a circuit simulator, using the physics-based approach of (5)-(6).

VIII. CONCLUSION

To conclude, in this work we presented a new method of noise model implementation for circuit simulations, which enables the generation of Lorentzian-type spectra, based on every trap's property. The *VERILOR* module has been successfully validated and applied at both device and circuit level. Finally, the Ring Oscillator was used to showcase the usefulness and applicability of the *VERILOR* model in circuit noise simulations. We demonstrated that the Lorentzian noise can either degrade or improve the phase noise close to the oscillation frequency, as well as the LFN corner frequency.

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REFERENCES

[1] E. G. Ioannidis *et al.*, "Low frequency noise variability in high-k/metal gate stack 28nm bulk and FD-SOI CMOS transistors," in *Int. Electron Devices Meeting Tech. Dig.*, 2011, pp. 449–452.
[2] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "Random telegraph noise of deep-submicrometer MOSFETs," *IEEE Electron Device Lett.*, vol. 11, no. 2, pp. 90–92, Feb. 1990, doi: 10.1109/55.46938.
[3] S. Mahapatra, N. Goel, and S. Mukhopadhyay, *Fundamentals of Bias Temperature Instability in MOS Transistors*, vol. 139. New Delhi, India: Springer, 2016.
[4] W. Fang, E. Simoen, M. Aoulaiche, J. Luo, C. Zhao, and C. Claeys, "Distinction between silicon and oxide traps using single-trap spectroscopy," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 212, no. 3, pp. 512–517, 2015, doi: 10.1002/pssa.201400087.
[5] N. B. Lukyanchikova, M. V Petrichuk, N. P. Garbar, E. Simoen, and C. Claeys, "Non-trivial GR and 1/f noise generated in the p-Si layer of SOI and SOS MOSFETs near the inverted front or buried p-Si/SiO2 interface," *Semicond. Sci. Technol.*, vol. 14, no. 9, pp. 775–783, 1999, doi: 10.1088/0268-1242/14/9/306.
[6] A. L. Rodríguez *et al.*, "Dependence of generation—Recombination noise with gate voltage in FD SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2780–2786, Oct. 2012.
[7] C. G. Theodorou, E. G. Ioannidis, S. Haendler, E. Josse, C. A. Dimitriadis, and G. Ghibaudo, "Low frequency noise variability in ultra scaled FD-SOI n-MOSFETs: Dependence on gate bias, frequency and temperature," *Solid-State. Electron.*, vol. 117, pp. 88–93, Mar. 2016, doi: 10.1016/j.sse.2015.11.011.
[8] K. V. Aadithya, A. Demir, S. Venugopalan, and J. Roychowdhury, "SAMURAI: An accurate method for modelling and simulating non-stationary random telegraph noise in SRAMs," in *Proc. Design Autom. Test Europe*, 2011, pp. 1113–1118, doi: 10.1109/date.2011.5763183.
[9] M. Luo, R. Wang, J. Wang, S. Guo, J. Zou, and R. Huang, "Compact modeling of random telegraph noise in nanoscale MOSFETs and impacts on digital circuits," in *Proc. Tech. Progr. Int. Symp. VLSI Technol. Syst. Appl.*, 2014, pp. 14–15, doi: 10.1109/VLSI-TSA.2014.6839681.
[10] G. I. Wirth, J. Koh, R. da Silva, R. Thewes, and R. Brederlow, "Modeling of statistical low-frequency noise of deep-submicrometer MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1576–1588, Jul. 2005, doi: 10.1109/TED.2005.850955.
[11] G. I. Wirth, R. da Silva, and R. Brederlow, "Statistical model for the circuit bandwidth dependence of low-frequency noise in deep-submicrometer MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 340–345, Feb. 2007, doi: 10.1109/TED.2006.888672.
[12] C. Y.-P. Chao *et al.*, "Statistical analysis of the random telegraph noise in a 1.1 μm pixel, 8.3 MP CMOS image sensor using on-chip time constant extraction method," *Sensors*, vol. 17, no. 12, p. 2704, Dec. 2017, doi: 10.3390/S17122704.
[13] J. Rhayem *et al.*, "Impact of scaling down from 0.25 μm to 0.18 μm CMOS technology on 1/f noise: Characterisation and modelling," in *Proc. IEEE 32nd Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2002, p. 25.
[14] E. Barajas *et al.*, "Analysis of body bias and RTN-induced frequency shift of low voltage ring oscillators in FDSOI technology," in *Proc. IEEE 28th Int. Symp. Power Timing Model. Optim. Simulat.*, 2018, pp. 82–87, doi: 10.1109/PATMOS.2018.8464145.
[15] C. Leyris, S. Pilorget, M. Marin, M. Minondo, and H. Jaouen, "Random telegraph signal noise SPICE modeling for circuit simulators," in *Proc. 37th Eur. Solid-State Device Res. Conf.*, vol. 37, 2007, pp. 187–190, doi: 10.1109/ESSDERC.2007.4430910.
[16] A. Tataridou, G. Ghibaudo, and C. Theodorou, "VERILOR: A verilog-a model of lorentzian spectra for simulating trap-related noise in CMOS circuits," in *Proc. IEEE 51st Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2021, pp. 247–250.
[17] M. B. Da Silva, H. Tuinhout, A. Zegers-Van Duijnhoven, G. I. Wirth, and A. Scholten, "A physics-based RTN variability model for MOSFETs," in *Int. Electron Devices Meeting Tech. Dig.*, 2015, pp. 35.2.1–35.2.4, doi: 10.1109/IEDM.2014.7047173.
[18] M. B. Da Silva, H. P. Tuinhout, A. Zegers-Van Duijnhoven, G. I. Wirth, and A. J. Scholten, "A physics-based statistical RTN model for the low frequency noise in MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3683–3692, Sep. 2016, doi: 10.1109/TED.2016.2593916.
[19] S. Barraud *et al.*, "Opportunities and challenges of nanowire-based CMOS technologies," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf.*, 2015, pp. 1–3.

[20] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 573–582, 2002, doi: 10.1016/S0026-2714(02)00025-2.

[21] C. Theodorou and G. Ghibaudo, *Noise and Fluctuations In Fully Depleted Silicon-On-Insulator MOSFETs*. Cham, Switzerland: Springer Int., 2020.

[22] T. A. Karatsori *et al.*, "Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction," *Solid-State. Electron.*, vol. 111, pp. 123–128, Sep. 2015, doi: 10.1016/j.sse.2015.06.002.

[23] D. Lopez, S. Haendler, C. Leyris, G. Bidal, and G. Ghibaudo, "Low-frequency noise investigation and noise variability analysis in high-k/metal gate 32-nm CMOS transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2310–2316, Aug. 2011, doi: 10.1109/TED.2011.2141139.

[24] B. Yu *et al.*, "Modeling local variation of low-frequency noise in MOSFETs via sum of lognormal random variables," in *Proc. Custom Integr. Circuits Conf.*, 2012, pp. 12–15, doi: 10.1109/CICC.2012.6330573.

[25] C. G. Theodorou and G. Ghibaudo, "A self-contained defect-aware module for realistic simulations of LFN, RTN and time-dependent variability in FD-SOI devices and circuits," in *Proc. IEEE S3S Conf.*, 2018, pp. 1–3.

[26] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectron. Rel.*, vol. 52, no. 1, pp. 39–70, 2012.

[27] B. Kaczer *et al.*, "The defect-centric perspective of device and circuit reliability—From individual defects to circuits," in *Proc. Eur. Solid-State Device Res. Conf.*, vol. 45, 2015, pp. 218–225, doi: 10.1109/ESSDERC.2015.7324754.

[28] P. Bolcato and R. Poujois, "A new approach for noise simulation in transient analysis," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, 1992, pp. 887–890.

[29] G. Ghibaudo, "On the theory of carrier number fluctuations in MOS devices," *Solid-State. Electron.*, vol. 32, no. 7, pp. 563–565, 1989, doi: 10.1016/0038-1101(89)90113-5.

[30] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999, doi: 10.1109/4.766813.