Received 17 April 2022; revised 14 May 2022; accepted 16 May 2022. Date of publication 18 May 2022; date of current version 2 August 2022.
The review of this article was arranged by Editor L. Hutin.

Digital Object Identifier 10.1109/JEDS.2022.3176205

Characterization and Modeling of Quantum Dot Behavior in FDSOI Devices

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This work was supported in part by the National Sciences and Engineering Research Council of Canada (NSERC); in part by the Ontario Centres of Excellence through 5G ECQOR Grant; in part by the EU Horizon 2020 FET OPEN Project "IQubits" under Grant 829005; and in part by the Romanian Authority for Scientific Research, UEFISCDI under Project PN-III-P3-3.6-H2020-2020-0054.

ABSTRACT A compact analytical model is proposed along with a parameter extraction methodology to accurately capture the steady-state (DC) sequential tunneling current observed in the subthreshold region of the transfer $I_{DS} - V_{GS}$ characteristics of MOSFETs at cryogenic temperatures. The model is shown to match measurements of *p*-MOSFETs and *n*-MOSFETs manufactured in a commercial 22nm FDSOI foundry technology, with reasonable accuracy across bias conditions and temperature (2 K - 50 K). Furthermore, the extracted model parameters are used to analyze the impact of the gate and drain voltages and of layout geometry on the device characteristics.

INDEX TERMS Compact modeling, Coulomb Blockade, cryogenics, semiconductor quantum dot, silicon germanium, silicon-on-insulator, cryo-CMOS.

I. INTRODUCTION

Cryogenic characterization [1]–[4] and modeling of CMOS technologies [5], [6] have gained attention in the past few years because of their potential use in cryogenic control and readout electronics for quantum processors [7]–[9]. While much of this work was focused on modeling the classical behavior of MOSFETs at cryogenic temperatures, discussion on how to capture the experimentally observed quantum effects in a compact model for circuit design is lacking. Production FinFET [10], [11] and FDSOI MOSFETs [12] exhibit strong sequential tunnelling effects in their I-V characteristics in the subthreshold region at low temperatures up to 50 K [13] due to the formation of a quantum dot (QD) in the device channel. Strong charge confinement is created due to the gate and STI oxides in the directions perpendicular to the channel, and due to electrostatic potential barriers formed below the gate oxide spacers [14] towards the source and drain. As sketched in the cartoon in Fig. 1, this leads to single electron/hole transistor (SET/SHT) behavior which manifests itself as multiple current peaks and valleys in the subthreshold region of the transfer characteristics at low V_{DS} [10]. At larger V_{DS}, transport across multiple energy levels will make the peaks less clearly defined. In FDSOI MOSFETs, Fig. 2, the positions of the current peaks and valleys can be controllably shifted to higher and lower V_{GS} values by employing MOSFETs with different threshold voltage flavors and back-gate doping type, as illustrated in Fig. 3, and also by changing the back-gate voltage. Fig. 4 shows that, in the latter case, the current peak values also change by orders of magnitude due to the interplay between the barrier heights and the quantized energy levels in the QD. The similar ΔV_{GS} between the first and the second detected peaks (30-34 mV for devices in Fig. 3) for devices with identical geometry but different V_t flavors suggests that this behavior depends primarily on the device geometry.

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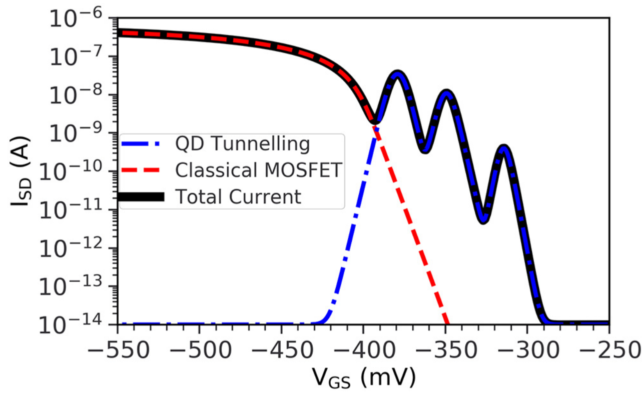

FIGURE 1. Cartoon I-V characteristics of a MOSFET based SHT with the total current (solid black), classical MOSFET current (dashed red) and QD tunnelling current (dash-dot blue).

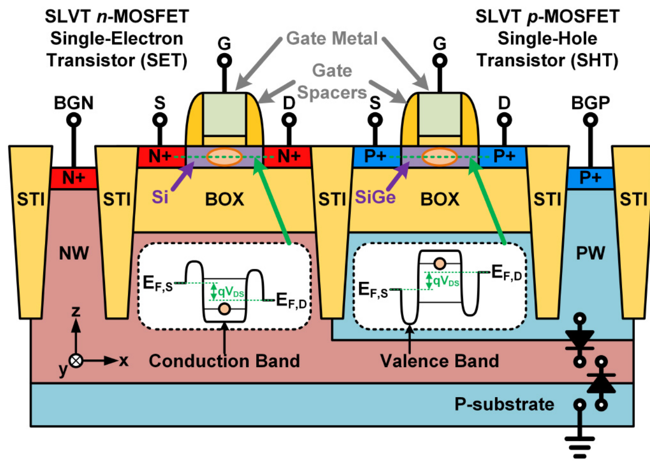

FIGURE 2. Cross-section diagram of SLVT FDSOI CMOS transistors which behave as single-electron/hole transistors (SETs/SHTs) at cryogenic temperatures. The QD in the conduction/valence band (E_C/E_V) in the n/p-MOSFET is depicted under their respective gates, showing the formation of the energy potential barriers in the x-direction under the gate spacers and occupation of the ground state energy level by an electron/hole below/above the Fermi potentials in the source and drain regions.

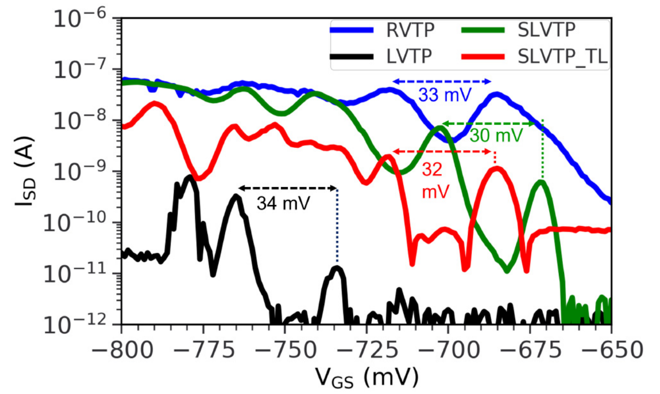

FIGURE 3. Transfer characteristics of identical layout, single gate finger 18nmx50nm FDSOI p-MOSFETs with 6 dummy gates and different threshold voltage flavors fabricated on the same die and measured a few minutes apart at $T = 2$ K under 2.5 Tesla magnetic field and at $V_{DS} = -1$ mV. ΔV_{GS} between the first and second detected tunnelling current peaks varies between 30 mV and 34 mV for the super low V_t, SLVTP, (undoped channel and p-type back-gate well region), SLVTP_TL (same as SLVTP but coupled to a $\lambda/2$ transmission line resonator at 60 GHz), low V_t, LVTP, (implanted channel for threshold adjustment), and reverse well, RVTP, (undoped channel with reversed back-gate well polarity) devices. $\Delta V_{GS} = \frac{q}{C_G}$ where C_G is the intrinsic capacitance between the gate and the QD below the gate and q is the electron charge. All devices were measured with a floating back-gate.

Unfortunately, this behavior, which will manifest itself at progressively higher temperatures in future, aggressively scaled technology nodes, is not captured by any of the current MOSFET compact models. These effects are also crucial when operating MOSFETs as QD qubits and in any analog mixed-signal circuits where the MOSFETs are biased in the subthreshold region. The former is very important for simulating monolithic quantum processors with the qubits and interface electronics integrated on the same die [12], [15]–[17]. Additionally, a comprehensive model capturing these effects will provide a means to analytically compare and analyze these quantum effects across various technology nodes for implementing qubits and quantum dot charge sensors, and help inform design decisions to control these effects.

In this work, the presence of quantum effects in FDSOI p-MOSFETs and n-MOSFETs is demonstrated and characterized. Furthermore, a compact analytical model accurately capturing the impact of eigenenergy spacing due to charge quantization and of Coulomb blockade on the drain current characteristics of a MOSFET-based semiconductor QD is described. This model is implemented as a Verilog-A add-on to the foundry design kit model (Fig. 5). Section II discusses the FDSOI device structure and the formation of the spacer-defined QD in these devices, while Section III describes the model equations and the model parameter extraction methodology. Section IV compares the model with measurements of 18 nm x 70nm SLVT FDSOI p-MOSFETs and SLVT n-MOSFETs across bias and temperatures and highlights its limitations and possible future extensions to make it more physical. An application scenario of the compact model to the simulation of a SET with a transimpedance amplifier for charge-based readout of semiconductor qubits is also discussed. Finally, the conclusion is presented in Section V.

II. SI/SIGE SEMICONDUCTOR QUANTUM DOTS IN FDSOI

The cross-sections of the 22nm FDSOI n/p-type SLVT MOSFETs are depicted in Fig. 2. The SLVT devices have the lowest threshold voltage and are best suited for SET/SHT and cryogenic controller design because they allow for a larger $V_{DD} - V_t$ bias range at cryogenic temperatures, where the absolute value of the threshold voltage increases by up to 200 mV. A QD capable of confining individual electrons/holes is formed in the conduction/valence band (E_C/E_V) at the center of the channel region between source and drain. The top gate oxide and the buried oxide (BOX)

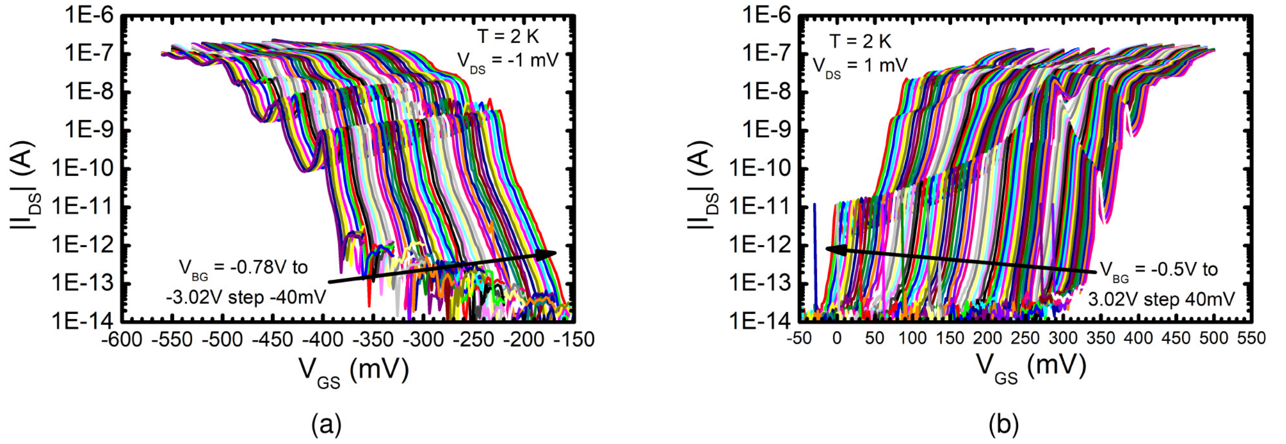

FIGURE 4. Measured transfer characteristics of a 18nmx70nm (with 6 dummy gates) (a) *p*-MOSFET for $V_{BG} = -0.78$ V to -3.02 V and (b) *n*-MOSFET for $V_{BG} = -0.5$ V to 3.02 V at $|V_{DS}| = 1$ mV and $T = 2$ K.

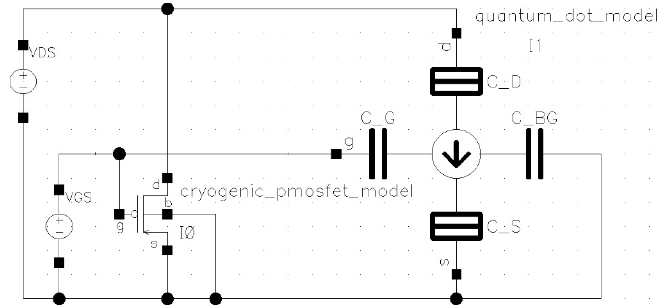

FIGURE 5. Schematic of the proposed compact model with the foundry p-MOSFET (I0), adapted to fit classical cryogenic behavior, in parallel with a single-hole transistor model implemented in Verilog-A (I1). The subscript *t* is used to indicate the circuit elements needed to model tunnelling and disambiguate from traditional MOSFET parasitic capacitances.

form potential barriers in the *z*-direction while the barriers in the *y*-direction are due to STI oxides. These potential barriers are a few eV in height and can be considered infinitely tall relative to the thermal energy at 50 K (≈3 meV), the highest temperature at which SET/SHT behavior is observed. Finite potential barriers are also created below the gate oxide spacers along the *x*-direction, between the channel region under the gate and the heavily doped source and drain contact regions, since the gate metal does not cover the gate oxide spacers [12]. In the *p*-MOSFET, because of the higher Ge mole fraction in the source/drain regions compared to that in the SiGe channel [18], a heterojunction is formed which increases the potential barrier height in the valence band of *p*-MOSFET compared to that encountered in the conduction band of the *n*-MOSFET. This leads to stronger confinement in the *p*-MOSFET QD compared to the *n*-MOSFET QD, where the potential barriers are purely electrostatic.

Modeling the SET/SHT behavior of these FDSOI MOSFETs requires information about the first few eigenenergy levels. An analytical expression for the eigenenergies of the FDSOI MOSFET QD can be derived using the time-independent Schrödinger equation (TISE) [19]

$$E\psi(x,y,z) = \left[-\frac{\hbar^2}{2}\left(\frac{1}{m_x^*}\frac{\partial^2}{\partial x^2} + \frac{1}{m_y^*}\frac{\partial^2}{\partial y^2} + \frac{1}{m_z^*}\frac{\partial^2}{\partial z^2}\right) + V(x,y,z)\right] \times \psi(x,y,z) \tag{1}$$

where $V(x, y, z)$ describes the potential energy of the electron/ hole in 3D space with a parabolic approximation for the effective mass, m^*, which is assumed to be anisotropic but homogeneous. Since the thin channel is surrounded by oxide, the energy potential barriers can be considered infinite in the *y*- and *z*-directions ($\psi_{x,y,z} = 0$ for $y \in [-W_f/2, W_f/2]$ and $z \in [-t_{ch}/2, t_{ch}/2]$). Assuming the reference potential inside the QD to be 0, the potential profile can be approximated as

$$V(x,y,z) = \begin{cases} 0 & |x| < \frac{L_g}{2}, |y| < \frac{W_f}{2}, |z| < \frac{t_{ch}}{2} \\ V_{x,0} & |x| \geq \frac{L_g}{2}, |y| < \frac{W_f}{2}, |z| < \frac{t_{ch}}{2} \\ \infty & |y| \geq \frac{W_f}{2} \quad or \quad |z| \geq \frac{t_{ch}}{2}. \end{cases} \tag{2}$$

For a MOSFET with known gate length, L_g, gate finger width, W_f, and channel thickness, t_{ch}, the *n*th eigenenergies due to confinement in the *y*- and *z*-directions can be found as the solutions of the infinite rectangular potential well [19]

$$E_{l,n} = \frac{\pi^2\hbar^2}{2}\left(\frac{l^2}{m_y^* W_f^2} + \frac{n^2}{m_z^* {t_{ch}}^2}\right) \tag{3}$$

with

$$E_{l,0} \approx \frac{376meV}{\left(m_y^*/m_0\right)}\left(\frac{l}{W_f/(1nm)}\right)^2 \tag{4}$$

and

$$E_{0,n} \approx \frac{376meV}{\left(m_z^*/m_0\right)}\left(\frac{n}{t_{ch}/(1nm)}\right)^2 \tag{5}$$

where m_0 is the electron rest mass and $l, n = 1, 2, 3..$ are positive integers. To obtain the approximate *x*-direction eigenenergy solutions, either a TCAD simulation of the

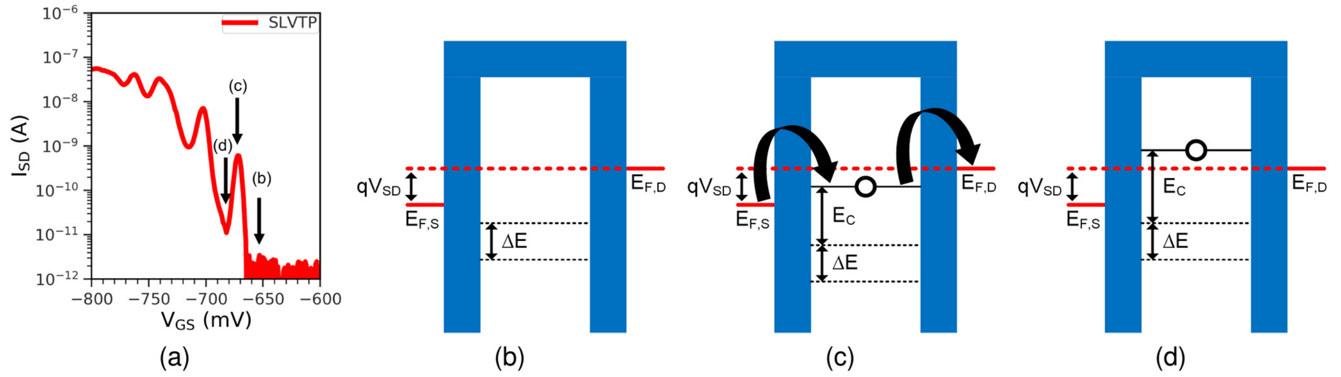

FIGURE 6. **(a) Measured $I_{SD} - V_{GS}$ characteristics of a 18nmx50nm SLVT *p*-MOSFET at $V_{DS} = -1$ mV and $T = 2$ K indicating the relevant V_{GS} values for the simplified valence band diagrams (shown in blue). (b) Simplified valence band diagram corresponding to bias point (b) when the energy levels in the QD are not occupied by holes and are located below the source Fermi level ($E_{F,S}$). (c) Simplified valence band diagram corresponding to bias point (c) when the first energy level in the QD lies between the source and drain Fermi levels ($E_{F,D}$). A hole can tunnel sequentially from the source into the first energy level in the QD and then into the drain, corresponding to the first tunnelling current peak in the transfer characteristics. The energy required to add another hole in the QD increases by E_C (charging energy) beyond that required by the first hole. (d) Simplified valence band diagram corresponding to bias point (d) when the first energy level in the QD lies above the $E_{F,D}$ and is occupied by a single hole which remains confined in the QD.**

E_C/E_V profile along the channel (as in [12]) or a simple finite rectangular potential well approximation can be used (with trade-offs in accuracy). For the minimum sized *n*-MOSFETs available in the 22nm FDSOI CMOS process with L_g = 18 nm, assumed finite rectangular well height of $V_{x,0} = 9$ meV [12] and $m_x^* = 0.2\ m_0$ [20]), the difference between the first and second eigenenergy solutions in the *x*-direction is found to be ≈5.75 meV [19]. Similarly for the minimum sized *p*-MOSFET with the same L_g = 18 nm, but with assumed finite rectangular well height of $V_{x,0}$ = 40 meV [12] and $m_x^* = 0.08\ m_0$ [21], the difference between the first and second eigenenergy solutions in the *x*-direction is found ≈19.99 meV. These differences between the first two eigenenergy levels are larger than those in the *y*-direction for the minimum sized MOSFETs with $W_f = 50$ nm. If the *y*-direction effective masses are assumed to be the same as those in the *x*-direction, then $E_{2,1}$ - $E_{1,1}$ is 2.256 meV for the *n*-MOSFET and 5.64 meV for the *p*-MOSFET. The eigenenergies from quantization in the *z*-direction need not be considered for a model of the first few eigenenergy levels of the FDSOI MOSFET QDs since the channel is very thin ($t_{ch} \approx 6$ nm).

III. QUANTUM DOT MODEL

A. MODEL EQUATIONS

The measured transfer characteristics at 2 K of a minimum size p-MOSFET biased at $V_{DS} = -1$ mV are shown in Fig. 6 along with cartoons of the corresponding valence band diagrams illustrating sequential tunnelling of holes from the source into the drain. When $|V_{GS}|$ is low, all QD energy levels lie below the source Fermi level ($E_{F,S}$) and no tunnelling current flows in the device (Fig. 6(b)). As V_{GS} becomes more negative, the first energy level in the valence band QD moves between the source and drain Fermi levels, $E_{F,D}$ (Fig. 6(c)). Holes can now sequentially tunnel (one by one) from the source reservoir into the drain reservoir via the first energy level of the QD, leading to a current peak in the measured transfer characteristics (Fig. 6(a)). While the first energy level of the QD is occupied by a hole, extra energy is required to add the second hole of the opposite spin. This extra energy must overcome the Coulomb repulsion force caused by the first hole and is known as charging energy, E_C. As V_{GS}, becomes more negative, (Fig. 6(d)), the tunnelling current is blocked. This effect is known as Coulomb Blockade [22].

The impact of sequential tunnelling on the $I-V$ characteristics becomes significant when the following two conditions are satisfied. First, the resistances of the potential barriers between the source and drain and the QD should each be larger than $h/q^2 = 25.8\ k\Omega$ (where h is Planck's constant and q is the electron charge). Second, the addition energy required to add the ith electron/hole to a QD ($E_{add,i}$), is larger than the thermal energy, k_BT, where k_B is Boltzmann's constant and T is the absolute temperature) [22]. The latter condition can be expressed as:

$$E_{add,i} = E_{C,i} + \Delta E_i = \frac{q^2}{C_{tot,i}} + \Delta E_i > k_BT \tag{6}$$

where $E_{C,i} = \frac{q^2}{C_{tot,i}}$ is the charging energy for adding the ith electron/hole in the QD with $i > 1$. ΔE_i is the energy spacing between adjacent QD energy levels which must be overcome to add the odd i^{th} electron/hole to the QD. $\Delta E_i = 0$ for even numbered electrons/holes to account for a spin degeneracy of two for each energy level in the QD.

To further simplify the model, we assume that the current through the QD depends only on the two most likely (i,$i-1$) numbers of electrons/holes in the QD to participate in the tunnelling event and neglect the effect of co-tunnelling. Under these assumptions, the tunnelling current for the ith peak in the transfer characteristics ($I_{DS}-V_{GS}$) can be derived analytically using the steady-state master equations [23] and

is expressed as

$$I_{t,i} = q_c \frac{T_S^+(i-1)T_D^-(i) - T_S^-(i)T_D^+(i-1)}{T_S^+(i-1) + T_S^-(i) + T_D^-(i) + T_D^+(i-1)} \quad (7)$$

where $q_c = \pm q$ for holes and electrons, respectively, and $T_D^{\pm}(i)$ represents the electron/hole tunnelling rate between the drain and the QD when the number of electrons/holes in the QD changes from i to $i \pm 1$. Similarly, $T_S^{\pm}(i)$ describes the corresponding tunnel rate between the source and the QD. As already discussed, in nanoscale CMOS, the effective dimensions of the QD are typically in the sub-70 nm range leading to large spacing between the QD energy levels. At sufficiently low temperatures ($\Delta E_i > k_B T$), the total tunnelling rate to the QD can be expressed as [24], [25]

$$T_{S/D}^{\pm}(i) = \frac{\Gamma_{S/D}^{\pm}(i)}{1 + e^{\frac{-\Delta F_{S/D}(i)}{k_B T}}} \quad (8)$$

$\Gamma_{S/D}$ is the tunnel rate coefficient that depends on the tunnel matrix element and the density of states in the source/drain for the indicated charge transfer event. $\Delta F_{S/D}$ represents the change in energy of the system during the corresponding tunnelling event. Historically, the value of $\Delta F_{S/D}$ has been calculated using the constant interaction model [22], which describes the interaction between the QD and the device terminals using constant capacitance parameters. However, the assumption of constant capacitances does not hold for devices with thin gate oxides and spacer-defined energy barriers where the capacitances change with bias and number of electrons/holes in the QD [26]. In this work we propose the following piecewise description of $\Delta F(i)$, with lumped parameters $C_{G,i}$, $C_{D,i}$, $C_{S,i}$ and $C_{BG,i}$ representing the intrinsic capacitances between the QD and the gate, drain, source and back-gate terminals of the MOSFET, respectively, for the ith tunnelling peak:

$$\begin{aligned}\Delta F_S^-(i) &= -\Delta F_S^+(i-1) \\ &= \frac{q_c}{C_{tot,i}}\left[C_{D,i}V_{DS} + C_{G,i}\left(V_{GS} - V_{pk,i-1}\right) + Q(i)\right] \\ &\quad + |\Delta E_{i-1}| \end{aligned} \quad (9)$$

$$\begin{aligned}\Delta F_D^-(i) &= -\Delta F_D^+(i-1) \\ &= \frac{q_c}{C_{tot,i}}\left[-\left(C_{tot,i} - C_{D,i}\right)V_{DS} + C_{G,i}\left(V_{GS} - V_{pk,i-1}\right)\right. \\ &\qquad \left. + Q(i)\right] + |\Delta E_{i-1}| \end{aligned} \quad (10)$$

where

$$Q(i) = \begin{Bmatrix} 0 & i = 1 \\ q_c & i > 1 \end{Bmatrix}, \quad (11)$$

$$V_{pk,i} = V_{th} - \sum_{j=2}^{i}\left[\frac{q_c}{C_{G,j}} + \frac{C_{tot,j}}{C_{G,j}}\left(\frac{\Delta E_{j-1}}{q_c}\right)\right] \quad (12)$$

and

$$C_{tot,i} = C_{G,i} + C_{D,i} + C_{S,i} + C_{BG,i}. \quad (13)$$

$V_{pk,i}$ is defined as the V_{GS} value of the ith tunnelling current peak when biased at $|V_{DS}| \approx 0$ V. The first peak voltage, $V_{pk,1}$, can be considered the threshold voltage, V_{th}, of the SET/SHT. It is the gate voltage at which the first electron/hole enters and occupies the lowest energy level in the QD, creating charge inversion in the channel. While maintaining a simple linear form, (9) and (10) also account for the variation in capacitances and work reasonably well for approximating the measured tunnelling current characteristics. The magnitude of the tunnelling current is captured by the $\Gamma_{S/D}$ terms, which depend on the shape of the energy barrier in the source and drain tunnel junctions. The impact of the barrier height variation on I_{DS} is captured phenomenologically by making the following substitution:

$$I_i = q\frac{\Gamma_D(i)\Gamma_S(i-1)}{\Gamma_D(i) + \Gamma_S(i-1)} = 2I_{pk,i}e^{\beta_i(V_{GS} - V_{pk,i})} \quad (14)$$

where $I_{pk,i}$ and β_i are parameters extracted from measurements detailed in the next sub-section. $I_{pk,i}$ is the peak tunnelling current at the ith current peak. β captures the tunnelling current dependence around the ith peak on V_{GS}, which controls the height and shape of the potential barrier under the spacer. Using (7) - (14) and summing over all n-tunnelling events (i.e., all n electrons/holes which can be stored in the QD) while satisfying (6), the total tunnelling current in the device becomes

$$I_t = \sum_{i=1}^{n} \frac{I_i\left[1 - e^{\frac{q_C V_{DS}}{k_B T_{eff}}}\right]}{1 + e^{\frac{\Delta F_S^-(i)}{k_B T_{eff}}} + e^{\frac{-\Delta F_D^-(i)}{k_B T_{eff}}} + e^{\frac{q_C V_{DS}}{k_B T_{eff}}}}. \quad (15)$$

Here T_{eff} is the effective temperature, defined as

$$T_{eff} = \begin{cases} T & T > T_{sat} \\ T_{sat} & T \leq T_{sat} \end{cases} \quad (16)$$

T_{sat} is the temperature below which the half-width of the tunnelling current peak stops shrinking. The half-width saturation below 10 K can be clearly seen for both devices in Fig. 7. It is likely due to the finite width of the resonant tunnelling transmission window [27].

B. MODEL PARAMETER EXTRACTION

Extracting the complete set of model parameters (i.e., V_{th}, $C_{tot,i}$, $C_{G,i}$, $C_{D,i}$, $I_{pk,i}$, β_i and T_{sat}) requires measuring the transfer characteristics at multiple V_{DS} values. The value of ΔE_i is calculated using the analytical expression described in Section II. Fig. 8 shows the idealized and measured tunnelling current characteristics for a p-MOSFET along with the definition and extraction methodology for the model parameters. Ideally, two transfer characteristics measured at $|V_{DS}| \approx 0V$ ($|V_{DS}| = 1$ mV is used in this work) and $|V_{DS}| \geq \frac{6k_BT}{q}$ are sufficient to extract all parameters. However, it is recommended to use a larger number of bias points to minimize measurement uncertainty and extraction error.

At $|V_{DS}| \approx 0V$, peak tunnelling current, characterized by $\Delta F_S^- = \Delta F_D^- = 0$, depends only on C_G/C_{tot} as evident

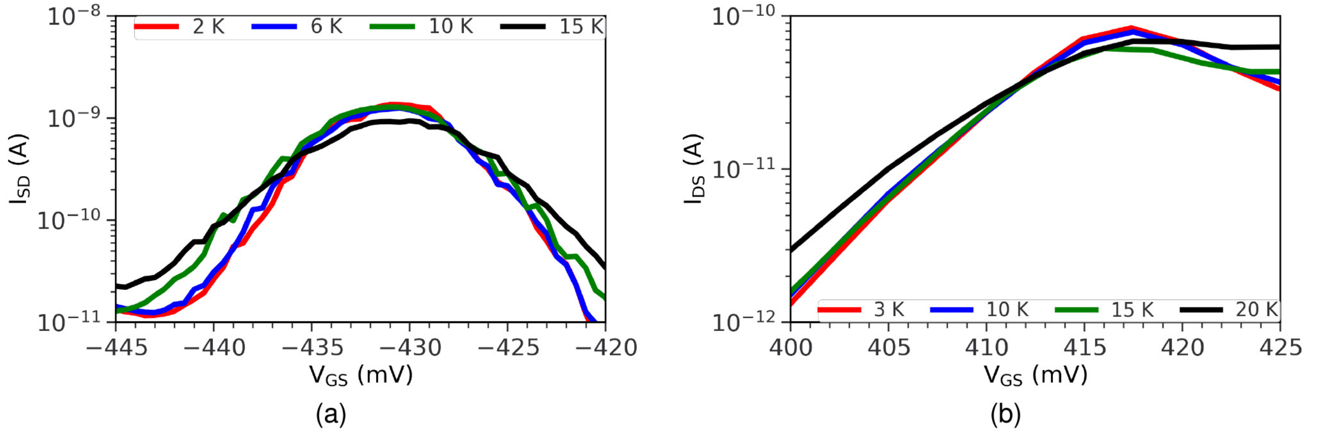

FIGURE 7. Measured transfer characteristics at the first tunnelling current peak as a function of temperature for the (a) *p*-MOSFET on die 2 (Fig. 11(b)) and (b) *n*-MOSFET on die 3 (Fig. 11(c)), each with 18 nm channel length and 70 nm channel width at $|V_{DS}| = 5$ mV. These figures illustrate the saturation of the half width of the tunnelling current peaks below a certain temperature, T_{sat}. The saturation temperature is 10 K and 6 K for the *n*-MOSFET and the *p*-MOSFET, respectively.

FIGURE 8. (a) Sample stability diagram (i.e., $I_{DS}(V_{DS}, V_{GS})$) of a *p*-MOSFET operating as a single hole transistor. Blue shaded diamond areas represent valley regions in the drain current. Extraction of s_1, s_2 and V_{pk} is illustrated graphically along with V_{th} defined as the V_{GS} value associated with the first current peak at $V_{DS} \approx 0$ (b) Measured stability diagram of a 18nmx70nm *p*-MOSFET showing extraction of $s_{1,1/2}$, $s_{2,1/2}$ and $V_{pk,1/2}$ at 6 K. (c) Sample Transfer characteristics with $\ln(I_{SD})$ shown on y-axis vs V_{GS} biased at $|V_{DS}| \geq \frac{6k_BT}{q}$. Extraction of I_{pk} and β is illustrated graphically on the figure (d) Measured transfer characteristics of the same 18nmx70nm *p*-MOSFET at $V_{DS} = -20/-30$ mV showing $I_{pk,1/2}$ and $\beta_{1/2}$ extraction.

from (9) and (10). In this limit, we can express $C_{G,i}$ as

$$C_{G,i} = \left| \frac{q_c}{\left(V_{pk,i} - V_{pk,(i-1)}\right) - \frac{(s_{2,i} - s_{1,i})}{s_{1,i} s_{2,i}} \frac{\Delta E_{i-1}}{q_c}} \right| \quad (17)$$

where $s_{1,i}$ and $s_{2,i}$ are the slopes of the boundary that demarcates the blockade region, as illustrated in Figs. 8(a) and 8(b). These values can be extracted from transfer characteristics at a minimum of two different V_{DS} values. The expression for

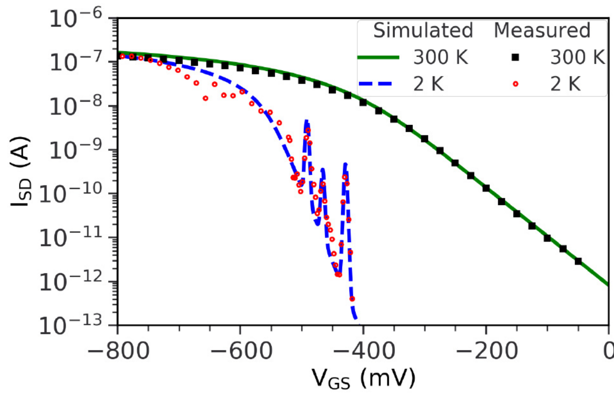

FIGURE 9. **Measured (symbols) and simulated (lines) transfer characteristics at V_{DS} = 1 mV at T = 2 K and 300 K for the 18nmx70nm *p*-MOSFET on die 2. Its model parameters are shown in column 2 of Table 1.**

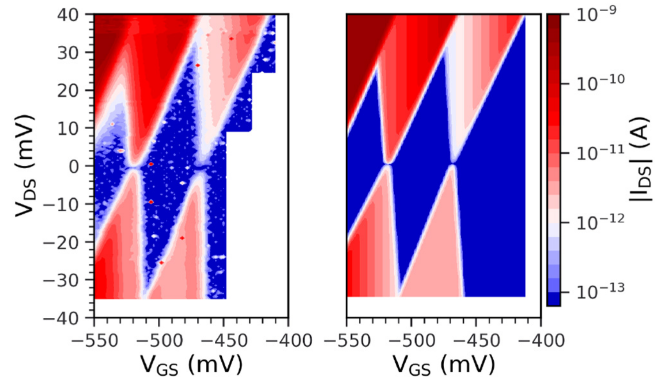

FIGURE 10. **Measured (left) and simulated (right) stability diagram of 18nmx70nm *p*-MOSFET on die 1 at 6 K [13]. Its model parameters are shown in column 1 of Table 1.**

$s_{1,i}$ and $s_{2,i}$ can be derived by taking the derivatives of (9) and (10) with respect to V_{DS} and equating both to zero:

$$C_{D,i} = \left|\frac{C_{G,i}}{s_{2,i}}\right| \tag{18}$$

$$C_{tot,i} = C_{G,i}\left|\frac{s_{2,i} - s_{1,i}}{s_{1,i}s_{2,i}}\right|. \tag{19}$$

All the capacitance parameters are obtained by solving (17)-(19) while $I_{pk,i}$ are extracted from the measured transfer characteristics in the triode region at relatively large $|V_{DS}|(\geq 6k_BT/q)$, as shown in Figs. 8(c) and 8(d). Parameters β_i are estimated from the slope of the ith peak of the transfer characteristic at $|V_{DS}| > (6k_BT)/q$ when plotted on a logarithmic scale, as shown in Fig. 8c.

Equation (17) cannot be used to find $C_{G,1}$ since $V_{pk,0}$ is undefined. Thus, to extract $C_{G,1}$, the approximation $C_{G,1} \approx C_{G,2}$ is applied. Similarly, the classical MOSFET diffusion current masks either one of the slopes s_1 or s_2 at the *n*-th (last) peak. Therefore, to extract the capacitances, it is assumed that $s_{1/2,n} \approx s_{1/2,n-1}$. T_{sat} can be extracted by measuring the transfer characteristics of the device at progressively lower temperatures until the half width of the first I_{DS} current peak ceases to change as the temperature is reduced, as shown in Figs. 7(a) and 7(b).

IV. MODEL VERIFICATION AND DISCUSSION

A. MODEL VERIFICATION

All measurements were conducted on-die with a Lake Shore Cryotronics CPX-VF-LT probe station in the 2 to 300 K range, using Keithley 4200A-SCS and Keysight B1500A semiconductor parameter analyzers. Silver paste with matched thermal expansion coefficient and high thermal/electrical conductivity was used to mount the dies on the sample holder. The power consumption of all devices in the bias range of interest for the applicability of the model is below 5 nW (I_{DS} < 1μA, V_{DS} < 5 mV) resulting in negligible self-heating. SHT and SET test structures were manufactured in three fabrication runs, across three different years, in GlobalFoundries' commercial 22FDX CMOS process [28]. Of these devices, seven single gate finger *p*-MOSFETs and two *n*-MOSFETs, each with a drawn gate length of 18 nm and drawn gate widths of 50 nm and 70 nm and with different numbers of dummy gates were measured for model extraction and to investigate the impact of the number of dummy gates on SET/SHT performance and model parameters. The $I - V$ characteristics of these devices were measured in the QD bias regime (subthreshold triode region) at cryogenic temperatures (<10 K) and model parameters were extracted using the methodology mentioned in the previous section. The QD model, coded in Verilog-A, was appended in a subcircuit to the standard foundry design kit MOSFET model, as illustrated in Fig. 5. Fig. 9 demonstrates the capability of the model to accurately capture the measured transfer characteristics at both 2 K and 300 K.

The extracted model parameters are summarized in Table 1 for one *n*-MOSFET and two *p*-MOSFETs with different number of dummy gate fingers. The latter is an attempt to investigate the impact of strain and to demonstrate the versatility of the model and parameter extraction methodology in monitoring strain and layout geometry variation and its impact on model parameters. Fig. 10 compares the measured and simulated stability diagram for the *p*-MOSFET on die 1, showing good accuracy across V_{GS} and V_{DS} values relevant for operation as a single-hole transistor (SHT) [13]. The measured and simulated transfer characteristics for the second *p*-MOSFET (die 2) and for the *n*-MOSFET are compiled in Fig. 11(b) and in Fig. 11(c), respectively, again showing good match in the subthreshold region where the devices operate as SHTs and SETs, respectively.

Figs. 12(a) and Fig. 12(b) demonstrate the accuracy of the model across temperature for a *p*-MOSFET and a *n*-MOSFET, respectively. It works reasonably well for all measured temperature values, even at elevated temperatures when $\Delta E < k_BT$ and where only weak SET/SHT behavior is observed.

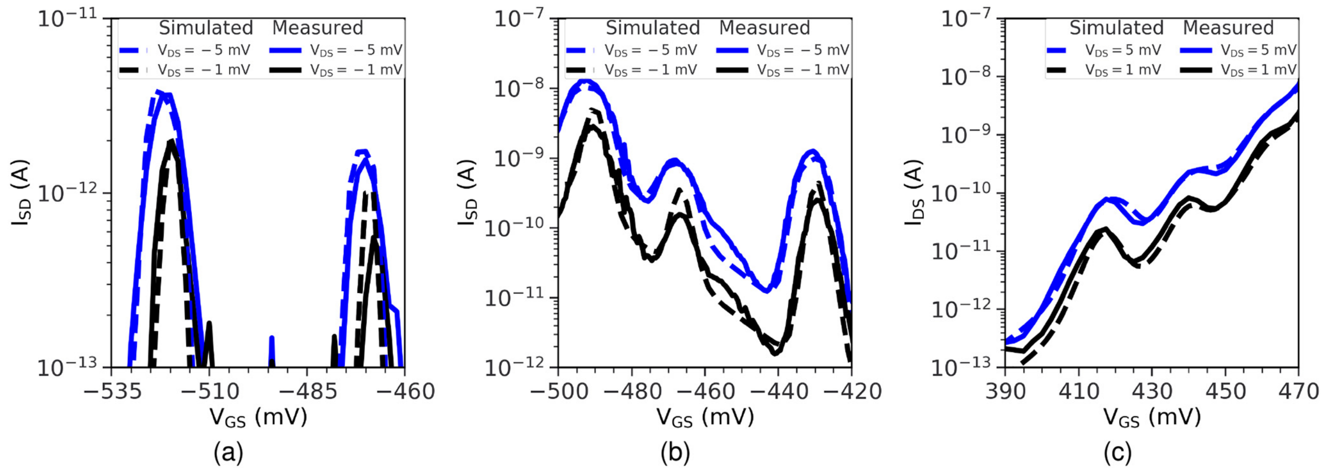

FIGURE 11. Measured (solid lines) and simulated (dashed lines) transfer characteristics at |VDS| = 1/5 mV for (a) 18nmx70nm p-MOSFET on die 1 (2 dummy gates) at 6 K (b) 18nmx70nm p-MOSFET on die 2 (6 dummy gates) at 6 K (c) 18nmx70nm n-MOSFET on die 3 (6 dummy gates) at 10 K.

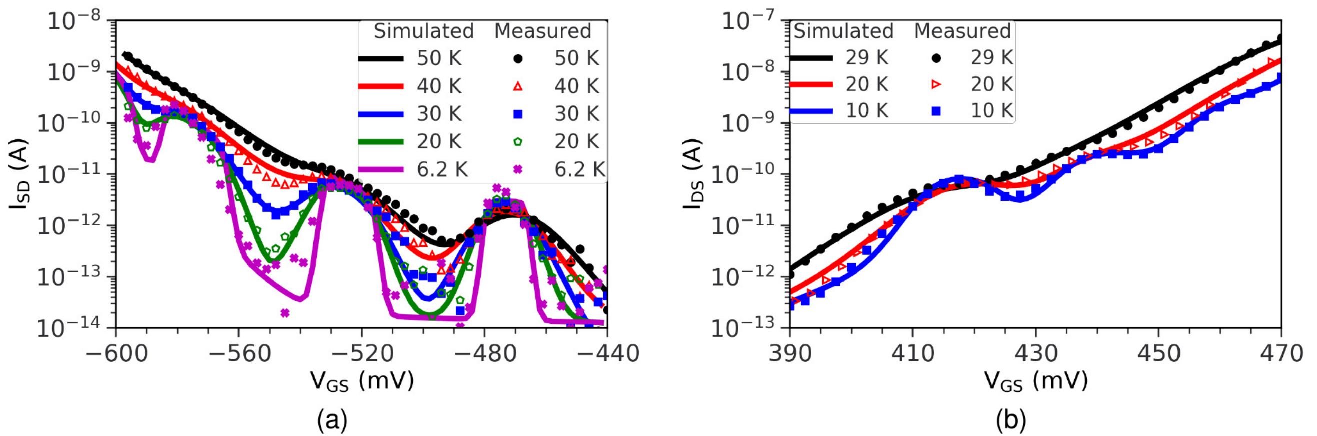

FIGURE 12. Measured (symbols) vs. simulated (lines) transfer characteristics across temperature for (a) 18nmx70nm *p*-MOSFET on die 1 biased at $V_{DS} = -10$ mV [13] and (b) 18nmx70nm *n*-MOSFET on die 2 biased at $V_{DS} = 5$ mV.

B. APPLICATION TO CHARGE READOUT CIRCUIT DESIGN

A promising, minimal-layout-footprint readout circuit for a linear qubit array consists of a parallel linear array of SETs or SHTs, each capacitively coupled to an individual qubit in the qubit array [28]–[30], followed by low-noise transimpedance amplification [12], [13], [31]. To that end, test structures consisting of two capacitively coupled SETs, as in Fig. 13, sharing the same floating back gate and placed at minimum distance (< 100 nm) from each other, were designed, fabricated and tested at 2 K. The structures mimic the capacitive coupling through the back-gate and through the STI region between one SET/SHT acting as the semiconductor qubit and the second SET/SHT acting as the charge readout SET/SHT. The measurements in Fig. 14 illustrate how the drain current of one SET changes when the number of electrons in the coupled SET changes from N to $N+1$. In this work, $V_{GS,A}$ was set to 470 mV and 510 mV to change the occupancy of SET A from N to $N+1$, respectively, at the first and second detected current peaks. Similar capacitively-coupled SET structures have been used for charge detection

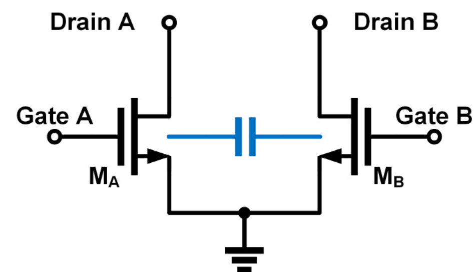

FIGURE 13. Schematic diagram of a test structure with two capacitively-coupled SETs, separated by 100 nm of STI, for charge readout measurements.

recently in [32]. As can be seen in Fig. 14, the sensitivity of the readout SET is a strong function of the bias point chosen for the readout SET. The highest sensitivity ≈4 nA is obtained when the readout SET is biased at the third tunneling current peak, when three electrons occupy its QD. This sets the design specification for the readout circuit scheme in Figs. 15 and 16. Fig. 17 shows the simulated transfer

TABLE 1. Extracted model parameters.

Model Parameters	p-MOSFET 18nmx70nm		n-MOSFET 18nmx70nm
	die 1 2 DG	die 2 6 DG	die 3 6 DG
V_{th} (mV)	-468	-428	416
$C_{G,1}$ (aF)	3.2	4.3	6.9
$C_{G,2}$ (aF)	3.2	4.3	6.9
$C_{G,3}$ (aF)	3.7	8	8
$C_{D,1}$ (aF)	0.6/0.6*	1	4
$C_{D,2}$ (aF)	0.7/0.7*	1.2	4.2
$C_{D,3}$ (aF)	0.8/0.8*	2.5	6
$C_{tot,1}$ (aF)	4.3/4.8*	7.5	14
$C_{tot,2}$ (aF)	5.12/4.8*	8.2	14.5
$C_{tot,3}$ (aF)	7/5.6*	15	20
$I_{pk,1}$ (nA)	0.0029/0.00085*	1.25	0.09
$I_{pk,2}$ (nA)	0.0037/0.011*	0.9	0.2
$I_{pk,3}$ (nA)	0.00033/0.475*	17.5	4
β_1 (V^{-1})	5.2/-70*	–	–
β_2 (V^{-1})	80/-56*	–	–
β_3 (V^{-1})	100/0*	–	–
ΔE_1 (meV)	2.88	2.88	1.15
T_{sat} (K)	6	6	10

* = values indicated of negative/positive V_{DS}
DG = No. of dummy gates

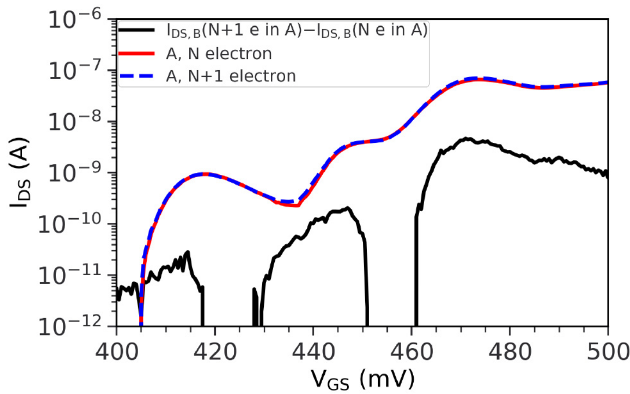

FIGURE 14. Measured transfer characteristics of one of the SETs (SET B) in Fig. 13 when the number of electrons in the second SET (SET A) changes from N (solid red) to $N+1$ (dashed blue) at $T = 2$ K. The difference between these currents is shown (solid black). Both SETs are biased at $V_{DS} = 5$ mV and the back-gate is floating.

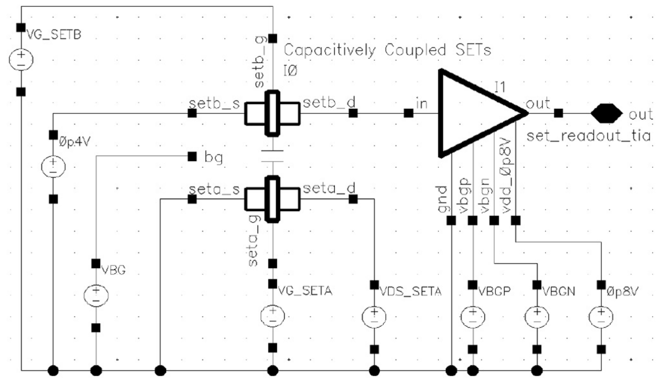

FIGURE 15. Simulation testbench of a system with capacitively coupled SETs and TIA.

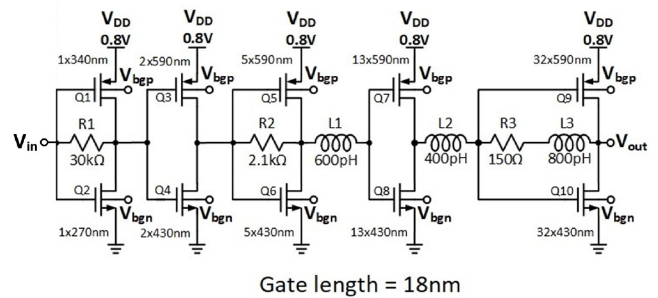

FIGURE 16. Transistor level schematic of the readout TIA [31].

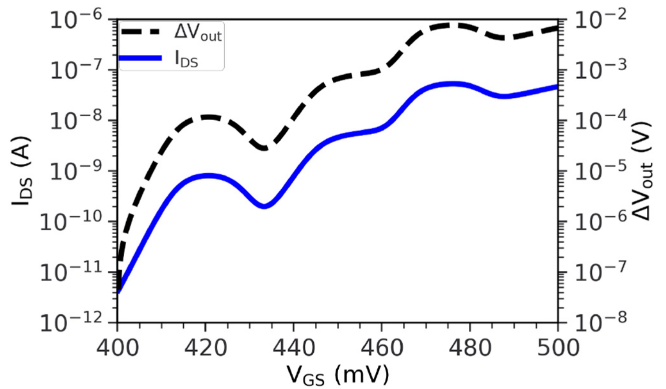

FIGURE 17. Simulated transfer characteristics of a readout SET (SET B in Fig. 14) at 2 K when biased at $V_{DS} = 5$ mV amplified by a cryogenic TIA [31] monolithically integrated with the SET.

characteristics of the SET amplified by the TIA demonstrating how the proposed model can be applied in the design of a semiconductor spin qubit monolithic quantum processor with integrated readout and control electronics.

C. DISCUSSION

As shown in Fig. 3, for devices with identical layouts fabricated on the same die, the variation of the intrinsic gate capacitance C_G is less than 13% and the V_{th} variation between SLVTP SHTs is about 12 mV, comparable to the threshold voltage variation observed in minimum size MOSFETs at room temperature. This variation in the V_{th} can be corrected by changing the back-gate voltage as shown in Fig. 4. More importantly, measurements of the SLVTP and SLVTP_TL devices in Fig. 3 prove that the intrinsic gate capacitance does not depend on the metal parasitics connected to the gate. However, variation in the value of the tunnel current peaks can be observed between devices with different number of dummy gates and, as mentioned, for a given device as the back-gate voltage is changed (Fig. 4). This is also reflected in variations observed in the extracted values of C_D in Table 1. It can be seen that the effective width of the potential barriers is different in all devices and it changes with bias, especially back-gate voltage. However, the peak voltage ($V_{pk,i}$) values remain unchanged for a fixed back-gate voltage. These effects are not yet fully understood

given the good V_t control exhibited by these devices even at 2 K. Work is underway using Ab initio simulations [33] to understand this observation and will be the subject of a later publication.

Variability in the I-V characteristics of individual SET/SHT devices can be accounted for in the circuit design process by allowing the model parameters to vary randomly within a specified range. Furthermore, based on the authors' limited number of experiments, this inevitable variability [32] can be reduced by forming SET/SHT devices as part of a larger active area array with tens of gate fingers. The latter arrangement is representative of the most likely application scenario where a large array of SETs/SHTs, all sharing the same active region, is placed parallel at 50-100 nm distance from a large array of hole-spin or electron-spin qubits, as recently demonstrated in [32].

The current model relies on parameters extracted directly from measurements. Systematic experimental- and simulation-based studies are needed to link the model parameters to the structural and material properties of the device. In particular, the parameters I_{pk}, β and C_D are linked to the height and width of the potential barriers formed below the gate oxide spacers. They change as a function of bias and spacer width. Similarly, C_G should be expressed as a function of the top gate oxide area, thickness, and quantum capacitance which changes with the effective mass of the electron/hole. Furthermore, additional work is required to capture the effect of V_{BG} on the transfer characteristics. V_{BG} modifies the threshold voltage and the potential barriers, leading to a change in capacitance parameters and peak tunnelling current.

V. CONCLUSION

A compact model was developed which adds a tunnelling component to the classical $I-V$ characteristics of the foundry MOSFET model. The proposed model and the associated model parameter extraction methodology were validated using detailed cryogenic measurements of *p*-MOSFETs and *n*-MOSFETs fabricated in a production 22nm FDSOI foundry process. The model reproduced the DC $I-V$ characteristics across bias and temperature for *n*- and *p*-type devices with different number of dummy gates and channel strain with reasonable accuracy. The quantum effects captured by the proposed model are expected to manifest at progressively higher temperatures as the device dimensions are scaled-down and, hence, will become increasingly important for more aggressively scaled technology nodes. Furthermore, the work also marks a first step towards the development of a complete simulation environment for the design and optimization of monolithic quantum processors.

ACKNOWLEDGMENT

The authors wish to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program and Dr. Nigel Cave for discussions on technology features and options. They would also like to acknowledge CMC for CAD tools and Jaro Pristupa for CAD support.

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