Amorphous IGZO Thin-Film Transistor Gate Driver in Array for Ultra-Narrow Border Displays

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ABSTRACT A gate driver in array (GIA) design based on the amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) is developed for narrow border displays. In the design, each TFT in the gate driver circuits is divided into a certain number of smaller size devices, which can be placed in different subpixels. Therefore, the pixel aperture ratio loss is minimized, and uniform placement of the gate driver circuits over the pixel array area is able to be achieved. The proposed step-like repeating block structure further reduces the occupied area of the signal interconnects. A 12.4-inch fringe field switching (FFS) liquid crystal display (LCD) panel of ultra-narrow border (0.5 mm) is demonstrated with reliable operation based on this GIA design, proving its potential for practical applications.

INDEX TERMS Display, narrow border, indium gallium zinc oxide, thin-film transistor, gate driver on array, gate driver in array.

I. INTRODUCTION

In advanced flat panel displays, the peripheral gate drivers are normally implemented in thin film transistor (TFT) technologies, and integrated onto the same substrate with the active pixel array. The so-called gate driver on array (GOA) technology eliminates connection of external gate driver chips and can thus help to make compact display panels of slim bezel, high yield and low system cost [1]–[4].

In recent years, the amorphous indium gallium zinc oxide (a-IGZO) TFT technology has been extensively studied for display backplanes, owing to relatively high mobility, extremely low leakage current, and large-area manufacturing capability with low thermal budget [5]–[7]. However, the a-IGZO TFTs still suffer operational instability issues under light illumination and electrical bias stress [8]–[10]. Their depletion-mode characteristics cause large leakage current at zero gate-to-source bias voltage, which makes design of low

power and reliable GOA circuits challenging. As a result, to avoid circuit deterioration and malfunction and reduce power consumption, complex circuit designs are developed to compensate influence of device performance instability and suppress the leakage current [11]–[14].

With the normal GOA architectures, the gate driver circuits are placed at both sides of the pixel array area, as shown in Fig. 1(a). As the display resolution increases, boarder areas are required for the GOA layout, and thus the bezel size is difficult to be further reduced. To overcome such a limit of reducing bezel size, a new architecture design by integrating gate driver circuits into the pixel array (gate-driver-in-array, GIA) is implemented [15], [16]. However, the used simple circuit designs are not able to support reliable operation in practical display panels. Moreover, it is a challenge to achieve optimal layout placement of the gate driver circuits into the active array without affecting the display quality.
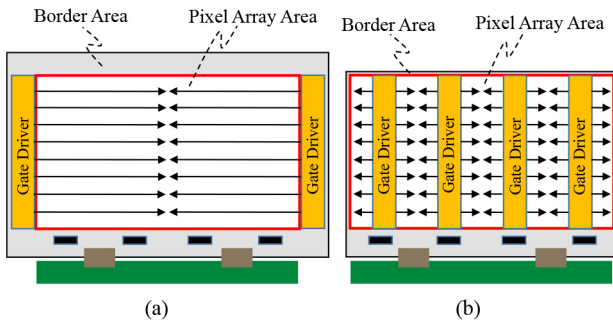
FIGURE 1. Illustration of two gate driver integration architectures for displays: (a) the gate driver on array (GOA), placing the gate driver circuits at both sides of the pixel array, and (b) the gate driver in array (GIA), integrating the gate driver circuits into the pixel array.
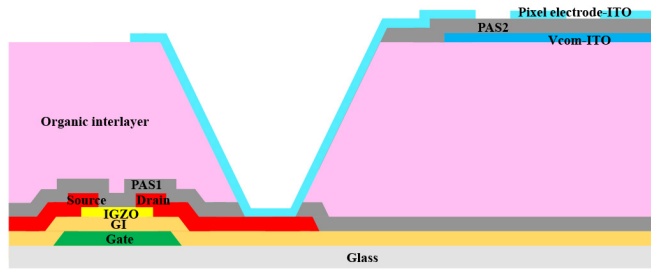

FIGURE 2. The cross-sectional structure of the back-channel etched (BCE) a-IGZO TFT backplane used in this work.

In this work, a four-clock controlled gate driver circuit with 8 TFTs in each stage is designed and integrated in the active array area based on a back-channel etched (BCE) structure a-IGZO TFT. To minimize the pixel aperture ratio loss and achieve uniformity of placement, each gate driver TFT is divided into a certain number of small TFTs, which are embedded in different subpixels. A step-like repeating block structure is designed to further reduce the occupied area of the signal interconnects. Implementation of the a-IGZO TFTs in smaller dimensions can also improve the operational stability. With such a GIA integration, a 12.4 inch nearly-bezel-free high-resolution liquid crystal display (LCD) panel is finally demonstrated.

II. DEVICE TECHNOLOGY
The IGZO TFT can be manufactured in an etch stopper (E/S) structure or a back-channel etched (BCE) structure. Although the E/S structure is able to protect the back-channel of IGZO from the influence of the following fabrication process, it has inherent drawbacks such as large parasitic capacitance, long channel length and more mask steps [7]. Therefore, the BCE structure has been widely used for its capability for small TFT size, low manufacturing cost and also small parasitic capacitance. Fig. 2 illustrates the cross-sectional structure of the BCE a-IGZO TFT backplane in this work, which was fabricated using an 8-mask process flow on a Gen-6 size glass substrate (1800 mm×1500 mm). The gate, source and drain electrodes are made of titanium/copper (Ti/Cu) metal
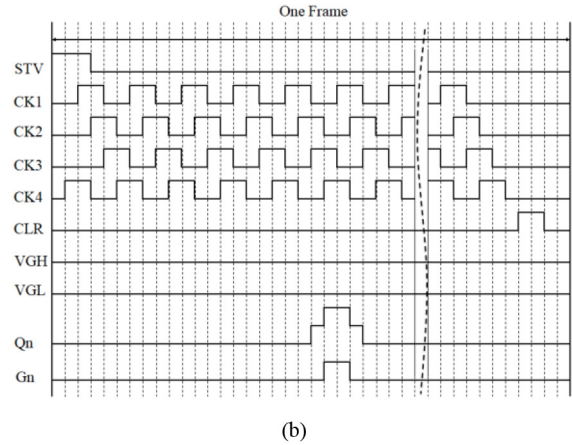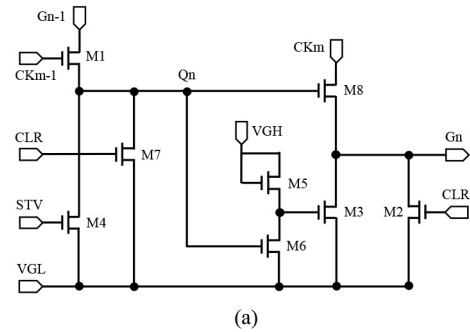

FIGURE 3. (a) Schematic of the gate driver circuit design being integrated within the pixel array area. (b) Timing diagram of the control signals.

layers, and the gate insulator (GI) is of a SiN_x/SiO_2 bi-layer structure. The a-IGZO active channel layer is deposited though DC sputtering. A thick organic interlayer was formed on top of the SiO_2/SiN_x passivation layer for subsequent pixel electrode integration with small parasitic capacitance. Both V_{COM} and pixel electrodes were made of transparent conductor (indium-tin oxide, ITO). The typical values of the extracted threshold voltage, mobility, and subthreshold swing (SS) of the a-IGZO TFT at room temperature are 1.93 V, 8.5 cm^2/V·s and 0.27 V/dec, respectively. The fringe field switching (FFS) liquid crystal mode was adopted in the study, attributed to its wide viewing angle, high contrast ratio, minimized color shift, fast response, and minimized Mura.

III. GATE DRIVER CIRCUIT DESIGN
Figure 3(a) shows the gate driver circuit design being integrated within the pixel array area. The circuit of one stage consists of eight a-IGZO TFTs (M1-M8), with operation being controlled by two pulse signals (STV, CLR), four clock signals (CK1, CK2, CK3, CK4), and two-level DC voltage (VGH, VGL), as shown in Fig. 3(b). Gn represents the nth stage output. Compared to the simple 2-clock design, the 4-clock scheme is able to reduce the capacitive load, enhance the pixel charging capability through doubling the high voltage pulse period, and suppress the signal ripple issue.

The operation of the proposed gate driver circuit consists of the following six periods:

1) *Pre-charge Qn:* CKm-1 rises from VGL to VGH to turn on M1, and the signal on the previous gate line pre-charges the Q(n) from VGL to VGH. M6 is gradually opened, leading to turn-off of M3. At the same time, M8 is turned on and Gn outputs a voltage level of VGL, since CKm is VGL.

2) *Pull-up Gn:* CKm switches from VGL to VGH, and the voltage at Qn is bootstrapped to about two times of VGH. In turn, the driving capability of M8 is enhanced to charge Gn to the level of VGH. Meanwhile, Gn output of this stage pre-charges the Qn+1 of the next stage through the inter-stage transmission circuit.

3) *Pull-down Gn:* CKm falls from VGH to VGL, and Gn is pulled-down to VGL through M8. In the meantime, Qn is still at a high voltage level.

4) *Pull-down Qn:* CKm-1 changes from VGL to VGH to turn on M1, and Qn is discharged to VGL through M1 (Gn-1 is VGL).

5) *Maintain Gn:* Qn is kept at the level of VGL, and M6 is turned off. M5 and M3 are turned on to maintain the low level (VGL) at Gn. Therefore, M3, M5 and M6 form low-level holding to ensure stable Gn output waveforms.

6) *Reset:* Before the end of each frame, a high-level pulse at CLR turns on M2 and M7 to reset Gn and Qn for elimination of the residual charges.

IV. LAYOUT PLACEMENT FOR IN-ARRAY INTEGRATION

In the conventional design, the gate driver circuits are located in the border area of the display panel, and thus require sufficient space on both sides of the pixel array area depending on the panel size and resolution. Integration of the gate driver circuits into the pixel array area can minimize the border size. However, the layout design needs to minimize the pixel aperture ratio loss, and additional crossover with the data lines in the array, which might result in excessive parasitic capacitance load on the panel. Moreover, the circuit components and interconnects should be uniformly placed over the pixel array area to avoid non-uniformity induced display non-idealities.

As shown in Fig. 4, each stage of the gate driver is distributed over many pixels. The main signal interconnects in the gate driver circuits are designed to be parallel to the data lines, so that crossover is able to be avoided. All the TFTs and the signal interconnects in the gate driver circuit are implemented in the blue sub-pixels, as shown in Fig. 5. As a result, the blue pixel includes a vertical data line and CK line, a horizontal gate line and Qn line and two TFTs, one for pixel charging and the other for the gate driver circuit. The TFTs in the gate driver are normally much larger than that of the pixel switch TFT. To minimize the pixel aperture ratio loss and achieve uniformity of placement, each gate driver TFT is divided into a certain number of small TFTs, which have similar sizes to that of the pixel switch
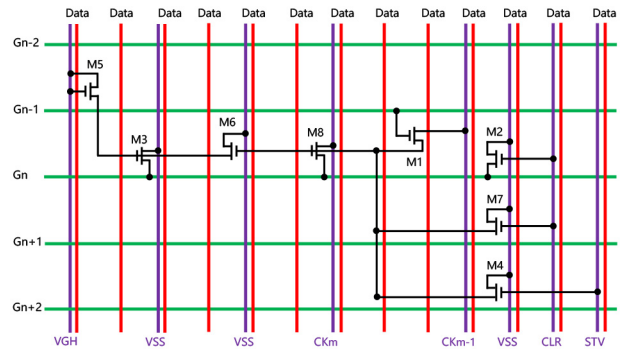

FIGURE 4. Illustration of the components in the gate driver circuit being placed over many pixels for GIA integration.
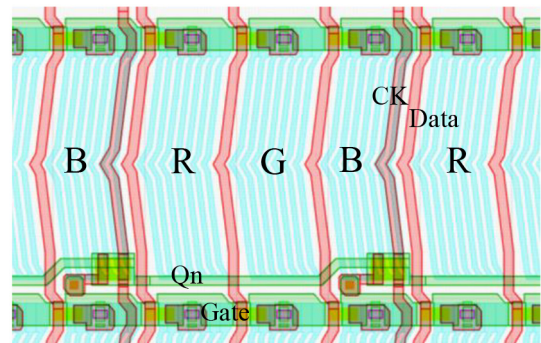

FIGURE 5. Layout design showing placement of the TFTs and the signal interconnects of the gate driver circuit in the sub-pixels.

TABLE 1. Sizing of the TFTs in the gate driver circuit and the decomposed unit devices placed in sub-pixels.

TFTs	M1	M2	M3	M4	M5	M6	M7	M8
Overall size*	144/6	144/6	432/6	144/6	48/13	432/6	144/6	1440/6
Unit size*	12/6	12/6	12/6	12/6	4/13	12/6	12/6	12/6

*The size values are of channel width/channel length in μm.

TFT and are embedded in several subpixels as shown in Table 1. For example, the bootstrap TFT M8 of the largest size (W/L = 1440 μm/6 μm) is divided into 120 small devices (W/L = 12 μm/6 μm) and integrated into 120 blue subpixels.

In order to further minimize the occupied area of the signal interconnects in each sub-pixel and the crossover, a step-like repeating block structure is designed, as illustrated in Fig. 6. Each block occupies 20 pixels in column and 4 pixels in row, and 4 adjacent blocks generate 4 rows of gate line signals (Gn-1, Gn, Gn+1 and Gn+2). All blocks are closely packed to form the whole gate driver in the pixel array area.

Implementation of the a-IGZO TFT gate driver into the pixel array area with small dimension devices can also help to improve the operational stability. Small threshold voltage (V_th) variation of a-IGZO TFTs induced by processes or long-term operation might result in performance deterioration of the gate driver circuits. Fig. 7(a) and (b) shows the measured transfer characteristics (I_D-V_GS) of a-IGZO TFT under a typical positive bias stress (PBS) at V_GS of 25 V and
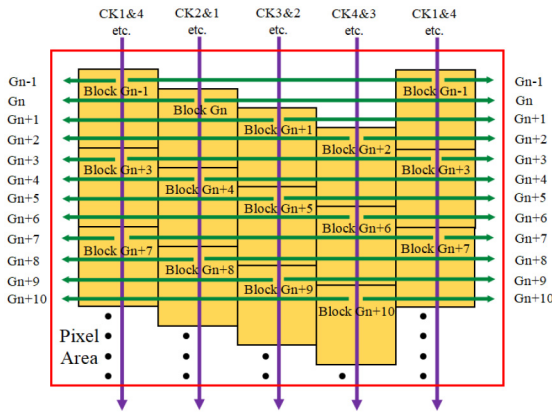
FIGURE 6. Illustration of the step-like repeating block structure for the GIA integration.
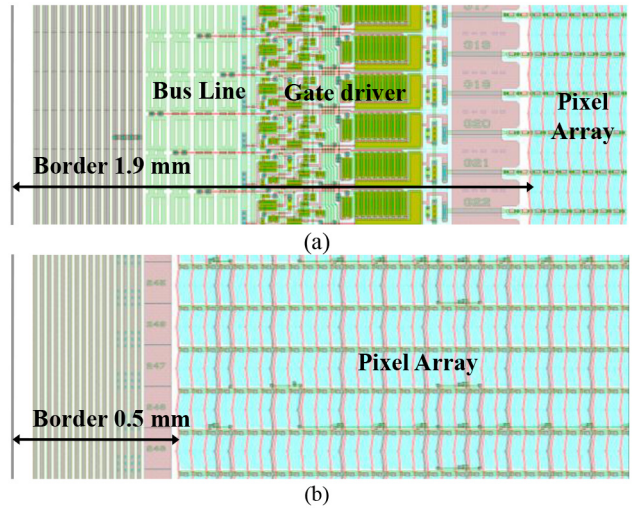

FIGURE 7. Comparison of the positive bias stress (PBS) stability of the narrow (20 μm/6 μm) and wide (1000 μm/6 μm) a-IGZO TFTs: (a) The measured transfer characteristics (I_D-V_{GS}) under PBS for 7200 s and (b) the extracted threshold voltage shift (ΔV_{th}) over PBS of 7200 s.

FIGURE 8. The layout images of (a) the conventional GOA design and (b) the GIA design in this work based on the a-IGZO TFT.
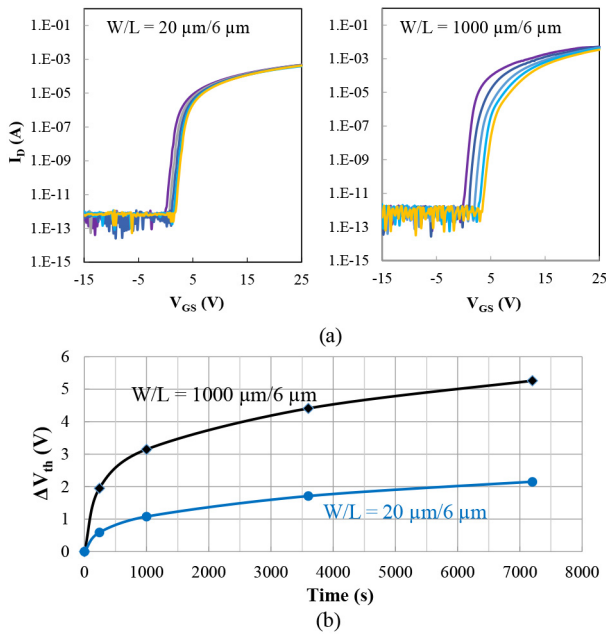

FIGURE 9. Photo image of the fabricated 12.4-inch nearly-bezel-free LCD panel based on the GIA integration.

TABLE 2. Specifications of the fabricated FFS LCD panel with a-IGZO TFT GIA integration.

Specification	Value
Diagonal Size	12.4 inch
Resolution	1920 (RGB) × 720
Pixel Pitch	156 μm x 156 μm
Border Size	0.5/0.5/0.5/6.4 mm (L/R/U/D)

V_{DS} of 10 V. The extracted V_{th} shifts (ΔV_{th}) over the stress time under PBS are given in Fig. 7(c). It can be observed that TFT with larger channel width (W) shows larger ΔV_{th} over time. For smaller size TFTs, the heating induced by current stressing is easier to be dissipated, and thus better PBS stability is able to be achieved [17]–[19]. Therefore, using smaller size TFTs, the proposed gate driver in array design is able to achieve better operation stability.

V. RESULTS AND DISCUSSIONS

Fig. 8 compares the layout of the conventional a-IGZO TFT gate driver design and the proposed design for a 12.4-in LCD panel of 1920 (RGB)×642 pixels. It can be seen that the total border width can be significantly decreased from 1.9 mm to 0.5 mm with the proposed design. The pixel aperture ratio of red and green subpixels is slightly reduced from 71.6% to 69.2%, respectively. Since the clock line are placed in the blue subpixel, its aperture ratio is reduced to 61.8%. The fabricated 12.4-inch nearly-bezel-free LCD panel is shown in Fig. 9. Its main specifications are listed in Table 2.

To verify the reliability, standard aging tests were carried out for the whole LCD panel, including storage at high temperature (70°C) and low temperature (−20°C) for 500 hours, operation at high temperature (60°C) and low temperature (−20°C) for 500 hours, operation at high temperature (60°C) and high humidity (RH of 90%) for 500 hours, being turned ON/OFF for 30000 cycles. After all the reliability tests, the display can work normally without any deterioration and malfunction. Fig. 10 shows the measured output waveforms
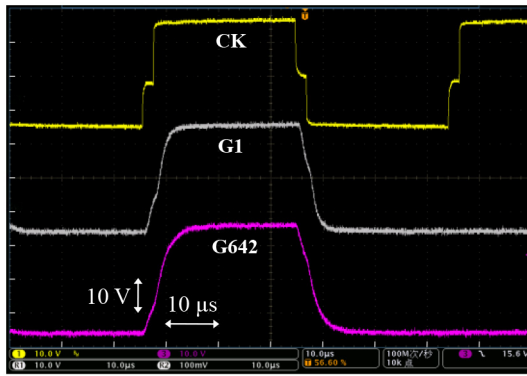
FIGURE 10. The measured output waveforms at the first and last stage gate line of the fabricated 12.4-inch LCD panel.

of the first and last gate line after the reliability tests, indicating proper operation of the a-IGZO gate driver and good enough operational stability.

VI. CONCLUSION

A gate driver in array (GIA) design based on the BCE structure a-IGZO TFT is developed for narrow border displays. In the design, each TFT in the gate driver circuits is divided into a certain number of small TFTs, which are integrated in different subpixels. Therefore, the pixel aperture ratio loss is minimized, and uniform placement of the gate driver circuits over the pixel array area is able to be achieved. The proposed step-like repeating block structure further reduces the occupied area of the signal interconnects. A 12.4 inch FFS LCD panel of ultra-narrow border (0.5 mm) is demonstrated based on this GIA design, proving its potential for practical applications. Although the GIA design might increase crossovers in the array and in turn result in slight increase of the gate line delay, the influence on pixel charging can be suppressed with optimal design based on the high mobility AOS TFT. This technology would be a universal approach for all state-of-the-art flat-panel displays, including organic light emitting diode (OLED) displays, e-paper and micro-LED displays.

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