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Improving the Scalability of Ferroelectric FET Nonvolatile Memories With High-k Spacers

YOU-SHENG LIU AND PIN SU (Member, IEEE)

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan

CORRESPONDING AUTHOR: P. SU (e-mail: pinsu@faculty.nctu.edu.tw)

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ABSTRACT This paper investigates scaled ferroelectric field-effect transistor (FeFET) nonvolatile memories (NVMs) with high-k spacer device design considering ferroelectric-dielectric random phase variations with TCAD atomistic simulations. Our study indicates that, in addition to raising the orthorhombic phase and reducing the grain size of the ferroelectric, using high-k spacers can serve as another way to enhance the scalability of FeFETs because it improves both the mean memory window (MW) and the worst-case MW. More importantly, these improvements increase with the down-scaling of gate length. In addition, we have investigated the impact of high-k spacers on the critical electric field across interfacial layer (E_{IL}) for the reliability of FeFET NVMs. Our study suggests that, for scaled FeFETs with high-k spacers, the highest E_{IL} during write operation is no longer located near the S/D edge but at the mid channel. Using high-k spacers can reduce the mid-channel E_{IL}, and the reduction increases with decreasing gate length due to the increasing impact of high-k spacers. Our study may provide insights for future high-density FeFET design.

INDEX TERMS Ferroelectric field-effect transistor (FeFET), memory window (MW), nonvolatile memory (NVM).

I. INTRODUCTION

With a CMOS-compatible HfO2-based ferroelectric, the ferroelectric FET (FeFET) has garnered substantial interest as a candidate for next-generation nonvolatile memory (NVM) [1]–[3], and the FeFET NVM integrated into leading-edge logic technology has also been demonstrated [4], [5]. For future high-density integration, the scalability of the FeFET is an important issue [2], [6]. Especially, the ferroelectric (FE) orthorhombic phase (O-phase) is not uniformly distributed and there exists cubic and monoclinic phases that may form dielectric (DE) [7], [8]. The random FE-DE phase distribution may seriously reduce the memory window (MW) of the FeFET NVM due to the forming of the DE leakage path from source to drain (see Fig. 1(c)) [9], posing a challenge to the gate-length scaling of the FeFET.

In addition, mitigating the electric field across the interfacial layer (E_{IL}) is crucial to the reliability of the FeFET. High E_{IL} from high write pulses increases the probability of trapped charge injection and IL breakdown [10], [11]. In this paper, with the aid of TCAD atomistic simulations, we demonstrate that high-k spacer device design can be used to improve the scalability of the FeFET NVM considering the ferroelectric phase non-uniformity. We also investigate the impact of high-k spacers on the E_{IL}.

This paper is organized as follows. In Section II, our simulation methodology is described. In Section III, we investigate the impact of high-k spacers on the scalability of FeFET NVMs assuming a nonuniform ferroelectric with FE-DE phase distribution. In Section IV, the impact of high-k spacers on the E_{IL} will be examined. The conclusion will be drawn in Section V.

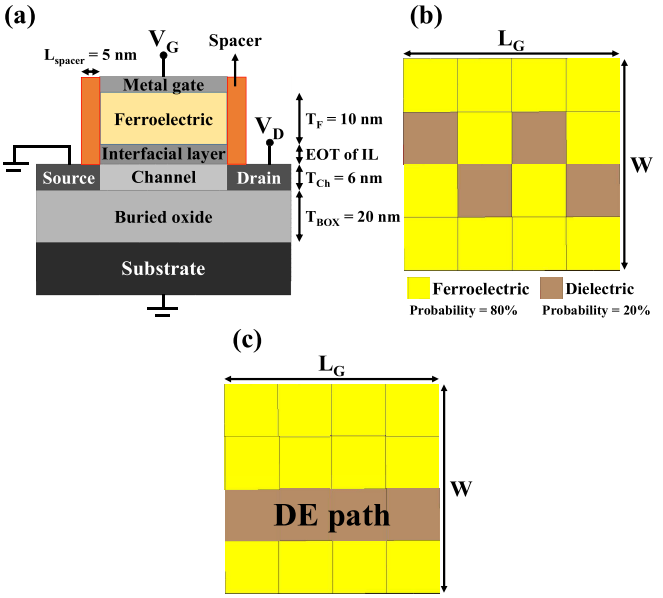

FIGURE 1. **(a) Schematic of the ultra-thin-body SOI FeFET in this study. The impacts of spacers on the FeFET NVM are investigated. (b) An instance of the ferroelectric-dielectric grain pattern. It is assumed that each grain has an 80% probability to be FE and a 20% probability to be DE. (c) An instance of the FE-DE grain pattern showing the forming of the DE leakage path from source to drain. L_G: gate length. W: gate width.**

II. SIMULATION METHODOLOGY

Fig. 1(a) shows the schematic of the FeFET device structure in this study. For the FeFET with spacer design, the spacer dielectric constant k = 30 and the spacer length L_{spacer} = 5 nm are assumed. Pertinent ferroelectric parameters used are remnant polarization $P_r = 20\ \mu C/cm^2$, saturated polarization $P_s = 23\ \mu C/cm^2$, and coercive electric field E_C = 1.5 MV/cm [10]. The equivalent interfacial-layer thickness (EOT of IL) = 0.8 nm unless otherwise specified. In TCAD simulation [12], we use square grains (see Fig. 1(b)) to capture the random FE-DE phase distribution effect. As each grain has a certain probability to be DE, the number of FE grains in each device instance is a variable. In addition, the random patterns of FE-DE grains (e.g., Fig. 1(b)) result in position fluctuations [9]. In this work, unless otherwise specified, 6 nm grain size and O-phase (FE) probability = 80% are assumed.

Regarding the operation of the FeFET NVM, we apply square gate pulses. The pulse magnitudes (V_W) are −4 V and 4 V in writing operation for high-V_{th} state and low-V_{th} state, respectively. We obtain I_D-V_G curves by sweeping gate bias (V_G) under 0.05 V drain bias (V_D) during reading operation. The MW can be extracted from the dispersive I-V curves at constant current condition ($I_D = 10^{-7} \times W/L_G$ (A)) during reading operation. Both read/write operations are simulated based on the Preisach model [12], [13].

III. IMPACT OF HIGH-K SPACERS ON THE SCALABILITY OF FEFETS CONSIDERING PHASE NON-UNIFORMITY

Fig. 2(a) shows the ideal and dispersive I_D-V_G curves considering the random FE-DE phase distribution for

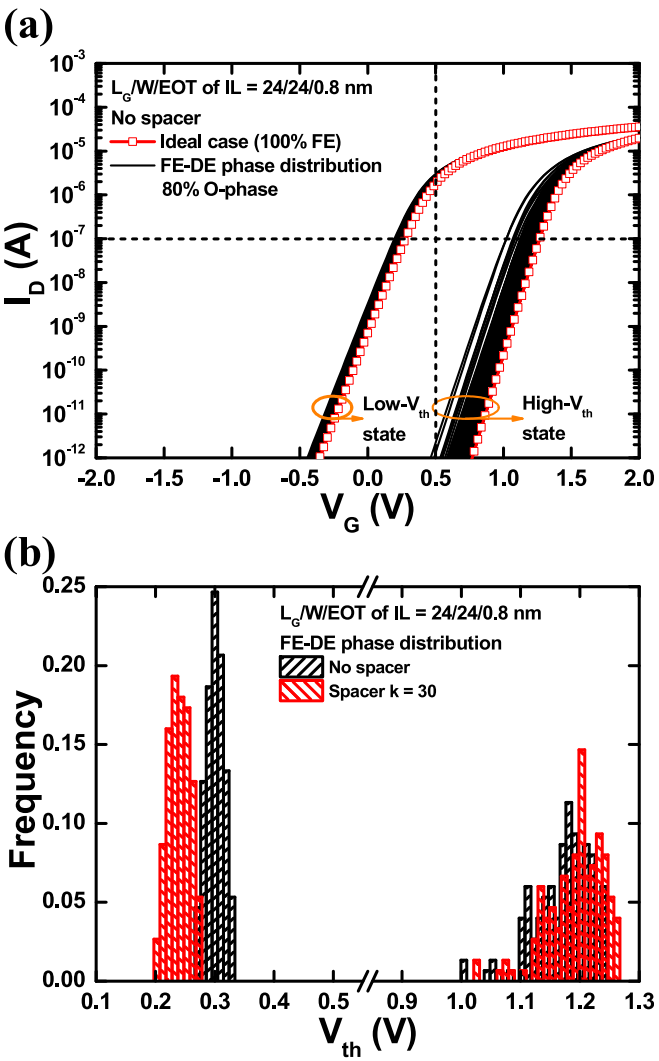

FIGURE 2. **(a) I-V dispersions for both high-V_{th} and low-V_{th} states of 150 FeFET devices for L_G/W/EOT of IL = 24 nm/24 nm/0.8 nm without spacer design. The MW can be extracted from the difference of the threshold voltages ($V_{th,high}$ and $V_{th,low}$) at $I_D = 10^{-7} \times W/L_G$ (A). (b) V_{th} distributions of the two states due to number and position fluctuations of the FE-DE grains with and without high-k spacers.**

150 FeFET device instances (L_G/W = 24 nm/24 nm) without spacers during reading operation. Compared with the ideal case (100% FE), significant I-V dispersion can be seen. Especially, Fig. 2(b) shows that the high-V_{th} distribution is strongly skewed towards lower V_{th} because of the FE-DE phase variation. The worst-case tail (around 1.0 V) occurs as the DE grains form a leakage path between source and drain. The electron current density under the DE path is much larger than that under the FE grains under the high-V_{th} (OFF) state, leading to reduced V_{th}. The worst-case high-V_{th} tail corresponds to the tail in the MW distribution shown in Fig. 3(a).

Fig. 2(b) also shows the impact of high-k spacers on the V_{th} distributions of the FeFETs. Compared with the V_{th} distributions for FeFETs without spacers, the low-V_{th} distribution for FeFETs with high-k spacers has a leftward

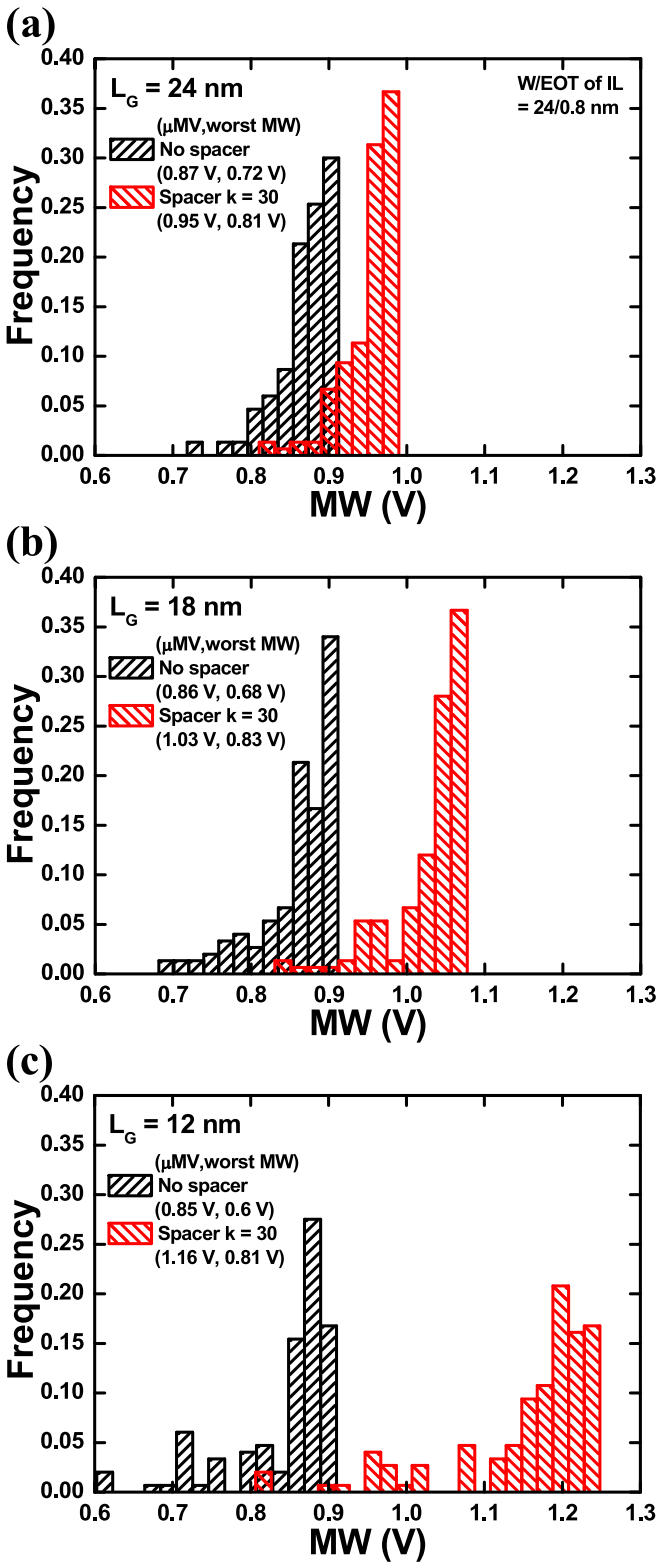

FIGURE 3. Impact of high-k spacers on the MW distributions considering the FE-DE phase variation for FeFETs with L_G = (a) 24, (b) 18 and (c) 12 nm. The impact of high-k spacers increases with decreasing L_G.

shift, while the high-V_{th} distribution with high-k spacers has a rightward shift, resulting in increased MW as shown in Fig. 3(a).

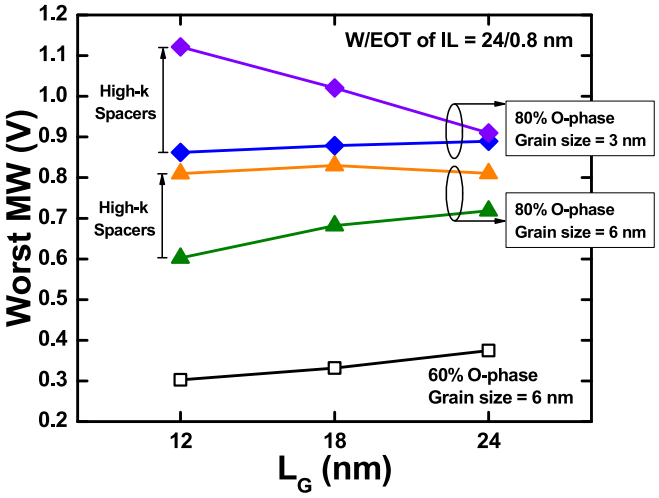

FIGURE 4. Worst-case MW versus L_G characteristics for FeFETs with various O-phase probabilities and grain sizes considering the impact of high-k spacers.

The improved MW for FeFETs with high-k spacers results from the fringing field through high-k spacers, which increases the electric field and voltage drop across the ferroelectric [10], [14], [15], leading to larger difference in polarization between the positive and negative writing pulses. More importantly, as shown in Fig. 3, the improvement increases with decreasing gate length (L_G). As L_G is downscaled from 24 to 18 and 12 nm, it can be seen from Fig. 3 that the improvement in mean value of MW (i.e., μMW) from high-k spacers increases from 9% to 20% and 36%, respectively. It can also be seen that, without spacers, the worst-case MW reduces with L_G (from 0.72 to 0.68 and 0.6 V as L_G is downscaled from 24 to 18 and 12 nm, respectively) because it is easier to form the DE path as L_G decreases. With high-k spacers, nevertheless, the worst-case MW stays nearly a constant (around 0.8 V) as L_G decreases due to the larger improvement from high-k spacers for FeFETs with shorter L_G.

Fig. 4 further shows the worst-case MW versus L_G characteristics for FeFETs with various O-phase probabilities (60% and 80%) and grain sizes (6 and 3 nm). It can be seen that raising the O-phase probability and reducing the grain size are two keys to sustaining the MW, while using high-k spacers can serve as another way to enhance the scalability of FeFETs. For example, under the case of 80% O-phase and 6 nm grain size (green triangle), using high-k spacers can provide a boost (orange triangle) in the worst-case MW close to that of reducing the grain size to 3 nm (blue diamond). It can also be seen that, under the case of 80% O-phase and 3 nm grain size, using high-k spacers may even result in a reverse trend in the MW versus L_G characteristic (purple diamond), i.e., the worst-case MW increases with decreasing L_G.

The remarkably increased MW for scaled FeFETs (e.g., L_G = 12 nm) with high-k spacers may also be utilized to

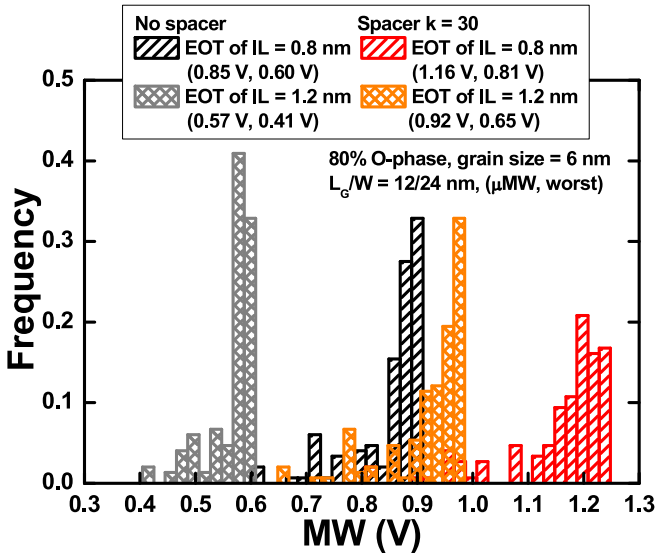

FIGURE 5. Impact of high-k spacers on the MW distributions considering the FE-DE phase variation for scaled FeFETs (L_G = 12 nm) with various EOT of IL. The impact of high-k spacers increases with increasing EOT of IL.

ease the FeFET device design. For example, Fig. 5 compares the impact of high-k spacers on the MW distributions for scaled FeFETs (L_G = 12 nm) with the EOT of IL = 0.8 and 1.2 nm. It can be seen that the high-k spacers induced MW improvement is larger for the FeFET with larger EOT of IL (The improvements in μMW and the worst-case MW are 0.35 V and 0.24 V, respectively, for EOT of IL = 1.2 nm, while the improvements in μMW and the worst-case MW are 0.31 V and 0.21 V, respectively, for EOT of IL = 0.8 nm). It can also be seen that, with the aid of high-k spacers, the FeFET with EOT of IL = 1.2 nm can possess a superior MW distribution (orange bar) than the FeFET with EOT of IL = 0.8 nm without high-k spacers (black dashed bar). In other words, for a given MW, the FeFET with high-k spacers can adopt a thicker IL design for better reliability.

IV. IMPACT OF HIGH-K SPACERS ON ELECTRIC FIELD ACROSS INTERFACIAL LAYER

The reliability challenge of FeFETs stems mainly from the high electric field across the interfacial layer, E_{IL}, during write operation [10], [11]. It is crucial to find a device design that can lower the E_{IL} without the cost of MW. In this section, we investigate the impact of high-k spacers on the E_{IL} for FeFET NVMs.

Figs. 6(a) and 6(b) show the electric field contours for ideal FeFETs (100% O-phase) designed with 0.8 nm EOT of IL without spacers and with high-k spacers, respectively, during write operation (V_W = −4 V). The high electric field across the IL and the fringing field through high-k spacers near the source/drain (S/D) edge can be clearly seen. Figs. 6(c) and 6(d) show the E_{IL} at mid channel and near the S/D edge, respectively, for FeFETs with various gate lengths during write operation (V_W = −4 and 4 V). For FeFETs without spacers, it can be seen by comparing

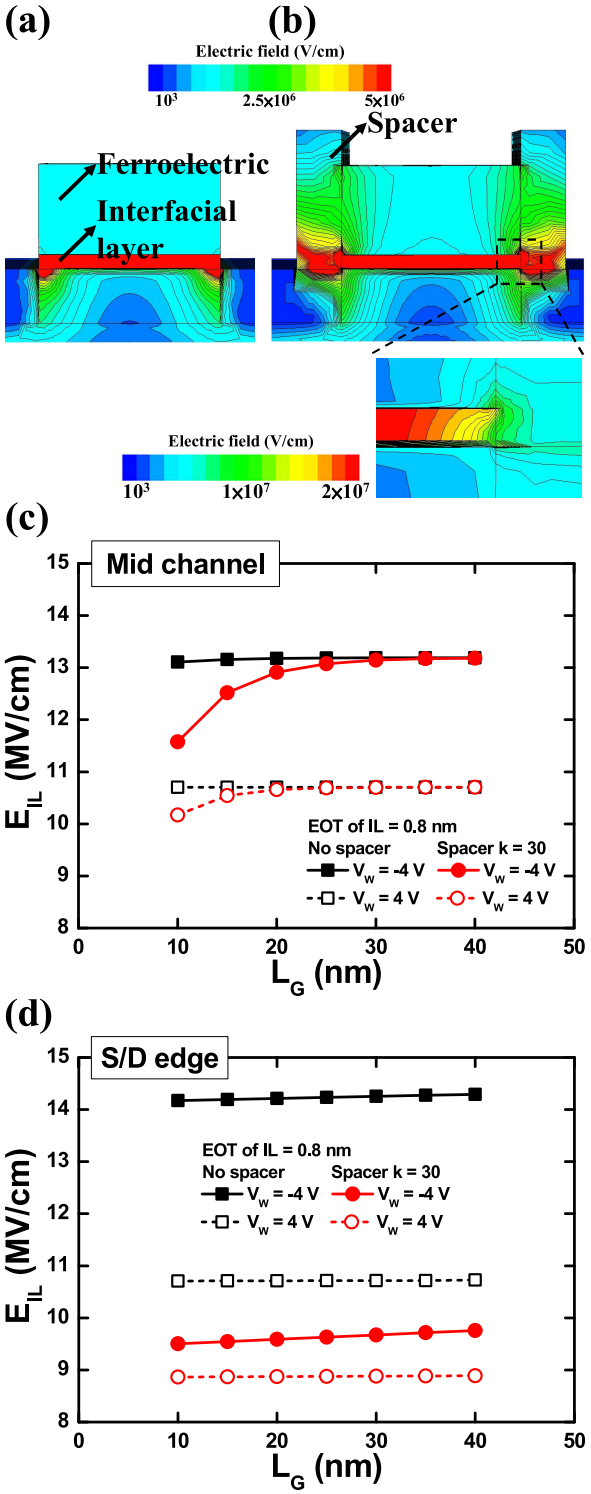

FIGURE 6. Electric field contours during write operation (V_W = −4 V) for FeFETs (L_G = 20 nm) under the design (a) without spacers and (b) with high-k spacers (including the zoom-in region and its contour range). The IL is assumed to be Si_3N_4 with k = 7.8 [16]. Also shown are impacts of high-k spacers on the E_{IL} at (c) mid channel and (d) source/drain edge during write operation (V_W = −4 and 4 V) for FeFETs with various L_G.

Figs. 6(c) and 6(d) that the highest E_{IL} occurs near the S/D edge (~14 MV/cm as shown in Fig. 6(d)), which is under the negative gate pulse (i.e., V_W = −4 V) [10], [17]

and is independent of L_G. For FeFETs with high-k spacers, however, the E_{IL} near the S/D edge substantially reduces ($\sim$9.5 MV/cm for $V_W = -4$ V as shown in Fig. 6(d)), and the highest E_{IL} is now located at the mid channel (red solid line in Fig. 6(c)). Moreover, as can be seen in Fig. 6(c), this highest E_{IL} starts to decrease when L_G is down-scaled (below $L_G \sim 30$ nm), and the reduction in mid-channel E_{IL} significantly increases with decreasing L_G due to the increasing impact of the S/D edges to the whole channel. In other words, for scaled FeFETs with high-k spacers, the ferroelectric field is increased and the voltage drop across the IL is decreased, resulting in reduced critical E_{IL} for reliability.

V. CONCLUSION

We have investigated scaled FeFET NVMs with the high-k spacer device design considering FE-DE random phase variations. Our study indicates that, the formation of DE leakage path is mainly determined by the grain size and O-phase probability of the ferroelectric for a given device size. However, using high-k spacers can significantly improve the MW of the worst device instance with the DE leakage path. More importantly, these MW improvements increase with the down-scaling of L_G. In other words, the scalability of FeFETs can be enhanced by using high-k spacers. In addition, we have investigated the impact of high-k spacers on the E_{IL} for FeFET NVMs. For FeFETs with high-k spacers, the E_{IL} near the S/D edge can be substantially reduced, and the highest E_{IL} is no longer located near the S/D edge but at the mid channel. Using high-k spacers can also reduce the mid-channel E_{IL}, and the reduction increases with decreasing L_G due to the increasing impact of high-k spacers.

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