Received 30 March 2022; revised 18 April 2022; accepted 20 April 2022. Date of publication 25 April 2022; date of current version 2 May 2022.
The review of this article was arranged by Editor G. I. Ng.

Digital Object Identifier 10.1109/JEDS.2022.3169811

Effective Suppression of Current Collapse in AlGaN/GaN HEMT With N_2O Plasma Treatment Followed by High Temperature Annealing in N_2 Ambience

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This work was supported in part by the Science and Technology Plan Projects of Guangdong Province under Grant 2020B010171001; in part by the Guangdong Basic and Applied Basic Research Foundation under Grant 2021A1515012566; in part by the Science and Technologies Plan Projects of Guangzhou City under Grant 201905010001 and Grant 202002030407; and in part by the Science and Technology Development Special Fund Projects of Zhongshan City under Grant 2019AG014, Grant 2019AG042, and Grant 2020AG023.

ABSTRACT We propose a high temperature annealing process in N_2 ambience after N_2O plasma treatment for AlGaN/GaN HEMT. The annealing process effectively improves the plasma treated surface condition and decreases the current collapse from 41.7% to 10.6%. The N_2O plasma treatment is performed in a PECVD chamber and the followed high temperature annealing process is carried out at 800°C for 20min in rapid temperature annealing (RTA) system. Compared to the devices with only N_2O plasma treatment, the devices with an extra high temperature annealing process perform lower surface state density (2.51E+12 $cm^{-2}eV^{-1}$, ΔE from 0.353 eV to 0.413 eV; 5.38E+11 cm^{-2}, $\Delta E > 0.519$ eV) and better dynamic characteristics.

INDEX TERMS AlGaN/GaN HEMT, N_2O plasma treatment, current collapse, high temperature annealing.

I. INTRODUCTION

In the past decades, the wide bandgap semiconductor material, gallium nitride (GaN), attracted great attention for the excellent potential application in high-power and high-voltage operations at high frequency band due to its wide bandgap, high breakdown electric field, and excellent thermal properties [1]. The main issues hindering dynamic and power performance, as well as the electrical reliability of AlGaN/GaN high -electron -mobility transistors (HEMTs), are gate leakage current and current collapse. To overcome these problems, different dielectric materials such as SiO_2 [2], [3], SiN_x [4], and Al_2O_3 [5] have been proposed for the fabrication of metal-insulator-semiconductor (MIS) HEMTs. However, to effectively suppress dispersion, the passivation layer like SiN or SiO_2 needs to exceed 50nm [6]. The relative thick passivation layer inevitably introduces extra parasitic capacitance which could degrade the RF performance [7].

In recent years, some researchers reported a dielectric-free passivation process on device access region with O_2 or N_2O-containing plasma treatment and obtained good device switching and a relatively high RF performance [6]–[9]. However, plasma treatment like N_2O treatment is usually performed in a PECVD chamber. Some researchers pointed out that the active plasma sources in PECVD could induce damage to the surface of (Al)GaN surface [10], [11]. The semiconductor surface damage increases the surface trap or dangling bond defects, resulting in a weak passivation protection effect and increased current collapse [12], [13]. Recently some researchers found that the long term high temperature (800 °C) annealing process in N_2 ambient help reconstruct the plasma-oxidized

GaN surface, which can result in better surface properties [14].

In this brief, we use a high temperature N_2 annealing process after N_2O plasma treatment for AlGaN/GaN HEMT to improve the plasma treated surface. The pulsed-IV result shows an obvious decrease in current collapse (from 41.7% to 10.6%) compare to the sample without the annealing process. Furthermore, the capacitance-voltage (C-V) measurement and the pulsed transfer characteristics also show a lower surface state density. Compared to N_2O plasma treated devices, the devices with an extra high temperature annealing process exhibit an improvement in surface state and a more effective suppression in current collapse.

II. MATERIAL AND METHODS

The AlGaN/GaN epilayer used in this work was grown on Si (111) substrate using metal organic chemical vapor deposition (MOCVD). The epitaxial structure consists of a 3.5 μm carbon doped GaN buffer layer, a 300 nm GaN channel layer, a 1 nm AlN interlayer, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 1 nm GaN cap layer grown by MOCVD. A 2DEG mobility of 1685 $cm^2/V \cdot s$ and a sheet carrier concentration of 1.215×10^{13} cm^{-2} are measured by Hall effect measurement.

The device fabrication of the AlGaN/GaN HEMTs started with the cleaning of the epitaxial wafer by a standard solvent. Then, devices were isolated using BCl_3 and Cl_2 etching in an Inductively Coupled Plasma (ICP) system. Prior to the deposition of ohmic metal, surface treatment was performed by immersing in BOE for 60 s. Different from samples C and D, a plasma-enhanced chemical vapor deposition (PECVD) system was used for N_2O plasma treatment before ohmic contact for samples A and B. The flow rate of N_2O was 120 sccm, the RF power was 50 W, the processing time was 20 min, and the chamber temperature was 300°C. Differing from sample A, samples B and D were immediately annealed at 800°C for 20 min in N_2 ambience by Rapid Temperature Annealing (RTA).

The 800°C long term annealing process was done before forming ohmic contact to avoid possible ohmic contact degradation during the high temperature annealing process. The S/D window was opened by Cl_2 etching in the ICP system. The Ti/Al/Ni/Au metal stack was then deposited by E-beam evaporation. RTA at 830 °C for 30 seconds in an N_2 ambient was then performed to form ohmic contact. The contact resistance calculated by transfer length method (TLM) measurement is 0.90 Ω.mm, 0.85 Ω.mm, 0.87 Ω.mm, 1.91 Ω.mm for samples A, B, C and D, respectively. Finally, an Ni/Au (50nm/250nm) gate electrode was deposited by electron beam evaporation for all samples without oxide stripping process before the gate metal deposition. The space of gate-to-source and gate-to-drain are 10 μm and 30μm, respectively. Meanwhile, the gate width and length are 100 μm and 3 μm respectively. Fig. 1 shows the cross-sectional view and optical microscope image of the device. Fig. 4 shows the process split of all samples.

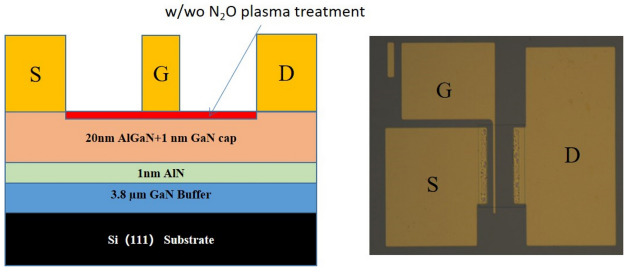

FIGURE 1. (a) Cross-sectional view. (b) Optical microscope image of the device.

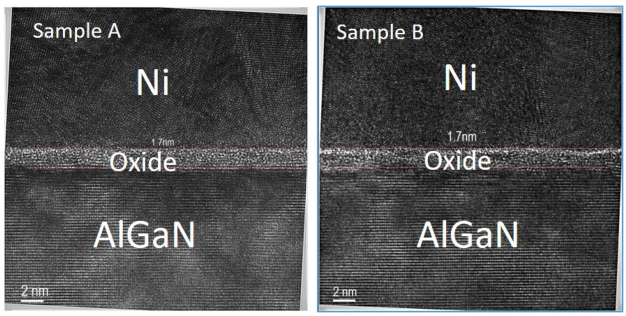

FIGURE 2. HRTEM image of N_2O plasma treatment formed oxide between the gate metal and AlGaN barrier layer for samples A and B.

Hall measurement was applied for all samples. The sheet carrier density of samples A, B, C and D are 1.130×10^{13} cm^{-2}, 1.137×10^{13} cm^{-2} and 1.215×10^{13} cm^{-2},1.020×10^{13} cm^{-2}. The 2DEG mobility of samples A, B and C are 1800 $cm^2/V \cdot s$, 1838 $cm^2/V \cdot s$ and 1685 $cm^2/V \cdot s$, 1350 $cm^2/V \cdot s$. The decrease in electron sheet density of samples A and B after plasma treatment is due to part of the barrier layer being converted to oxide. The decrease in electron sheet density of sample D is due to the extra long term RTA process. And it has been reported that the high temperature RTA process decreases 2DEG carrier density and mobility [15], [16]. However, the same situation did not occur in sample B. It may be due to the plasma-oxide layer working as a protection layer during the RTA process. And it has been reported that depositing a protection layer like SiN before ohmic to avoid the negative influence of the high temperature RTA process [17].

The device cross-section view and High Resolution Transmission Electron Microscope (HRTEM) image is displayed in Fig. 2. The thickness of the oxide layer was measured to be around 1.7 nm for both samples A and B by using the HRTEM image. Fig. 3 shows the surface morphology of a plasma treated, a plasma-treated/high temperature annealed and an untreated GaN surface, which was characterized by an atomic force microscope (AFM). A slightly surface degradation was found after the RTA process. Such a long term 800°C high temperature may be essential to reconstructing the plasma treated GaN surface [14]. Fig. 5(a) shows X-ray photoelectron spectroscopy (XPS) spectra N1s core-level spectra of samples A and B, we found the N-O bond at around 403 eV [18] in sample A. However,

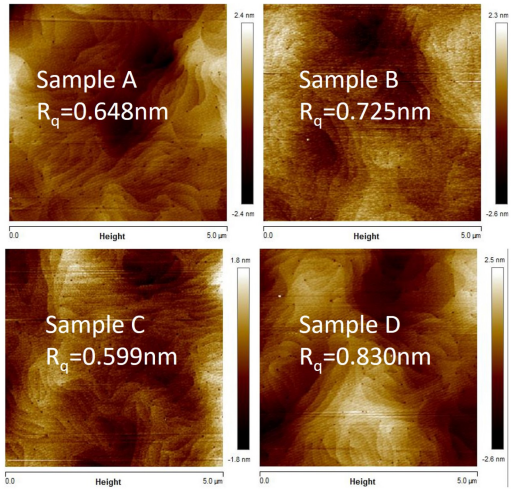

FIGURE 3. Surface roughness of samples A, B, C and D.

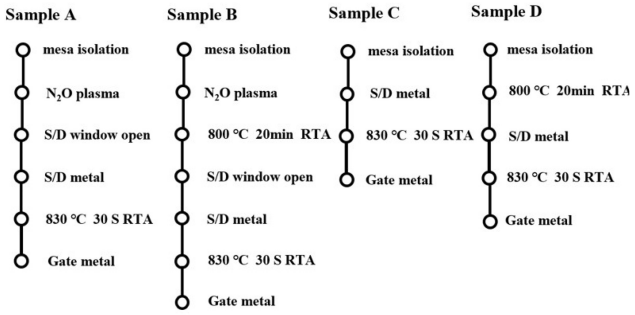

FIGURE 4. The process splits of all samples.

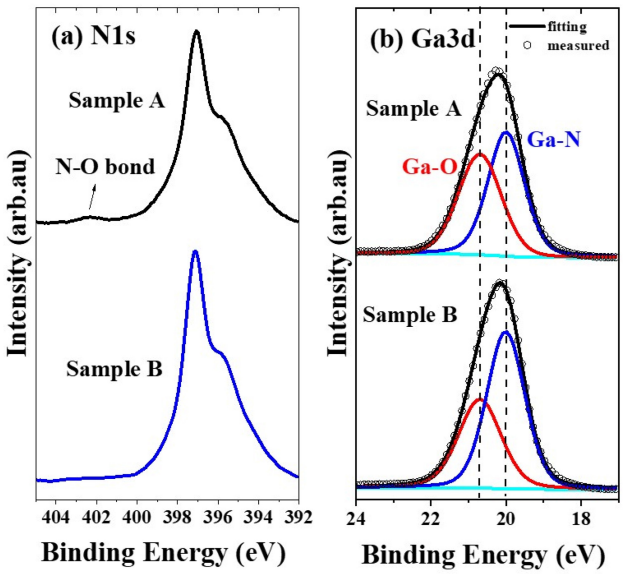

FIGURE 5. XPS spectra of N 1s and Ga 3d for samples A and B.

we did not find any N-O peaks in sample B. The N 1s result for sample B is similar to the "2 ML EC" structure which does not contain any N-O bonds [19]. This may indicate the breaking up of the N-O bond or the reconstruction of the plasma-treated surface during the high temperature annealing

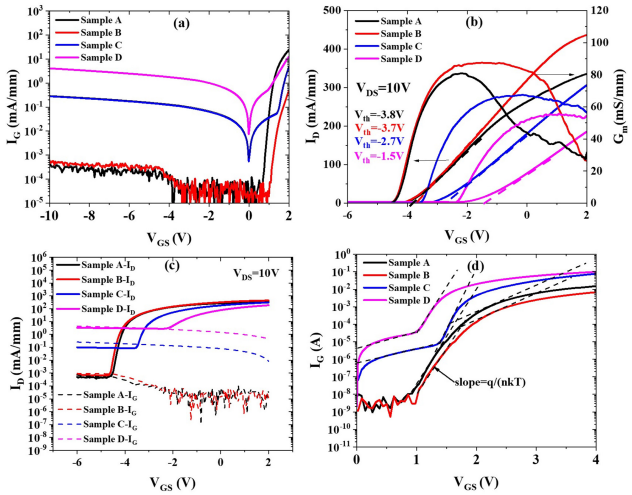

FIGURE 6. (a) Gate leakage current (b) Transfer characteristics in linear scale (c) Transfer characteristics in semi-log scale. (d) the forward I_G-V_{GS} characteristics of Ni/Au Schottky diodes.

process. As shown in Fig. 5(b), the 800°C annealing process decreases the Ga-O/Ga-N ratio from 0.92 to 0.64 compared to sample A. The Ga-O/Ga-N ratio is calculated by integration and taking appropriate values for the sensitivity factor for Ga3d spectrum.

III. RESULTS AND DISCUSSION

Fig. 6 shows the gate leakage current and transfer I_D-V_{GS} characteristics at $V_{DS} = 10$V of all samples. The reverse gate leakage current of sample B is slightly increased compared to sample A. The sample C without N_2O plasma treatment shows a much higher gate leakage current compare to samples A and B. And the ratio of on-state current and off-state current (I_{on}/I_{off}) is around 10^6, 10^6, 10^3, 10^2 for samples A, B, C and D. Different from the previous studies in which the post-gate annealing process decreased the leakage current and enhance both dc and microwave characteristics [20], the slightly increased reverse gate leakage current after high temperature annealing may due to the decreased Ga-O/Ga-N ratio of plasma treated surface in sample B (GaO has a larger bandgap than GaN, 4.8 eV compare to 3.4 eV) and the slightly surface degradation confirmed by AFM test. And for the forward gate leakage current, the long term 800° Cannealing after plasma oxidation treatment can probably reconstruct the plasma-oxidized GaN surface, which is expected to present stronger immunity to the bombardment of hot electrons generated under forward gate bias and get a lower forward gate leakage current [14]. The slightly higher off drain current of sample B is due to the slightly higher gate leakage current in the off state compared to sample A. The higher off state gate leakage current is consistent with the higher reverse gate leakage current of sample B. The increased gate leakage current of sample D may be due to the surface roughness degradation confirmed by the AFM test compared to sample C.

The threshold voltage (V_{th}) of samples A, B, C and D are −3.80 V, −3.70 V, −2.70 V and −1.5V, respectively.

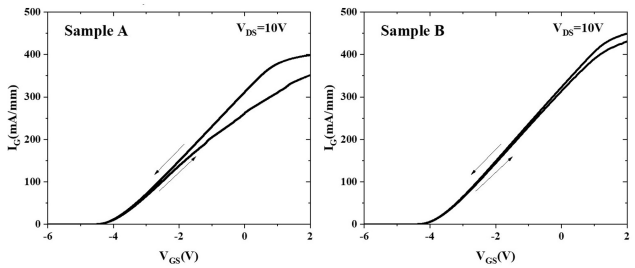

FIGURE 7. The forward and backward sweep transfer curves for samples A and B.

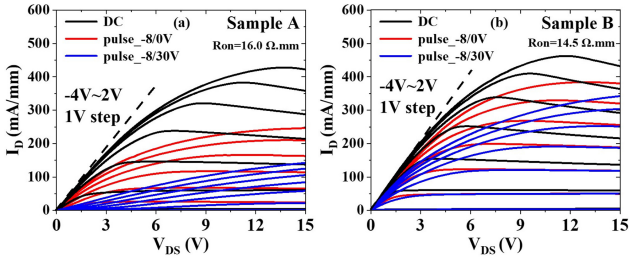

FIGURE 8. DC mode and pulse mode output characteristics of samples A and B.

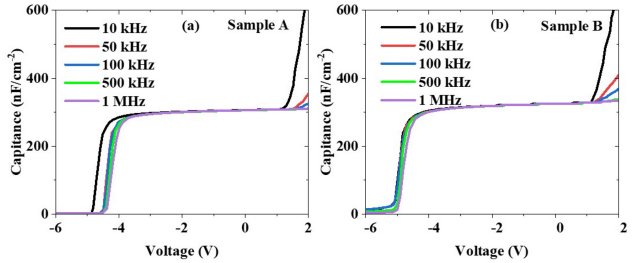

FIGURE 9. CV measurement at different frequencies of samples A and B.

Compare to sample C without N_2O plasma treatment, the threshold voltage for samples A and B shift towards the negative side. It is probably that the dielectric constant of the formed oxide layer is lower and can sustain more gate voltage than GaN cap layer. The gate voltage dropped on the AlGaN barrier layer was reduced and a larger negative gate voltage is expected to deplete the channel electrons, resulting in the negative shifted threshold voltage [21].

The I_D at higher V_g is much higher for sample B compare to sample A. The possible reason is that we measured the transfer curves from negative Vg to positive, the traps in the access region capture electrons and decrease the sheet density during the off state. Fig. 7 shows that the I_D of sample A in the forward sweep is much higher than the I_D in the backward sweep. And the hysteresis of sample B is much smaller. This probably reveals that the plasma treated GaN surface reconstructs during the long term 800°C high temperature annealing process. Sample B should have less N vacancy which may cause by the plasma treatment process or a better surface state compared to sample A.

The Schottky parameters including barrier height and ideality factor were extracted from forward I_G-V_{GS} characteristics of Ni/Au Schottky diodes in Fig. 6(d). The ideality factor n can be extracted from the slope of the first fitting line (slope = q/(nkT), q is the electron charge, k is the Boltzmann's constant, and T is the temperature), and the barrier height can be calculated with the flat-band voltage [22]. The calculated ideality factors are 2.93, 3.14, 15.8, 19.7, for samples A, B, C, and D. The calculated Schottky barrier height is 0.99eV, 0.97eV, 0.61eV and 0.53eV for samples A, B, C and D.

Fig. 8 shows the current collapse characteristics of samples A and B by pulsed-IV measurements. The width and period of the pulse are set to 100 μs and 5 ms, respectively. The biases (V_{GQ}/V_{DQ}) are set at −8/0 V and −8/30 V in the measurement. The current collapse is 41.7% and 10.6% for samples A and B at −8/0 V, respectively. And the current collapse is 66.4% and 20.8% for samples A and B at −8/30 V, respectively. The current collapse is well suppressed in sample B compared to sample A, indicating the effective passivation effect of N_2O plasma treated/high temperature annealing process. The current of sample A exhibits great collapse in pulsed-IV mode, revealing the surface traps in the gate-drain area.

The capacitance-voltage (C-V) measurement results at different frequencies of samples A and B are shown in Fig. 9. Circular-shaped capacitors with the same process as samples A and B were used for CV measurements. The diameter of the circular area is 200 μm. Samples A and B have two rising slopes when frequencies are below 100kHz. The first slope represents the complete depletion of two-dimensional electron gas (2DEG) and the second slope indicates the electron transfer from AlGaN/ GaN to dielectric/AlGaN interface [23]. At frequencies of 500kHz and 1MHz, the second slope is missing for the two samples which means that the oxide /AlGaN interface trap states do not respond at those frequencies. The interface state density (Dit) at different energy levels can be extracted from the C-V curves [24]. We used dielectric capacitance in series with the barrier capacitance model to extract the gate dielectric capacitance per unit area (C_{ox}) of samples A and B [25]. The C_{ox} is 860 and 1000 nF/cm^2 for samples A and B, respectively. The calculated energy gap between the conduction band and interface trap (ΔE) is from 0.353 eV to 0.413 eV. By comparing the test results with frequencies of 10 kHz and 100 kHz, we calculated the surface state density (Dit) values of the two samples. The Dit is 4.78E+12 and 2.51E+12 cm^{-2} eV^{-1} for samples A and B, respectively.

The pulsed transfer characteristics with various drain biases of samples A and B are measured to evaluate the trap density (Dit) in Fig. 10. The measurement contains an up sweep (V_G_Base = −6 V) and a down sweep (V_G_Base = +3 V). During each individual measurement, the drain bias remains stable. The width and period of the pulse are set to 1 ms and 10 ms, respectively. The short pulse width (1 ms) is set to retain all electrons whose emission time constant is larger than 1 ms or ΔE >0.519 eV trapped in trap states [26]. These trap states consist of the oxide/AlGaN

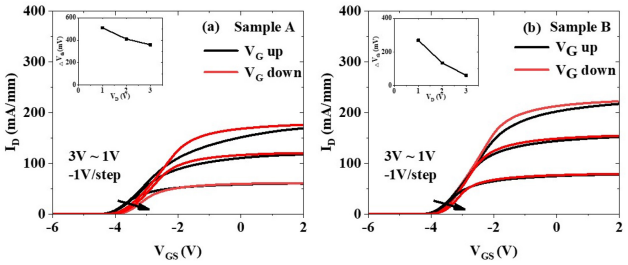

FIGURE 10. Pulse mode transfer characteristics of samples A and B from 3 to 1 V. Insets: Vth hysteresis varied with different applied V_D.

interface states and the trapped charges in the AlGaN barrier and the oxide layer. The interface state charge (Qit) could be calculated by the equation $Qit = C_{ox} \times \Delta V_{th}/q$, where ΔV_{th} is the threshold hysteresis extracted from the pulsed mode transfer curves. We use ΔV_{th} at $V_D = 1V$ to reduce drain-to-gate field-assisted detrapping. The Qit values are 9.67E+11 cm^{-2} and 5.38E+11 cm^{-2} for samples A and B, respectively. The C-V and pulsed transfer characteristics results show a lower trap density of sample B than sample A.

IV. CONCLUSION

We propose a high temperature annealing process in N_2 ambience after N_2O plasma treatment for AlGaN/GaN HEMT. The oxide layer work as gate dielectric layer and passivation layer. Compared to the devices with only N_2O plasma treatment, the devices with an extra high temperature annealing process perform lower surface state density and better dynamic characteristics. It is probably that the long term high temperature annealing process reconstructs the plasma treated GaN surface, resulting in better current collapse performance and lower Dit. In general, a long term 800°C high temperature annealing process after N_2O plasma treatment improves the surface state, receiving better current collapse performance for AlGaN/GaN HEMT.

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