Received 24 February 2022; revised 17 April 2022; accepted 20 April 2022. Date of publication 22 April 2022; date of current version 2 May 2022.
The review of this article was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2022.3169702

LDMOS Drift Region With Field Oxides: Figure-of-Merit Derivation and Verification

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ABSTRACT We analytically and numerically investigate the performance of Laterally-Diffused Metal-Oxide-Semiconductor (LDMOS) transistors with Semi-circular Field OXide (S-FOX) focusing on mid-voltage (30 V – 100 V) power applications. We derive an analytical relation between breakdown voltage and on-resistance to realize the ideal behavior of the drift region for an LDMOS with S-FOX. Then, we find the optimized drift doping concentration minimizing the on-resistance at a given breakdown voltage. We introduce a new figure-of-merit for the drift region of a lateral device with S-FOX. We finally verify our ideal analytical findings with numerical results modeled and simulated in a commercial Technology Computer-Aided Design (TCAD).

INDEX TERMS Analytical study, breakdown voltage, drift region, figure-of-merit, LDMOS, on-resistance, TCAD.

I. INTRODUCTION

Laterally-Diffused Metal-Oxide-Semiconductor (LDMOS) field-effect transistors are commonly used in low-voltage [1], [2], mid-voltage [3], [4], and high-voltage [5]–[8] applications because of their promising performance and their use of silicon technology. Ever growing commercial applications of LDMOS transistors has attracted much attention in the research community [9]–[11]. Recently, many studies have been experimentally [12]–[14] and numerically [15]–[18] performed on the improvement of LDMOS design and optimization.

One essential component of device improvement is the understanding of fundamental performance limits, which can be derived using analytical investigations. For example, Baliga introduced a very practical and well-known figure-of-merit (*FOM*) relating the breakdown voltage (*BV*) and specific on-resistance ($R_{SP} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^{s3}}$) on a one-dimensional (1-D) ideal drift region in 1989 [19]. Later on, several other analytical studies have been performed on super-junction vertical power devices [20]–[22], lateral power devices with homogenization field [23], and double gate MOSFETs [24], [25]. However, an analytical study providing a fundamental understanding on LDMOS devices with a specific shape of field oxide is surprisingly missing.

A Field Oxide (FOX) is commonly used in different kinds of transistors by encroaching an oxide into the semiconductor at the drain side for mid-voltage and high-voltage applications. The FOX improves the breakdown voltage, by distributing more potential drop and reducing the electric field crowding underneath the gate edge at the drain side. Several recent experimental studies have been done on LDMOS devices with different shapes of FOX, improving the LDMOS performance using a FOX [26]–[30].

Recently, we reported the importance of the *FOM* for LDMOS drift regions in [31] and found relations between device characteristics with different shape of field oxides. However, more details regarding the *FOM* derivation procedure are needed to fully clarify our analytical approach for readers. Moreover, a comprehensive and promising comparison of the *FOM* equation with simulation results is needed to confirm the accuracy of our results and further enhance the validity of our findings.

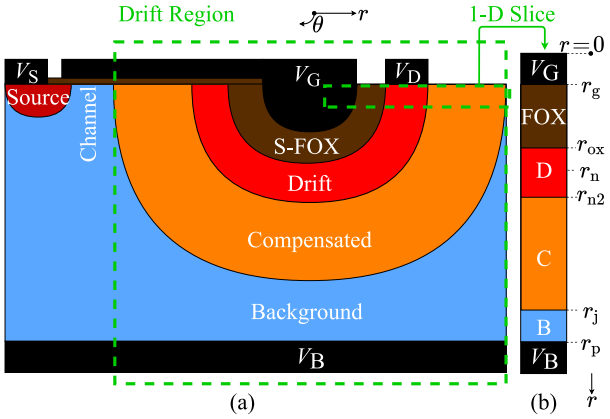

FIGURE 1. (a) Schematic configuration of an *n*-channel LDMOS transistor with S-FOX. (b) 1-D slice of the drift region. We consider uniform doping profiles for all regions except for the C-region. A doping profile of $\varrho \propto \frac{1}{r}$ is used in the C-region.

In this paper, we perform an analytical study on LDMOS transistors with semi-circular FOX (S-FOX) suitable for mid-voltage power applications targeting 30 V – 100 V. The structure of the S-FOX represents an ideal FOX in a drift region of lateral devices and we compare our results with Baliga's ideal drift region. The reason we choose a S-FOX structure is that we can solve our analytical equations in polar coordinates to provide a simple and applicable figure-of-merit. Instead of the conventional FOXs such as local oxidation of silicon (LOCOS), shallow trench isolation (STI), and stepped gate oxide, we use an ideal FOX to perform a fundamental study and find a theoretical limit for the ideal drift region of LDMOS transistors. Moreover, we verify our analytical findings by carrying out a numerical study, modeling and simulating an extensive number of LDMOS devices (more than 2,000) using a commercial technology computer-aided design (TCAD) simulation package [32]. Our key result is a modified LDMOS *FOM* which can be used as a target during practical LDMOS design.

II. DEVICE STRUCTURES AND ANALYTICAL DERIVATION

Fig. 1(a) shows the schematic configuration of an *n*-channel LDMOS with S-FOX. We consider uniform doping profiles for all regions except for the compensated region (C-region). A doping profile of $\varrho \propto \frac{1}{r}$ is used in the C-region. We assume the drift region resistance dominates over the contact and channel resistances. Fig. 1(b) shows a 1-D slice of the drift region over which we solve the Poisson equation in polar coordinates. As indicated in Fig. 1(b), r_g is the radius of the gate electrode, r_{ox}, r_{n2}, r_j, r_p are respectively the coordinates of the FOX, drift region, *p*-*n* junction, background, and r_n is the coordinate in the drift region where the depletion region originating in the oxide region and the depletion originating in the background meet.

Gauss's Law ($\frac{1}{r}\frac{d}{dr}(rE(r)) = \frac{\varrho(r)}{\varepsilon(r)}$) and the potential equation ($\frac{d}{dr}V(r) = -E(r)$) are solved in 1-D polar coordinates over each region to derive the electric field and potential profile. Considering an ideal situation, we assume the electric field all over the C-region equals the critical electric field of silicon (E_c^s) at breakdown; we realize this by taking $\varrho \propto \frac{1}{r}$.

To find the *FOM* for the LDMOS with S-FOX, we combine the breakdown voltage equation, calculated from the Poisson equation, and the specific on-resistance. The R_{SP} is calculated by determining the drain-to-source on-resistance (R_{DS}) and multiplying by the half-pitch (*HP*). We model the drift region as infinitesimal semi-circular resistors with radius ranging from r_{ox} to r_{n2} conducting current in parallel. Each of these semi-circular resistors has length πr and thickness dr. The total drift region resistance is then

$$\frac{1}{R_{DS}} = \frac{1}{\rho}\int_{r_{ox}}^{r_{n2}} \frac{1}{\pi r} dr,$$

where ρ is the resistivity. Now assuming a minimum *HP* equaling $2r_{n2}$, the specific on-resistance is

$$R_{SP} = R_{DS} \times HP = \frac{1}{q\mu_n N_D} \frac{\pi}{\ln\left(\frac{r_{n2}}{r_{ox}}\right)} \times 2r_{n2}, \tag{1}$$

where q, μ_n, and N_D are respectively elementary charge, electron mobility, and drift doping concentration.

To simplify Eq. (1) and deduce a more applicable equation, we use the following logarithm expansion approximation from [33].

$$\ln z \approx \left(\frac{z-1}{z}\right) + \frac{1}{2}\left(\frac{z-1}{z}\right)^2, \tag{2}$$

which is valid for $z \geq \frac{1}{2}$. In our equation since r_{n2} is always greater than or equal to r_{ox}, $z = \frac{r_{n2}}{r_{ox}} \geq 1$ and we can use the expansion approximation. We also assume that the breakdown voltage is determined by the oxide radius and the drift length. That is,

$$BV = \pi E_c^s r_{ox} + E_c^s (r_{n2} - r_{ox}) \tag{3}$$

where the first part ($\pi E_c^s r_{ox}$) is the voltage drop around the FOX and the second part ($E_c^s(r_{n2} - r_{ox})$) is the voltage drop in the drift region between the FOX and the channel. Considering an ideal case, we assume the electric field reaches the breakdown field of silicon over the drift region at breakdown voltage. This is realized when the thickness of the drift region is

$$r_{n2} - r_{ox} = 2\frac{\varepsilon_s E_c^s}{q N_D}. \tag{4}$$

Combining Eq. (1), Eq. (2), Eq. (3), and Eq. (4) simplifies Eq. (1) to

$$R_{SP} = \frac{BV^2}{\pi \varepsilon_s \mu_n E_c^{s3}} + \frac{(3\pi - 4)BV}{\pi q \mu_n N_D E_c^s} \tag{5}$$

where the first term of Eq. (5), which we call the 1st order approximation, can be used in high N_D and/or high *BV* conditions. The 1st order approximation predicts that the S-FOX outperforms Baliga's ideal drift region by a factor $\frac{1}{4\pi}$. However, for low N_D and/or low *BV,* both terms

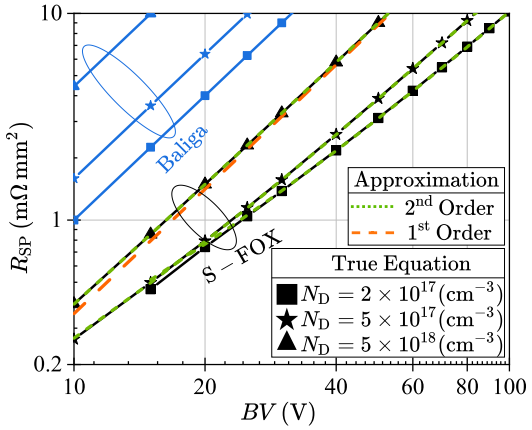

FIGURE 2. R_{SP} versus BV for LDMOS with S-FOX and Baliga's ideal drift region at different N_D values. The dashed lines show the approximated relations. The 1st order approximation is used for high N_D whereas the 2nd order approximation is used for $N_D < 5 \times 10^{18}$ cm^{-3}.

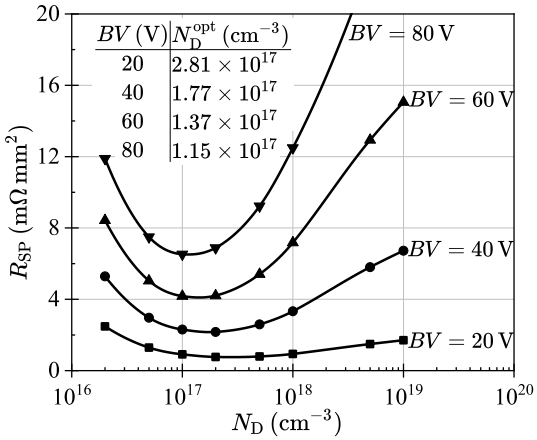

FIGURE 3. R_{SP} versus N_D at different BV values. There is an optimum N_D (N_D^{opt}) which minimizes the R_{SP} at a given BV. $1.15 \times 10^{17} \leq N_D^{opt} \leq 2.81 \times 10^{17}$ is the optimum range for devices with 20 V $\leq BV \leq$ 80 V. The values of N_D^{opt} for different BVs are shown in the inset.

are required which we call the 2nd order approximation. To check the logarithm expansion approximation and validate our approximated equation (Eq. (5)), we numerically solve the Eq. (1), referred as "true relation", and compare it with results taken from Eq. (5).

III. ANALYTICAL RESULTS AND DISCUSSION

Fig. 2 shows the R_{SP} versus BV for LDMOS transistors with S-FOX for three different N_D values. The black solid lines show the true relations (Eq. (1)) whereas the dashed lines present the approximated relations (Eq. (5)). The long orange dashed line shows the 1st order approximation, suitable for $N_D = 5 \times 10^{18}$ cm^{-3} and higher, whereas the short green dashed lines represent the 2nd order approximation, suitable for lower N_D values. We also added Baliga's curves with three N_D values for the purpose of comparison. To consider the mobility degradation due to the ion scattering in high drift doping concentration, we assume a doping-dependent electron mobility. We use the well-known Baliga's mobility equation for silicon [19] as follows

$$\mu_n = \frac{5.1 \times 10^{18} + 92 \times {N_D}^{0.91}}{3.75 \times 10^{15} + {N_D}^{0.91}} \left(\frac{\text{cm}^2}{\text{Vs}}\right).$$

According to Fig. 2, the S-FOX devices outperform Baliga's FOM, at a given N_D, for three reasons: (*i*) Double reduced surface field (RESURF): forming two depletion regions in the drift region, as a result of the *p*-*n* junction and the *n*-FOX junction, improving device performance [34]. (*ii*) Current direction: lateral direction for current pass, compared to the vertical direction in Baliga's original device, enhances the performance. (*iii*) Geometry: the semi-circular structure reduces the *HP* for a given drift length by a factor $\frac{2}{\pi}$. Hence, Baliga's *FOM* cannot be fully applicable for LDMOS transistors. However, we put Baliga's *FOM* in our study for the purpose of comparison as Baliga's *FOM* is universally viewed as a fundamental materials power electronics performance limit.

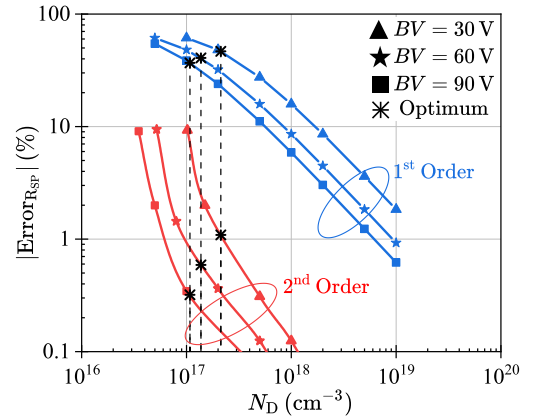

FIGURE 4. Error in R_{SP} between true relation (Eq. (1)) and the 1st and 2nd order approximations (Eq. (5)), at different BV. The Error$_{R_{SP}}$ < 1.1% for the optimum conditions of the 2nd order approximation confirms the accuracy of Eq. (5).

Fig. 3 shows the R_{SP} versus N_D at four different BV values. There is an optimum value for N_D (N_D^{opt}) minimizing R_{SP} at a given BV. The exact values of N_D^{opt} can be found in the inset of Fig. 3. Lower drift doping is required for an optimized LDMOS with higher BV. However, 10^{17} cm^{-3} < N_D < 3×10^{17} cm^{-3} is a reasonable doping range for mid-voltage power applications. Moreover, a sharper minimum in higher breakdown voltage of LDMOS devices shows the importance of drift optimization to achieve the RESURF condition in higher voltage transistors.

Fig. 4 shows the error of R_{SP} between the true relation (Eq. (1)) and the approximated equation (Eq. (5)) at different BV values. The dashed lines show the error at N_D^{opt}. The 1st order approximation fails to predict the R_{SP} for the optimum conditions with Error$_{R_{SP}} \geq 35\%$. However, the 2nd order approximation predicts the R_{SP} for the optimum conditions with Error$_{R_{SP}} < 1.1\%$, confirming the accuracy of the R_{SP} determined in Eq. (5).

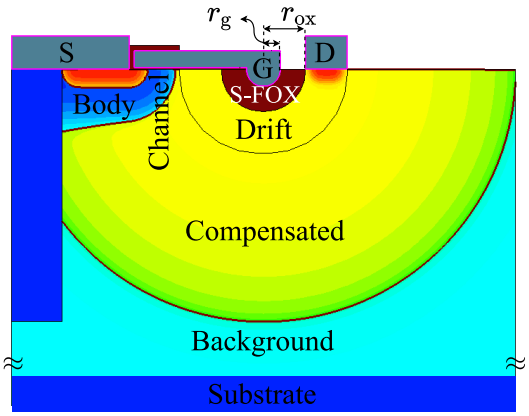

FIGURE 5. Schematic demonstration of an *n*-channel LDMOS transistor simulated in TCAD [32]. A Gaussian distribution is used for the C-region and body region. Background and drift region are uniformly doped. The r_g and r_{ox} are the radius of gate electrode and the radius of S-FOX respectively.

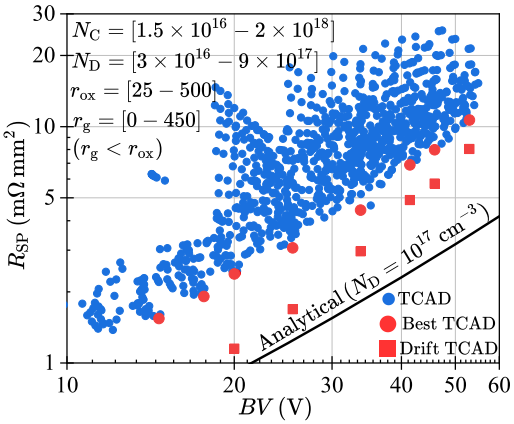

FIGURE 6. R_{SP} comparison between numerical methods (the TCAD devices, the best TCAD devices, and the drift resistance of the best TCAD devices) and analytical derivations. The R_{SP} of analytical study is always smaller than the best TCAD drift results.

To have a better understanding of our device performance we formulate our analytical equation (Eq. (5)) such that the *FOM* determined in this work for LDMOS transistors ($FOM_{\rm LDMOS}$) incorporates Baliga's FOM for an ideal drift region ($FOM_{\rm Bal}$). That is,

$$FOM_{\rm LDMOS} = \frac{BV^2}{R_{SP}} = \frac{4\pi}{(1 + V_{\rm FOX}/BV)} FOM_{\rm Bal} \qquad (6)$$

where $FOM_{\rm Bal} = \frac{\varepsilon_s \mu_n E_c^{s3}}{4}$ and $V_{FOX} = (3\pi - 4)\frac{\varepsilon_s E_c^{s2}}{qN_D}$. Assuming $E_c^s = 4 \times 10^5$ V/cm and $N_D = 10^{17}$ cm^{-3} results in $V_{FOX} = 56.1$ V. Eq. (6) reveals that the 2$^{\rm nd}$ order approximation yields a $FOM_{\rm LDMOS}$ that is up to 4π better than Baliga's *FOM*.

IV. NUMERICAL VERIFICATION

Fig. 5 shows a schematic configuration of an *n*-channel LDMOS transistor with S-FOX, simulated in TCAD. To have a fair comparison between our analytical findings (Section III) and numerical results (Section IV), we model our TCAD device similar to Fig. 1. That is, we consider an ideal S-FOX in the drift region to analyze the fundamental behavior of the device and find the theoretical limit of the drift region. However, a Gaussian distribution doping profile is used for the C-region in the TCAD LDMOS instead of a $\frac{1}{r}$ distribution. Similar to the analytical approach, we utilize a doping-dependent electron mobility in our simulations to consider the electron mobility degradation. We use the inversion and accumulation layer mobility model (IALMob) which includes doping and transverse-field dependencies based of the field perpendicular to the semiconductor–insulator interface [35]. Furthermore, we account for the effects of impact ionization using the van Overstraeten avalanche model [36].

We model and simulate more than 2,000 LDMOS devices in TCAD by changing four impactful parameters: gate radius (r_g), FOX radius (r_{ox}), N_D, and C-region doping (N_C), as shown in Fig. 6. The N_C is the peak of the Gaussian doping profile which we place at the surface of the device. Each small blue dot shows one LDMOS device simulated in TCAD, and the best devices, with the smallest on-resistance, are shown in large red dots. All the best devices have $N_D = 10^{17}$ cm^{-3} except the red dot at $BV = 53$ V which has $N_D = 9 \times 10^{16}$ cm^{-3} showing that the $N_D^{\rm opt}$ are around 10^{17} cm^{-3} and slightly decrease for higher voltages confirming our analytical results shown in Fig. 3.

We separate the specific channel on-resistance ($R_{SP}^{\rm ch}$) and drift on-resistance ($R_{SP}^{\rm drift} = R_{SP} - R_{SP}^{\rm ch}$) [37] to compare the analytical results with $R_{SP}^{\rm drift}$. The $R_{SP}^{\rm drift}$ values for the best TCAD results are calculated and plotted in red square dots in Fig. 6. For the purpose of comparison, we also plot the analytical result for $N_D = 10^{17}$ cm^{-3}. The reason for choosing 10^{17} cm^{-3} is that, according to Fig. 3, there is a minimal R_{SP} change for 8×10^{16} cm^{-3} $< N_D <$ 3×10^{17} cm^{-3} which lies in the analytical optimum range, 1.15×10^{17} cm^{-3} $\le N_D^{\rm opt} \le 2.81 \times 10^{17}$ cm^{-3}, for 20 V $\le BV \le$ 80 V. There is a good agreement between the numerical and analytical results. However, the analytical results show better performance because we assume ideal conditions in our analytical derivations. For example, the constant E_c^s over the C-region is considered for the analytical relations at breakdown whereas forming a perfect constant electric field is not possible in TCAD due to the Gaussian doping distribution.

Fig. 7 compares the *FOM* determined in this work for LDMOS transistors with Baliga's *FOM* for an ideal drift region, our TCAD results, and recent lateral transistors with new technologies and designs [38]–[44]. The solid black line shows our proposed *FOM* derived from Eq. (5) which outperforms the optimized TCAD LDMOS devices shown in Fig. 6 and all proposed devices from other studies. In addition, the solid black line outperformes Baliga's ideal drift region more in higher breakdown voltage devices, up to 4π times, which is shown in Eq. (6). Note that the solid black line is the drift resistance only whereas optimized TCAD results and other lateral transistors resistance include the channel resistance

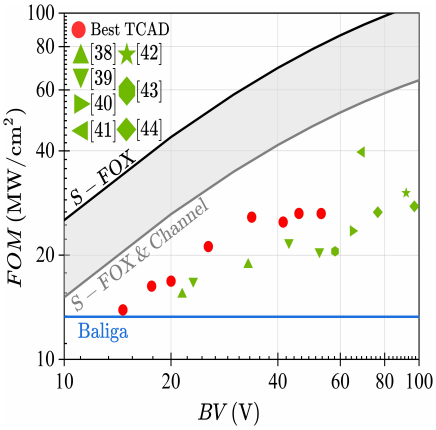

FIGURE 7. Comparison of $FOM = BV^2/R_{SP}$ calculated analytically and numerically in this work with Baliga's ideal drift region [19] and other recent studies on LDMOS devices [38]–[44]. Shaded area shows the added channel resistance to S-FOX resistance.

in addition to the drift resistance. For example, in LDMOS devices simulated in TCAD, channel resistances comprise 25% - 67% of the total resistance with lower BV devices containing a higher percentage of channel resistance showing the importance of channel optimization in low-voltage applications [16]. To include the channel resistance to the analytically derived drift resistance and set up a total resistance, in Fig. 7, we indicate added channel resistance to our S-FOX results by shading a region. Hence, in an ideal case of $R_{SP}^{ch} = 0$, we have $R_{SP} = R_{SP}^{drift}$ (solid black line) and in the case that channel resistance has a contribution of 67%, according to our TCAD results, we have $R_{SP} = 1.67R_{SP}^{drift}$ (solid gray line).

In our analytical study, considering fully depleted drift and compensated regions as well as reaching the critical electric field of a semiconductor at breakdown provide a perfect RESURF condition. In our numerical study, fully depleted drift and compensated regions are achieved by identifying the optimized LDMOS transistor as the result of our comprehensive and systematic simulation study. However, a perfectly uniformed critical electric field at breakdown is not achieved in our simulations due to using a Gaussian distribution profile in the compensated region, rather than the $\varrho \propto \frac{1}{r}$ profile of our analytical devices.

Although the proposed semi-circular FOX in this study outperforms many novel LDMOS transistors which are recently published, as shown in Fig. 7, a semi-circular FOX is not necessarily the best configuration of FOX. We have derived an analytical relationship between the breakdown voltage and the on-state resistance but determining the optimal FOX shape remains an open research question.

We focus on mid-voltage applications of LDMOS transistors with $BV < 100$ V in this paper. For applications with $BV > 100$ V, industry relies on more elaborate structures such as IGBT or superjunctions, or compound semiconductors such as GaN or SiC which have higher field strength due to their wider bandgap.

In terms of fabrication challenges, building a perfect semi-circular configuration is impossible with current oxidation processes. However, designing and building a FOX that somewhat resembles a semi-circle is experimentally feasible and can take advantages of the figure-of-merit derived in our study. For example, a semi-circular FOX can be a promising representative of a LOCOS configuration with flatter angle of tapers avoiding sharp corners. Moreover, another semi-circular-like FOX is realized when using a STI-based LDMOS when the length of the STI is comparable to or larger than the depth of the STI.

V. CONCLUSION

We performed a fundamental study to find the theoretical limit of LDMOS drift regions with field oxides. We derived an analytical relation between R_{SP} and BV for LDMOS devices with S-FOX by solving Gauss's Law and the potential equation in polar coordinates and determined approximating equations (1st order and 2nd order). We found optimum drift doping concentrations, 1.15×10^{17} cm$^{-3} \leq N_D^{opt} \leq 2.81 \times 10^{17}$ cm^{-3}, minimizing on-resistance for breakdown voltages in the range of [20–80] V. We verified our analytical finding with a large number of TCAD simulations (more than 2,000 devices) and we determined that the 2nd order approximation yields a FOM_{LDMOS} that is up to 4π better than Baliga's FOM.

The proposed figure-of-merit in this study can be used as a new target line for device designers. Engineers can improve their device characteristics using the advantages of the proposed field oxide configuration and increase their device performance.

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