Received 11 January 2022; revised 27 March 2022; accepted 28 March 2022. Date of publication 21 April 2022; date of current version 16 June 2022.
The review of this article was arranged by Editor A. Escobosa.

Digital Object Identifier 10.1109/JEDS.2022.3165877

Fully Depleted SOI Technology for Millimeter-Wave Integrated Circuits

JEAN-PIERRE RASKIN (Fellow, IEEE)

Department of Electrical Engineering, Institute of Information and Communication Technologies, Electronics and Applied Mathematics,
Université catholique de Louvain, 1348 Ottignies-Louvain-la-Neuve, Belgium

CORRESPONDING AUTHOR: J.-P. RASKIN (e-mail: jean-pierre.raskin@uclouvain.be)

This work was supported by Ecsel JU Project "Beyond5" through EU H2020 and Innoviris, Brussels, Belgium, under Grant 876124.

ABSTRACT Performances of high-frequency integrated circuits are directly linked to the analog and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate. Today, Partially Depleted Silicon-on-Insulator (SOI) MOSFET is the mainstream technology for RF SOI systems. Fully Depleted (FD) SOI MOSFET is foreseen as one of the most promising candidates for the development of future lower power wireless communication systems operating in the millimeter-wave range. The high frequency performances of FD SOI transistors are presented at room but also at cryogenic and high temperature. Recently published results for FD SOI switches and low noise amplifiers are summarized. And finally, the potential interest and challenges to move from standard to high resistivity FD SOI substrates are discussed.

INDEX TERMS RF CMOS, silicon-on-insulator (SOI) technology, fully depleted (FD) SOI transistor, RF and millimeter-wave performance, high temperature, cryogenic temperature, RF switches, LNA, silicon-based substrate, high resistivity Si substrate.

I. INTRODUCTION

Radio Frequency (RF) performance of an integrated circuit (IC) does not only depend on the analog and high frequency characteristics of the active devices, i.e., the transistors, but also the quality of the back-end of line (BEOL) process which defines the losses along the interconnection lines and the quality factor of the passive elements such as the inductors and metal-insulator-metal (MIM) capacitors, as well as the electromagnetic properties of the substrate on which the RF IC is lying.

The parasitic resistances (metal lines and vias) and capacitances (dielectric layers) along the interconnections constitute a low-pass filter which drastically limits the operational frequency of ICs [1]. Advanced BEOL process provides higher number of metal lines, thicker metal layers for the top levels, low-k dielectric interlayers and denser vias using carbon nanotubes which are investigated for diminishing the parasitic resistances between metal layers [2], [3]. The substrate losses, crosstalk and non-linearities remain the major challenges for designing high-performance RF ICs in Si-based technologies. The root cause of missing RF performance of high-resistivity (HR) Silicon-on-Insulator (SOI) substrate was found by demonstrating the existence of a parasitic surface conduction (PSC) [4], [5] below the buried oxide (BOX) and one efficient way to disable it by introducing traps. In 2005, the possibility of creating SOI substrates characterized with an effective resistivity [6] as high as 10 kΩ.cm thanks to the introduction of a thin undoped polysilicon layer below the BOX of a HR SOI substrate was demonstrated [7].

Today, Partially Depleted (PD) SOI transistors with a channel length of 90 or 130 nm combined with a HR trap-rich SOI substrate is the mainstream technology for RF ICs. New generation of mobile communication systems such as 5G require higher cut-off frequency for the system, better linearity and lower power consumption. Moreover, the integration of high-quality inductors requires higher number and thicker metal layers. To fulfil those requirements, RF SOI must move to shorter nodes. Fully Depleted (FD) electronic regime is a promising approach to continue the scaling down of MOSFETs while controlling the short channel effects (SCE). In order to limit SCE, the channel thickness must be approximately 1/4 and 2/3 of the channel length, respectively, in the case of ultra-thin body and

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

buried oxide (UTBB) and FinFET. Technological aspects, electrostatics, scalability and variability issues in UTBB FD-SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [8], [9].

In this paper, the low-power feature and high-frequency performance of FD SOI at room but also at cryogenic and high temperature are presented. State-of-the-art switches and low noise amplifiers (LNAs) designed in FD SOI are summarized and the impact of different FD SOI back gate configurations on the high frequency behavior of switches is highlighted. The potential interest but also the challenges related to the move from standard to high resistivity SOI substrate are briefly discussed before concluding.

II. LOW-POWER AND HIGH-FREQUENCY PERFORMANCE OF FD SOI TRANSISTORS

Thanks to its low power features and technological maturity, FD SOI is a prime candidate for Internet-of-Things (IoT) applications, that will for the most part require low data throughput, but in which low-power is essential, as well as large volume manufacturing capabilities at low cost. Indeed, thanks to its high ratio of transconductance to drive current (g_m/I_d) FD SOI can significantly reduce consumption in analog and RF circuits such as power amplifiers and RF dividers. Moreover, the FD flavor of SOI technology can produce very short devices with quite low threshold voltages that are desirable for low-power and IoT applications. For a given off current target, FD SOI can have a lower threshold voltage (V_T) than bulk MOSFET counterparts, and thus can provide the same drive current at lower supply voltage (V_{DD}), resulting in reduction in both active power (proportional to V_{DD}^2) and standby power (proportional to V_{DD}).

To enable the designs of low power and high-performance Systems-on-Chip (SoCs), it is essential for a technology platform to offer transistors with a wide range of threshold voltage options V_T. In conventional bulk CMOS, multi-V_T options are mainly achieved through the use of different channel doping options. However, such a technique has disadvantages when implemented in advanced nodes because the (short) channel's electrical behavior becomes more sensitive to random doping fluctuations (RDF). But, in FD SOI, devices of various V_T can be built by employing different doping polarities of the wells created beneath the thin BOX, while preserving an undoped channel (uniform 10 Ω.cm P-type from SOI wafer providers) and minimizing RDF. This scheme is represented in Fig. 1, and switching the polarity of the well produces a shift of approximately 100 mV in the V_T of the transistor [8], [9], for usual UTBB-FD-SOI BOX thicknesses of 20 to 25 nm. Regular V_T devices (RVT) are obtained using conventional wells (well polarity opposite to S/D polarity), while flipped wells (well polarity the same as S/D polarity) are used to obtain low V_T devices (LVT). Furthermore, these doped wells beneath the BOX layer can be electrically contacted to define the so-called back-gate contact, as is shown in Fig. 1. Then,

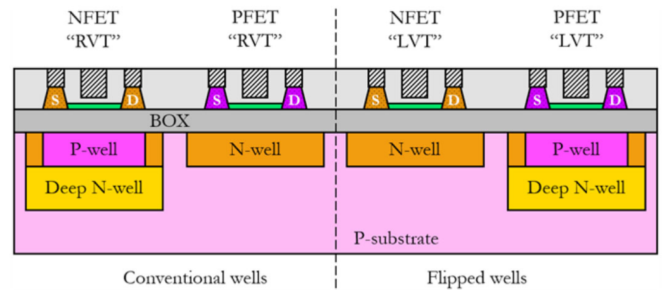

FIGURE 1. FD SOI transistors built over conventional and flipped wells.

transistor V_T can be tuned even further by applying different well biases. Applying well biases up to ±3 V produces V_T control of up to ±250 mV. Forward biasing a flipped well device will yield a low V_T (LVT) transistor, and reverse biasing a conventional well will yield a high V_T device (HVT). While a constant well bias produces a fixed V_T, a dynamic biasing scheme may be implemented to manage device and circuit power consumption. Such schemes are very attractive to reduce standby power consumption when the circuit is in the idle-state.

The aggressive and continuous gate-length downscaling of MOSFETs those last decades, which has proved beneficial to digital circuits, has resulted in tremendous reduction of the gate capacitance controlling the carriers in the channel and in a great enhancement of the transconductance, thereby leading to very high cut-off frequencies. Nowadays, the most advanced PD (45 nm) and FD SOI (28 nm and 22 nm) nodes are boasting speed metrics that are entirely sufficient for RF and even mm-wave applications. Fig. 2 presents the state-of-the-art current gain cut-off frequency f_t and maximum oscillation frequency f_{max} for N-type SOI MOSFETs as a function of gate length [10], with the dashed lines being the prediction from the International Technology Roadmap for Semiconductors (ITRS) [10]. Silicon-based devices are inherently slower than III-V transistors due to naturally lower carrier mobility. However, the mobility in silicon MOSFETs can be enhanced for electrons in N-FETs (holes in P-FETs) by applying tensile (compressive) strain to the device's channel using silicon-carbide (silicon-germanium) S/D regions. SOI devices with strained channels therefore present boosted f_t and f_{max} metrics, as shown in Fig. 2. Despite the lower carrier mobility in silicon compared with III-V materials, silicon MOSFETs can be considered as a competitive technology for high frequency applications, with cut-off frequencies and maximum oscillation frequencies in the 300 to 400 GHz range, easily enabling key telecommunications modules at millimeter-wave frequencies up to 100 GHz.

In [11], [12], the impact of back-gate biasing to DC and high frequency performance of 22 nm (22FDX from GlobalFoundries) and 28 nm FD SOI (from ST-Microelectronics) is presented. The front-gate and the back-gate cut-off frequencies f_t and f_{max} were extracted from the four-port S-parameters data. The maximum achieved

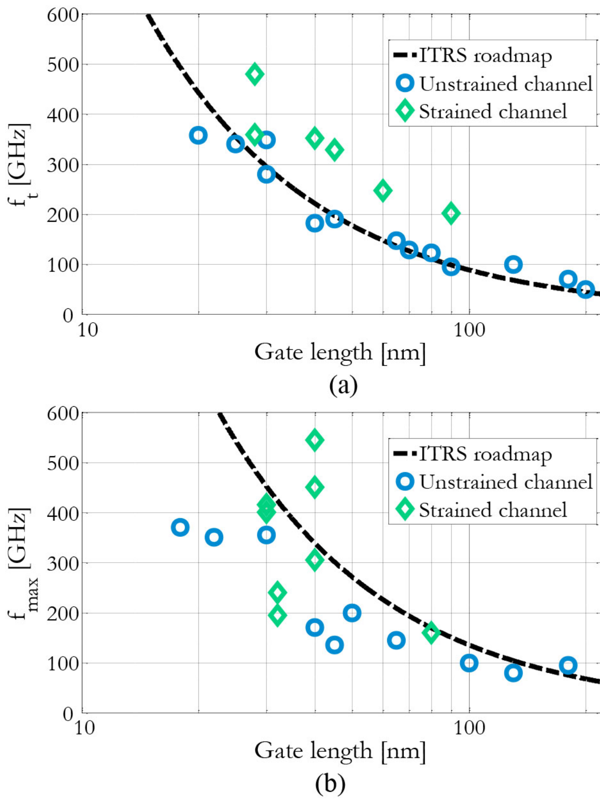

FIGURE 2. **(a) Current gain cut-off frequency f_t and (b) maximum oscillation frequency f_{max} as a function of gate length for state-of-the-art unstrained and strained SOI NMOSFETs.**

front-gate/back-gate f_t and f_{max} for the 22FDX NFET is 350/85 GHz and 370/23 GHz, respectively. In [13], 22FDX technology demonstrated a tunable HF noise parameter by using the back-gate biasing to achieve best-in-class minimum noise figure of 2.8 dB at 94 GHz.

In [14], the effect of the back-gate bias (V_{bg}) on non-linearity of the 28 nm FD SOI device is studied by means of 2nd and 3rd harmonic distortions (HD2 and HD3) extracted from DC I-V curves as well as from large-signal RF measurements using 1-dB and third-order intercept (IP3) points. It is shown that the non-linearity is reduced by applying a positive back-gate bias providing, e.g., 10-30 dB drop in HD2, 3-5 dB in HD3, depending on bias/current conditions as well as output-referred 1-dB compression and IP3 points increase by 1.2 dB and 1 dB, respectively. The reduction of non-linearity by the positive V_{bg} application can be understood in terms of "effective" body factor and mobility behaviors as a function of V_{bg}.

Besides the advantages of the thin undoped Si channel and the back-gate contact, FD SOI unfortunately suffers from self-heating issues because of the BOX that strongly increases the thermal isolation of the channel from the bulk Si substrate [15]. In [16], self-heating and its impact on analog performance were studied and compared for 28 nm technology bulk and FD SOI devices. The extracted thermal resistance (R_{th}) in FD SOI devices is significantly higher than in bulk devices, in the shortest 28 nm gate length devices, R_{th} of 143 and 42 K·μm/mW, have been experimentally measured for, respectively. Self-heating causes variation of analog figures of merit in the wide frequency range. This variation is considerably stronger in FD SOI devices than in bulk. Nevertheless, the voltage gain in FD SOI transistors remains larger than in bulk by 5 – 20 dB depending on the gate length and frequency. Therefore, FD SOI outperforms bulk in a wide frequency range. While thermal effects are stronger in FD SOI, their influence on device parameters is limited.

In order to mitigate the self-heating in advanced FD SOI transistors, Halder *et al.* in [17] proposed to build a heat-evacuator (heat sink) in the rich BEOL. A reduction of thermal resistance (and hence temperature rise) by ~20-30% in the case of a sink connected to the gate in comparison to it being left floating with respect to the gate has been experimentally demonstrated. While this study has been conducted on FD SOI MOSFETs, the idea of using a heat sink in the BEOL can be extended to other technologies. It is worth emphasizing that proposed configuration has two advantages: (i) it does not alter the area occupied by the devices /circuit and (ii) it does not degrade the gate resistance (but rather improve it).

III. LOW AND HIGH TEMPERATURE PERFORMANCE OF FD SOI

Apart from space applications, cryogenic studies are nowadays strongly motivated by a breakthrough in silicon-based quantum bits (qubit) which requires their co-integration with the control blocks and read-out electronics for the realization of quantum computers [18], [19]. Advanced FD SOI CMOS is a viable solution for quantum-integrated circuits as the implementation of qubits is compatible with this platform and just additionally requires a few non-standard process steps, like e-beam lithography [20], [21].

Recently, in [22], RF characterization of 28-nm FD SOI NMOSFETs at cryogenic temperatures down to 4.2 K was conducted. An improvement of up to ~130 GHz in f_t and ~75 GHz in f_{max} was observed for the shortest device (25 nm) at low temperature. The temperature evolution of the RF figures of merit (FoMs) is mainly explained in terms of mobility enhancement (improvement of 40% in intrinsic transconductance) and gate resistance reduction (~30%).

The RF performance of 28 nm FD SOI transistors at cryogenic temperature under low bias conditions was also investigated in [22]. Fig. 3 shows the f_t and f_{max} of the different devices at room (300 K) and cryogenic (4.2 K) temperatures at a low V_{ds} bias of 0.6 V. Operating at lower V_{ds} reduces power dissipation and thereby self-heating, which is a key concern for circuits aiming quantum computing [23]. Despite an overall reduction of approximately 13-20 % in f_t and f_{max}, compared to the nominal V_{ds} of 1 V, the devices are still operating incredibly well.

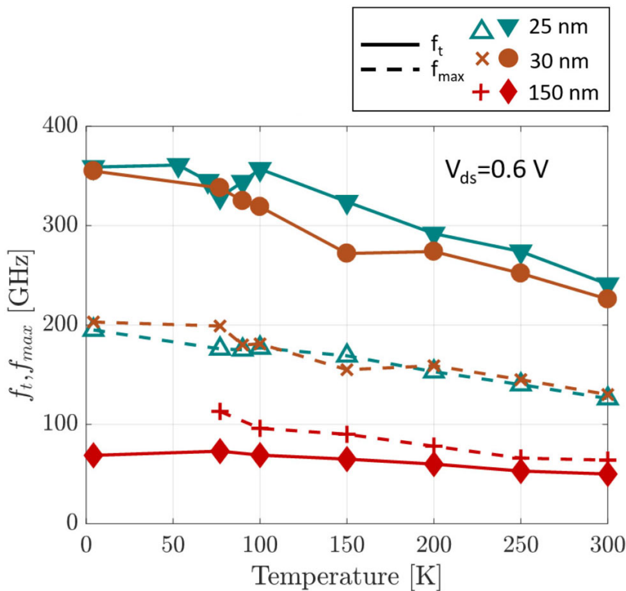

FIGURE 3. f_t (solid lines) and f_{max} (dashed lines) extracted from extrapolation from 300 K down to 4.2 K for the 25 nm (blue), 30 nm (brown) and 150 nm-long (red) devices at V_{ds} = 0.6 V and V_{gs} corresponding to $g_{m,max}$. The devices are still operating in saturation at V_{ds} = 0.6 V [22].

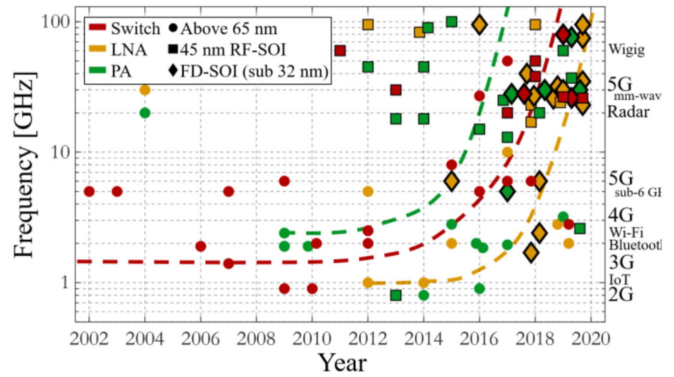

FIGURE 4. Literature review over time of SOI technologies for RF and millimeter-wave circuit elements of Front-End Modules (FEMs).

The RF FoMs are well above the values needed for quantum readout circuits for a ∼50% reduced power dissipation passing from 41.2 mW (V_{ds} = 1 V) down to 20.7 mW (V_{ds} = 0.6 V).

With the enormous increase of electronics components in vehicles, automotive ICs located close to the engine, for instance, are subject to high temperature environment [24]. In [25], the effect of increased temperature up to 175°C on the 22 nm FD SOI MOSFET devices' RF and mm-wave performance metrics are presented through on-wafer measurements and extractions. The transistor threshold voltage (V_T) was seen to reduce by 0.6 mV/°C over the temperature range of 300 to 450 K. When increasing the operating temperature from 300 to 450 K, a reduction of 21% and 14% was observed, respectively, for f_t and f_{max}. The degradation in the gate transconductance with temperature was found to be one of the major factors for the reduction in the aforementioned RF FoMs. Interestingly, there is a bias point at which the transconductance value of the transistor does not vary with temperature. That specific bias condition is named the zero-temperature coefficient (ZTC) operating point of the transistor [26], [27]. As demonstrated in [28], [29], when the temperature stability of the RF performance of an IC is required, the transistors must not be biased at the peak of transconductance but at the transconductance ZTC point. Obviously, the price to pay is a slight degradation of the transistor RF performance. For the nominal gate length of the 22FDX NFET, f_t at room temperature decreases approximately by 15% when the transistor is not biased at the peak of transconductance but at ZTC point [25].

IV. HIGH FREQUENCY FRONT-END MODULE IN SOI CMOS

Tremendous research effort has been dedicated to RF-SOI driven by large volume applications requiring inexpensive single-chip transceivers (switches, LNAs, PAs, etc.), including both at the base-band and the RF front ends. To highlight this, Fig. 4 presents a historical review of SOI technologies for RF and mm-wave applications.

Integrated switches were the first SOI modules for RF applications, hitting the market around 2007 and dominating it for handsets by 2012. In 2019, most RF switches found in smartphones in consumer hands are implemented in the 180 nm and 130 nm nodes on specially engineered RF substrates named enhanced Signal-Integrity high-resistivity SOI substrates (eSI) produced and sold by the French company SOITEC. The success of that Si-based technology for RF switches is mainly related to the RF performance of its substrate providing low insertion loss, good isolation and great linearity, all of those features at low cost. Indeed, substrate linearity impact is directly observed on switch performance. The DC-5 GHz Single Pole Double Throw (SPDT) switch module in [30], implemented using a 180 nm PD-SOI technology node from TowerJazz18, is depicted in Figure 5a. The switch is measured using the same harmonic distortion setup described in [31], [32]. Identical SPDT circuit modules are implemented on two types of SOI substrates, a HR SOI and an RFeSI90 TR-SOI. The switch is measured under large signal at 900 MHz in the ON-state from the Tx port to the Antenna port, while the Rx port is loaded to 50 Ω. The harmonic distortion results are given in Figure 6b. It is shown that approximately 20 dB of linearity increase is achieved by substituting the HR substrate with a TR RFeSI90 substrate, highlighting the substrate's impact on overall signal distortion in RF modules.

Significant research interest and industry development pushed the RF SOI nodes even further, down to the 45 nm PD-SOI node, truly optimized for RF performance, and beyond, to sub-30 nm FD-SOI nodes. These advanced PD-SOI and FD-SOI technologies boast cutoff and oscillation frequencies in the range of 400 GHz. With these performances other key RF circuit elements emerged in the

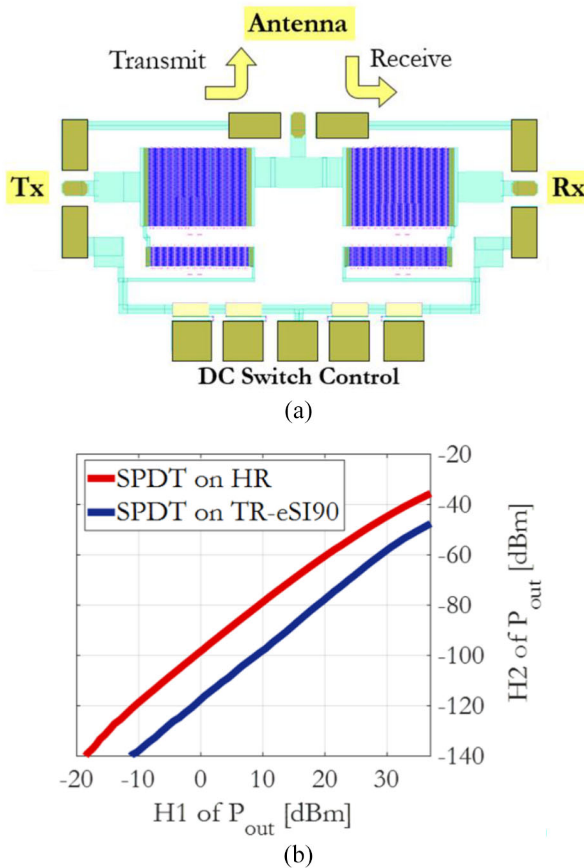

FIGURE 5. Harmonic distortion of a DC-5 GHz SPDT module in 180 nm PD-SOI technology on two types of substrate, HR and TR SOI [30]. (a) Switch layout. (b) Power of second harmonic (at 1.8 GHz) component H2 plotted versus power of fundamental component (at 900 MHz) of the output of an SPDT RF switch PD-SOI implemented on HR and TR SOI substrates. The switch is in the state that connects Tx to Antenna. The large signal is introduced at the Tx port, and the harmonics are measured at the Antenna port. The Rx port is loaded to 50 Ω.

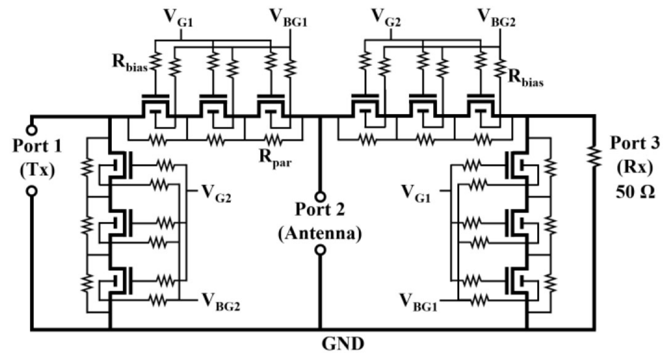

FIGURE 6. Schematic of the designed SPDT switches.

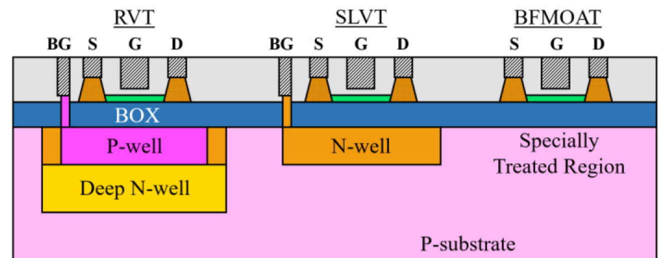

FIGURE 7. Simple representation of the three different flavors of UTBB-FD-SOI devices considered for the implementation of the mm-wave SPDT switches. The source (S), drain (D), gate (G) and back-gate (BG) terminals are depicted.

literature, starting from around 2010-2012 for low-noise amplifiers (LNAs) and power amplifiers (PAs). The partially depleted 45 nm RF-SOI process from GlobalFoundries has demonstrated its strong potential for RF and mm-wave circuits. Fig. 4 shows the emergence of this technology around 2012, implementing RF functions such as VCOs, LNAs, PAs and switches at millimeter wave frequencies up to 100 GHz, and this process is commercially available to the industry as of late 2017. Integrated on low-loss and highly linear trap-rich substrates from SOITEC, this process is truly optimized for RF purposes allowing high-quality interconnects, transmission lines and passives (inductors, transformers, etc.) along with strong substrate isolation and linearity [33]. Around 2015, IC demonstrator circuits in 22 nm and 28 nm UTBB FD-SOI processes (from GlobalFoundries and ST-Microelectronics or Samsung, respectively) were developed, and interest in these technologies for high frequency applications has increased significantly since then. In particular, Fig. 4 clearly reveals a focus at 28 GHz in the recent FD-SOI research literature. While 45 nm RF-SOI has a strong application focus at the millimeter-wave (above approximately 20 GHz) bands (due to its high speed and optimized substrate and process), FD-SOI nodes also find applications at lower frequencies (sub-6 GHz) where their RF performances can be tuned down to remain sufficient for IoT type RF applications but at ultra-low power consumption.

More recently, FD SOI is gaining interest for millimeter wave switches. In [34], the design of ultra-wideband SPDT switches (Fig. 6) targeting the Ka-band fabricated using the 22FDX technology has been presented. Three types of SPDTs were designed, based on the three key mm-wave FET devices offered by the foundry library (Fig. 7): (i) the conventional-well device with regular-V_T (RVT), (ii) the flipped-well devices with super-low-V_T (SLVT), and (iii) the BFMOAT which lacks the back-gate contact as the substrate region directly beneath the BOX is specially treated in order to reduce substrate parasitics [35]. The devices are compared in terms of SPDT FoMs, with a focus on the impact of back-gate bias.

The SPDT switches were designed based on a series-shunt topology, as shown in Fig. 6, for wideband functionality. The designs were made to achieve the lowest possible insertion-loss (IL) while maintaining an isolation (ISO) of 30 dB at 28 GHz. A stack of three transistors was used in each branch targeting 20 dBm of input power 1-dB compression point. NFET devices with 20 nm nominal gate length were used to implement the SPDTs. The total transistor width chosen

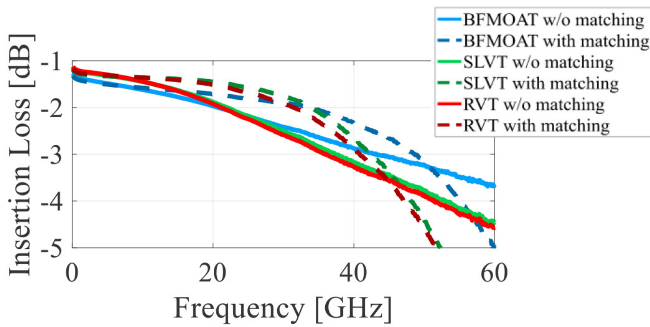

FIGURE 8. Measured insertion loss for the three SPDT switches. The applied back-gate bias is $V_{bg1} = 3$ V and $V_{bg2} = 0$ V for the RVT and SLVT switches.

to achieve these specifications are W_{series} of 72 μm and W_{shunt} of 29.4 μm. The bias resistors at the gate and back-gate terminals are 9.20 kΩ, and the resistors in parallel with the FETs are 2.45 kΩ.

In [34], all devices have been compared at 28 GHz under both small- and large-signal analysis. At 28 GHz, the SLVT device outperforms both the RVT and BFMOAT in all small- and large-signal FoMs. This is because the SLVT can attain the lowest threshold voltage, which has the simultaneous impact of lowering IL and increasing P1dB and IIP3.

However, the IL curves in Fig. 8 show that the BFMOAT device has slower IL roll off versus frequency, thanks to its lower parasitics. This is supported by the conclusions from [35], and marks the BFMOAT device as the preferred choice over SLVT and RVT for mm-wave switches in the 40-100 GHz range. In the lower frequency range RVT and SLVT switches outperform the BFMOAT ones thanks to an applied back gate bias, that enables them to achieve approximately 0.2 dB advantage in IL from DC to 20 GHz. The IL of SLVT with back-gate biasing is lower than that of BFMOAT up to around 34 GHz for the designs presented in [34] with matching, and up to around 26 GHz for the unmatched design. The applied bias that improves IL also simultaneously enhances P1dB and IIP3, by 1 dBm and 4 dBm, respectively.

In [36], it has been demonstrated that shunt parasitics are non-negligible contributors to FET performance for mm-wave switch applications and complement the well-known $R_{on}.C_{off}$ figure of merit for FET benchmarking, as $R_{on}.C_{off}$ contains information only on the series Y-parameter Y_{21}. While the imaginary parts of shunt admittances can be compensated for with matching circuits, the real parts cannot, and will always be a source of S_{21} degradation (insertion loss) in all of the most common switch topologies. The importance of shunt loss was demonstrated by analyzing how a BFMOAT device outperforms an SLVT as a mm-wave switch despite having a significantly larger $R_{on}.C_{off}$. Based on this understanding, a wideband DC-80 GHz SPDT switch was designed and fabricated to showcase the BFMOAT's low shunt-parasitic performance. On-wafer measurements demonstrate this SPDT to be competitive over this band, with an insertion loss of 2.6 (2.1) dB at 80 (60) GHz, and an isolation of 25 (21) dB at 80 (60) GHz, for a of P1dB = 19.9 dBm and IIP3 of 33.6 dBm. As highlighted in [36], those performances are quite competitive when compared with the state-of-the-art mm-wave SPDT modules operating close to 60 and/or 80 GHz.

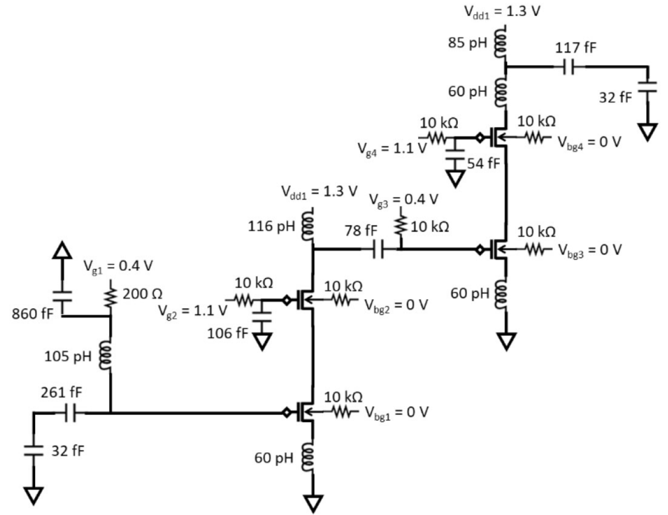

FIGURE 9. Schematic of the 2-stage LNA.

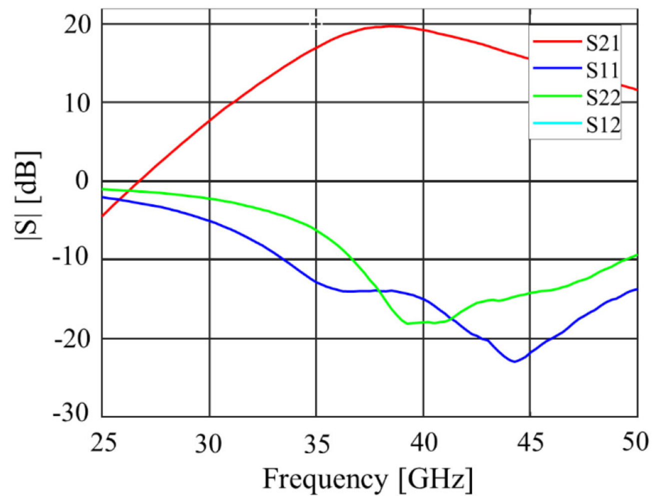

FIGURE 10. S-parameters measurements of the 2-stage LNA.

In [37], a 2-stage low noise amplifier (LNA) with 22FDX SLVT transistors including degenerate source inductors is demonstrated at 39 GHz (Fig. 9). The back-gate of each transistor is biased individually in order to fine tune the LNA performance. The SLVT NFETs have a channel length of 20 nm, a finger width of 0.5 μm and a total width of 60 μm. For a power consumption of 20.8 mW, the characteristics of the LNA are: a measured peak gain of 19.9 dB at 39 GHz, a 3-dB bandwidth from 34.9 to 43.3 GHz, a return loss less than −10 dB from 36.7 to 49.5 GHz, a RF noise figure (NF) of ∼2.6 dB at 39 GHz and lower than 3 dB from 34.5 to 48 GHz.

V. HIGH RESISTIVITY FD SOI SUBSTRATE

Today, all the ICs based the FD SOI technology are fabricated in starting with a SOI substrate which includes a handle Si substrate characterized by a standard resistivity of around 10 Ω.cm. At high-frequencies the thin dielectric layers isolating the metal interconnects, passives, and transistors from the substrate become transparent by their capacitive nature, and significant electric fields from these devices penetrate into the silicon substrate, inducing losses and strongly impacting the values of parasitic coupling elements. To minimize as much as possible losses along interconnection lines and also to mitigate parasitic coupling between integrated circuits on the same substrate, it has been demonstrated that it is important for the underlying substrate to have a high effective resistivity [38]. Low-doped silicon is then favored with high nominal resistivity (ρ_{nom}) above 1 kΩ.cm. However, the effective resistivity (ρ_{eff}), i.e., which is sensed by the overlying planar circuits, can differ strongly from the nominal resistivity ρ_{nom} due to band bending effects at the semiconductor/insulator interface that severely reduce the local resistivity, greatly impacting the overall sensed ρ_{eff}. The resistivity of semiconductors is by nature dependent on the local electric field (and we call this the field-effect). Low-doped high-resistivity (HR) substrates are particularly field-sensitive, and it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. The most common parasitic fields originate from fixed charges (usually positive in Si/SiO_2 heterostructures) that are present at the insulator/semiconductor interface. Then, a highly conductive channel-like layer is induced beneath the insulator [5], [6]. These charges are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This in turn lowers the sensed effective resistivity by a factor of 10 to 10^4, to values as low as 1 Ω.cm (Fig. 11). This is referred to as the parasitic surface conduction (PSC) effect that renders the use of a HR substrate ineffective for improving the performance of overlying RF-ICs as compared to standard-doped (Std) silicon ($\rho_{nom} \approx 10$ Ω.cm).

A breakthrough in this area was made in the early 2000's with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide in SOI technology [7]. This layer effectively mitigates the PSC effect by pinning the Fermi level near mid-gap at the interface in a highly resistive state, enabling ρ_{eff} values of over 1 kΩ.cm.

In order to evaluate harmonic distortion originating from the substrate, a simple CPW line structure is employed, a single tone with fundamental frequency of 900 MHz is injected into one port of the CPW line. The power of this input tone, which we shall denote as H'1, is swept from −30 dBm to +25 dBm using 50 Ω reference port impedances, and the output signal is retrieved and analyzed in terms of its frequency components. Due to the non-linear behaviour of silicon-based substrates signal distortion is introduced and the output signal is in general a multi-tone signal, with a fundamental component, denoted as H1, along with harmonic components at all integer multiples of this fundamental frequency, denoted as H2 (at 1.8 GHz), H3 (at 2.7 GHz) and so on [39]. Fig. 11 plots the H2 component for increasing fundamental output power H1 obtained from on-wafer measurements of a 2.1 mm-long CPW line on the three types of SOI substrates under consideration. Large voltage signals modify the free carrier distributions in the underlying silicon substrate, as it is pulsed through inversion / depletion / accumulation states over time in response to the large signal (the field effect). This leads to relatively high harmonic distortion at the output of the CPW line, induced by the voltage-sensitive Std and HR silicon substrates.

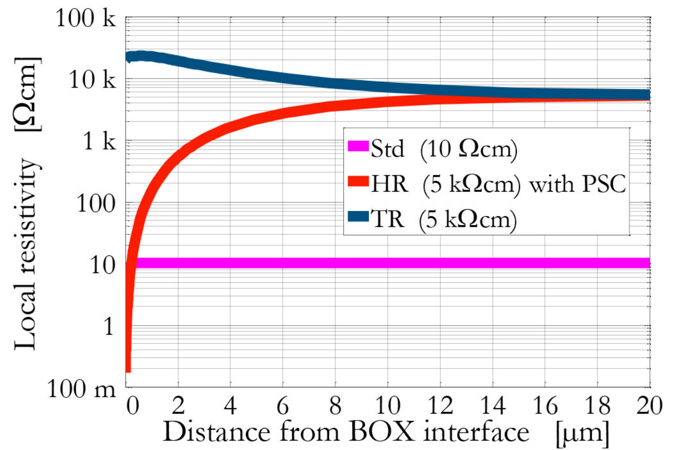

FIGURE 11. Resistivity profiles in the semiconductor volume beneath the BOX layer for a standard-resistivity substrate (10 Ω.cm), a high-resistivity substrate (5 kΩ.cm), and a trap-rich substrate (5 kΩ.cm bulk + 2 μm-thick polysilicon rich in traps at BOX interface). All profiles include the presence of interfacial oxide charges with a density of 10^{11} cm^{-2}.

The introduction of the polysilicon trap-rich layer beneath the BOX of a nominally high resistivity substrate brings reductions of 40 to 60 dB in the total distortion over the measured power range (Fig. 12). The traps at the Si/SiO_2 interface effectively pin the Fermi-level near mid-gap. Contained to a narrow energy range by these traps, the position of the Fermi-level is rendered much less voltage-sensitive, improving the linearity of the substrate and reducing the substrate-induced distortion in signals propagating through overlying transmission lines. More in-depth description and modeling of the non-linear behaviour of semiconductor substrate over a wide frequency band can be found in [40], [41].

Today's success of PD-SOI technology for RF ICs is mainly due to significant technological improvements at the substrate level brought by the trap-rich substrates developed by SOITEC, also named eSI, which stands for enhanced Signal-Integrity. Different flavors of eSI trap-rich wafers can be found on today's market. The eSI80 product presents a

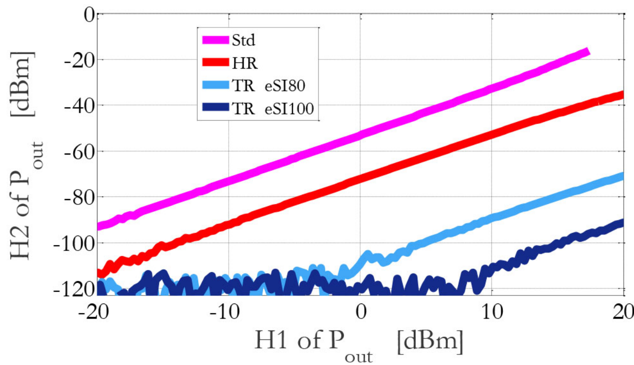

FIGURE 12. Power of second harmonic (at 1.8 GHz) component H2 plotted versus power of fundamental component (at 900 MHz) of the output signal of a 2.1 mm-long CPW line (central conductor width of 26 μm and a spacing of 12 μm between conductors) implemented on the considered types of SOI substrates.

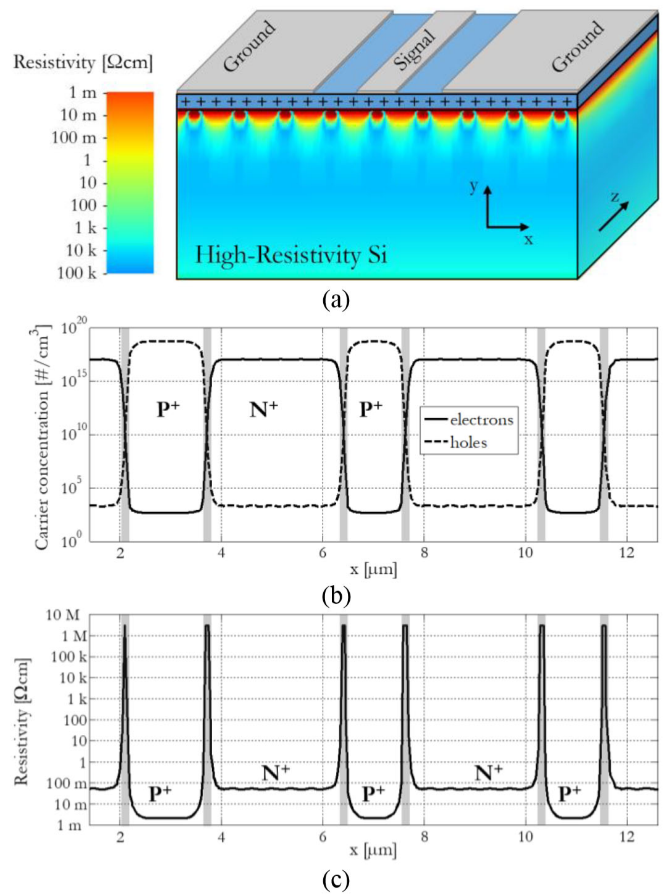

FIGURE 13. (a) 2D resistivity profile in a DP substrate upon which a CPW line is defined. Fixed positive oxide charges are represented by "+" symbols. (b) and (c) are the local carrier concentration and resistivity profiles in the x-direction at the BOX/Si interface where the buried PN junctions are defined. The depletion regions are shaded in grey.

low H2 distortion level at −80 dBm for a fundamental component H1 of +15 dBm, while the eSI100 boasts an even lower level at −100 dBm, thanks to a combination of a higher quality trap-rich polysilicon layer and a lower doping level of the Si handle substrate [33]. In today's market (2021), 300 mm-diameter SOI trap-rich wafers are commercially available for the most advanced PD-SOI nodes (180 nm to 45 nm) and used in front-end switching modules of virtually all modern-day smartphones.

As mentioned in the introduction, there is a clear move to FD SOI technology for targeting the new generations of mobile communication systems such as 5G requiring higher cut-off frequency for the system, better linearity and lower power consumption. Building on the commercial success of RF-SOI obtained through the development of trap-rich SOI substrates (eSI), researchers from academia and the microelectronics industry are working on the development of FD SOI substrates including a highly-resistive handle Si substrate of a few kΩ.cm. Similar to HR SOI substrates, we have to develop solutions to mitigate the PSC which will be present underneath the thin BOX. Contrary to the PD SOI technology, FD SOI transistors feature a back-gate contact, and therefore, integration issues exist between advanced FD-SOI nodes and trap-rich (TR) substrates due to the foreseen difficulty of defining back-gate contacts below the BOX within the polysilicon trapping layer.

Hereafter, a different solution from TR to counter the PSC effect in HR wafers, which is fully compatible with FD-SOI, and based on a smart array of P- and N-implants below the BOX is presented. The major idea is to locally interrupt the PSC channel by inducing a chain series of buried depletion junctions at the HR Si substrate / SiO_2 (BOX) interface. The functioning principle behind this type of depletion-enhanced (DP) substrate is illustrated in Fig. 13. A series of P and N regions are defined by ion implantation beneath the BOX (Figs. 13a and 13b). The depletion junctions induced between adjacent P and N regions serve to impede the field propagation in unwanted directions. Furthermore, the strong dopant concentration in these P and N regions is much less field sensitive, giving rise to an increase in substrate linearity. The conductive PSC path is interrupted, which results in an increase in substrate ρ_{eff} in the direction perpendicular to the buried junctions. The interruption of the interfacial conduction channel (PSC) with resistive depletion regions is highlighted by grey regions in Figs. 13b and 13c. Although the resistivity in the P and N regions is low, they come in series with the depleted junctions characterized by very low free carrier density that are, therefore, highly resistive. The overall impedance of the path through the substrate between signal and ground electrodes of the CPW line is dominated by the depletion regions that are shown in Fig. 13c to be highly resistive. The PN junctions should be placed normal to the desired direction of increased substrate impedance. An array-type configuration may be adopted, or a tailored layout to suit the needs of the overlying passive device.

In [42], CPW lines and crosstalk structures defined at a 90° angle to the doping lines, as shown in Fig. 14, have been deposited on high-resistivity (> 5 kΩ.cm) Si substrates into which alternative P and N doped regions, of different

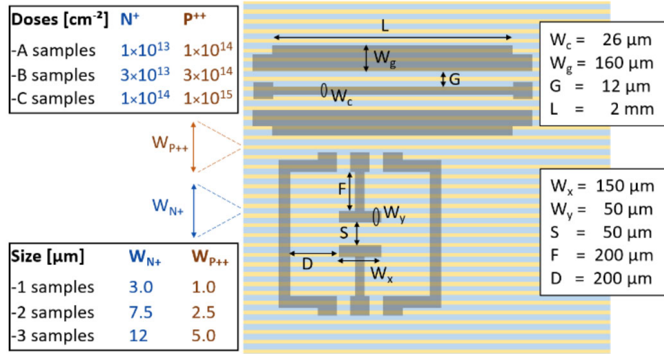

FIGURE 14. Pattern and sizing of the P and N doped regions relative to the CPW and crosstalk structures on the DP substrates.

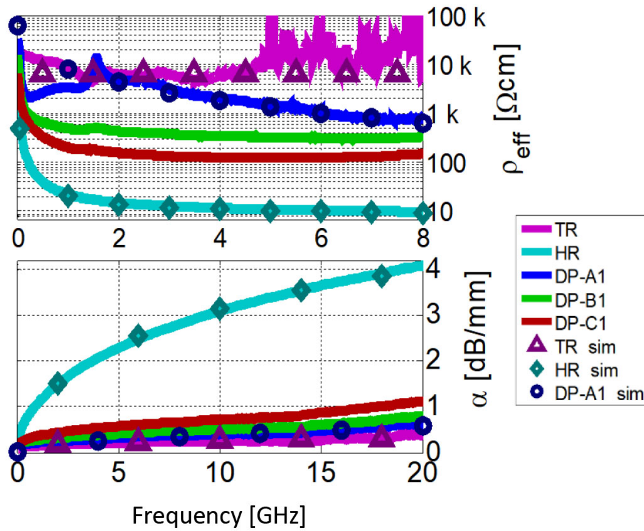

FIGURE 15. Effective electrical substrate parameters extracted from RF measurements of CPW-lines.

doping levels and dimensions, were defined by implantation to create depletion junctions.

From the measured S-parameters the RF line losses α and the effective resistivity ρ_{eff} were extracted (Fig. 15) up to 20 GHz. The DP substrates show increased performance compared to the HR wafer. The DP-A1 sample shows the best performance values of all nine DP wafers because it has the highest density of PN junctions between signal and ground lines in the CPW, and because it has the widest depletion junctions due to it using the lowest doping levels. It presents a high ρ_{eff} in the range of 2 kΩ.cm at 5 GHz and low RF losses. Large-signal measurements of the CPWs were also performed. A single tone with fundamental frequency of 900 MHz is injected into one port of the CPWs on each substrate. The power of this input tone H'1, is swept from −30 dBm to +25 dBm, and the output signal's components H1 (fundamental), H2 and H3 (second and third harmonics) are retrieved by a spectrum analyzer. The total harmonic distortion (THD) is plotted in Fig. 16. It is shown that the voltage sensitive HR sample is highly non-linear, whereas the CPW on the TR wafer shows low distortion. The DP

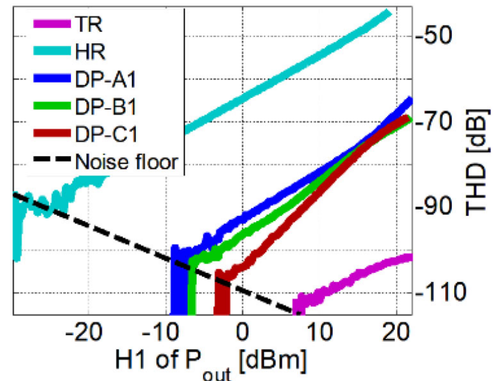

FIGURE 16. Total harmonic distortion level at the output of a 2 mm-long CPW line on various substrates.

substrates present intermediate results, achieving 30 dB total linearity increase over HR. The lower doped DP-A1 sample shows slightly higher THD due to slightly wider and more field sensitive depletion regions, highlighting therefore a slight trade-off between effective resistivity and linearity.

It is worth noting that the used P and N implants for the DP samples are quite similar than the ones existing in a full UTBB-FD-SOI process for defining the back-gate electrodes below-BOX wells. This technique to mitigate PSC in the case of FD SOI on HR Si is thus quite cost effective. It is also important to mention that the preliminary results presented in [42] were obtained with a lithography with a limited resolution of around 2 μm. Thus, the proportion of depleted volume in the interfacial silicon layer (P- and N-doped regions) for those samples was 7.4% (160 nm/2.16 μm). More recently, the concept has been tested with a more advanced fabrication process (180 nm photolithography resolution) at CEA-Leti enabling a higher density of depletion junctions (47%) to be defined in a given space, thereby increasing the substrate impedance even further to produce even better RF results [43].

Still based on the same concept of buried PN junctions, a spiral inductor's quality factor was shown to increase by placing a series of spiral depletion regions in between each turn of the inductor, because quality factor degradation is due to high coupling between adjacent spirals, which is facilitated by the conductive substrate or PSC effect [44].

VI. CONCLUSION

Today's success of PD-SOI technology for RF is due to significant technological improvements made at both the transistor and the substrate levels. In 2021, the 130 nm and 180 nm PD-SOI nodes on optimized RF substrates dominate the RF switch market in handheld smartphone devices.

The more advanced PD-SOI nodes (sub-100 nm) as well as the most advanced FD-SOI nodes (sub-30 nm) are demonstrating their potential for all kinds of RF and millimeter-wave functional blocks beyond RF switches (LNAs, PAs, VCOs, etc.) towards full SOI front-end module integration.

In the case of FD-SOI nodes, there is still some room of improvement for their high frequency performances thanks to the introduction of high-resistivity handle substrate in the near future. Furthermore, FD-SOI' ultra-low power capabilities are of significant interest toward IoT types of applications.

ACKNOWLEDGMENT

The author would like to thank Dr. Martin Rack, Dr. Valeriya Kilchytska, Dr. Babak Kazemi Esfeh, Lucas Nyssens, Massinissa Nabet for their overall research contributions to the study of RF-SOI substrates and circuit modules. A warm thanks to Dr. Frédéric Allibert and his colleagues from SOITEC, for providing high-quality RF-SOI substrate samples and invaluable technical discussions. Thanks to Pascal Simon from Welcome and Dr. Mostafa Emam from Incize for their help and contributions to high-frequency and non-linear RF on-wafer measurements.

REFERENCES

[1] J. S. Clarke, C. George, C. Jezewski, A. M. Caro, D. Michalak, and J. Torres, "Process technology scaling in an increasingly interconnect dominated world," in *Proc. Symp. VLSI Technol.*, 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894407.

[2] A. Ceyhan and A. Naeemi, "Cu interconnect limitations and opportunities for SWNT interconnects at the end of the roadmap," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 374–382, Jan. 2013, doi: 10.1109/TED.2012.2224663.

[3] S. Kincal, M. C. Abraham, and K. Schuegraf, "*RC* performance evaluation of interconnect architecture options beyond the 10-nm logic node," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 1914–1919, Jun. 2014, doi: 10.1109/TED.2014.2315572.

[4] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 1, pp. 10–12, Jan. 1999, doi: 10.1109/75.752108.

[5] D. Lederer and J.-P. Raskin, "Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers," *Solid-State Electron.*, vol. 47, no. 11, pp. 1927–1936, Nov. 2003, doi: 10.1109/MWSYM.2002.1011714.

[6] D. Lederer and J.-P. Raskin, "Effective resistivity of fully-processed SOI substrates," *Solid-State Electron.*, vol. 49, no. 3, pp. 491–496, 2005, doi: 10.1016/j.sse.2004.12.003.

[7] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 805–807, Nov. 2005, doi: 10.1109/LED.2005.857730.

[8] C. Fenouillet-Beranger *et al.*, "Impact of a 10 nm ultra-thin BOX (UTBOX) and ground plane on FD SOI devices for 32 nm node and below," *Solid-State Electron.*, vol. 54, no. 9, pp. 849–854, 2010.

[9] Q. Liu *et al.*, "Impact of back bias on ultra-thin body and BOX (UTBB) devices," in *Proc. Symp. VLSI Technol. Dig. Techn. Papers*, Honolulu, HI, USA, 2011, pp. 160–161.

[10] V. Passi and J.-P. Raskin, "Review on analog/radio frequency performance of advanced silicon MOSFETs," *Semicond. Sci. Technol.*, vol. 32, no. 12, Dec. 2017, Art. no. 123004, doi: 10.1088/1361-6641/aa9145.

[11] S. N. Ong *et al.*, "22nm FD-SOI technology with back-biasing capability offers excellent performance for enabling efficient, ultra-low power analog and RF/millimeter-wave designs," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Boston, MA, USA, 2019, pp. 323–326, doi: 10.1109/RFIC.2019.8701768.

[12] B. K. Esfeh *et al.*, "Back-gate bias effect on FDSOI MOSFET RF figures of merits and parasitic elements," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon–ULIS*, Athens, Greece, Apr. 2017, pp. 228–230, doi: 10.1109/ULIS.2017.7962569.

[13] Q. H. Le *et al.*, "W-band noise characterization with back-gate effects for advanced 22nm FDSOI mm-wave MOSFETs," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Los Angeles, CA, USA, 2020, pp. 131–134, doi: 10.1109/RFIC49505.2020.9218369.

[14] B. K. Esfeh *et al.*, "Back-gate bias effect on UTBB-FDSOI non-linearity performance," in *Proc. 47th Eur. Solid-State Device Conf. (ESSDERC)*, Leuven, Belgium, Sep. 2017, pp. 74–77, doi: 10.1109/ESSDERC.2017.8066613.

[15] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, J. T. Bunyan, and M. J. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996, doi: 10.1109/16.544417.

[16] S. Makovejev, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Comparison of self-heating and its effect on analogue performance in 28 nm bulk and FDSOI," *Solid-State Electron.*, vol. 115, pp. 219–224, Jan. 2016, doi: 10.1016/j.sse.2015.08.022.

[17] A. Halder, L. Nyssens, M. Rack, D. Lederer, J.-P. Raskin, and V. Kilchytska, "Heat sink implementation in back-end of line for self-heating reduction in 22 nm FDSOI MOSFETs," *Solid-State Electron.*, vol. 184, Oct. 2021, Art. no. 108088, doi: 10.1016/j.sse.2021.108088.

[18] E. Charbon *et al.*, "Cryo-CMOS for quantum computing," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, p. 13, doi: 10.1109/IEDM.2016.7838410.

[19] P. Galy, J. C. Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Pioro-Ladrière, "Cryogenic temperature characterization of a 28-nm FD-SOI dedicated structure for advanced CMOS and quantum technologies co-integration," *IEEE J. Electron Devices Soc.*, vol. 6, no. 6, pp. 594–600, May 2018, doi: 10.1109/JEDS.2018.2828465.

[20] R. Maurand *et al.*, "A CMOS silicon spin qubit," *Nature Commun.*, vol. 7, Nov. 2016, Art. no. 13575, doi: 10.1038/ncomms13575.

[21] L. Hutin *et al.*, "Si CMOS platform for quantum information processing," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573380.

[22] L. Nyssens *et al.*, "28-nm FD-SOI CMOS RF figures of merit down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 646–654, 2020, doi: 10.1109/JEDS.2020.3002201.

[23] L. Nyssens *et al.*, "Self-heating in FDSOI UTBB MOSFETs at cryogenic temperatures and its effect on analog figures of merit," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 789–796, 2020, doi: 10.1109/JEDS.2020.2999632.

[24] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: High-temperature electronics," *IEEE Trans. Electron. Packag. Manuf.*, vol. 27, no. 3, pp. 164–176, Jul. 2004, doi: 10.1109/TEPM.2004.843109.

[25] A. Halder, L. Nyssens, M. Rack, V. Kilchytska, D. Lederer, and J.-P. Raskin, "22 nm FD-SOI MOSFET figures of merit at high temperatures upto 175°C," in *Proc. 22nd IEEE Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Las Vegas, NV, USA, Jan. 2022, doi: 10.1109/SiRF53094.2022.9720052.

[26] F. S. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors," *Electron. Lett.*, vol. 25, no. 17, pp. 1196–1198, Aug. 1989, doi: 10.1049/el:19890802.

[27] Z. D. Prijić, S. S. Dimitrijev, and N. D. Stojadinović, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectron. Rel.*, vol. 32, no. 6, pp. 769–773, Jun. 1992, doi: 10.1016/0026-2714(92)90041-I.

[28] M. Emam, D. Vanhoenacker-Janvier, and J.-P. Raskin, "Zero temperature coefficient of current gain cutoff frequency and maximum oscillation frequency for various SOI and Si bulk MOSFETs," *Electrochem. Soc. Trans.*, vol. 35, no. 5, pp. 129–134, May 2011, doi: 10.1149/1.3570787.

[29] M. Emam, D. Vanhoenacker, and J.-P. Raskin, "Partially depleted SOI versus deep N-well protected bulk-Si MOSFETs: A high-temperature RF study for low-voltage low-power applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1496–1504, Apr. 2013, doi: 10.1109/TMTT.2013.2250513.

[30] B. K. Esfeh, M. Rack, S. Makovejev, F. Allibert, and J.-P. Raskin, "A SPDT RF switch small- and large-signal characteristics on TR-HR SOI substrates," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 543–550, 2018, doi: 10.1109/JEDS.2018.2805780.

[31] D. C. Kerr, J. M. Gering, T. McKay, M. S. Carroll, C. Roda Neve, and J.-P. Raskin, "Identification of RF harmonic distortion on Si substrates and its reduction using a trap-rich layer," in *Proc. 8th Topical Meeting Silicon Monolithic Integr. Circuits RF Systems (SiRF)*, Orlando, FL, USA, Jan. 2008, pp. 151–154, doi: 10.1109/SMIC.2008.44.

[32] C. R. Neve *et al.*, "Impact of Si substrate resistivity on the non-linear behaviour of RF CPW transmission lines," in *Proc. 38th Eur. Microw. Week (EuMW)*, Amsterdam, The Netherlands, Oct. 2008, pp. 36–39, doi: 10.1109/EMICC.2008.4772222.

[33] F. Allibert *et al.*, "Engineering SOI substrates for RF to mmWave front-ends," *Microw. J.*, vol. 10, pp. 72–82, Oct. 2020,

[34] M. Rack, L. Nyssens, S. Wane, D. Bajon, and J.-P. Raskin, "DC-40 GHz SPDTs in 22 nm FD-SOI and back-gate impact study," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Los Angeles, CA, USA, Aug. 2020, pp. 67–70, doi: 10.1109/RFIC49505.2020.9218317.

[35] S. Yadav *et al.*, "Demonstration and modelling of excellent RF switch performance of 22nm FD-SOI technology for millimeter-wave applications," in *Proc. 49th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2019, pp. 170–173, doi: 10.1109/ESSDERC.2019.8901823.

[36] M. Rack, L. Nyssens, Q. Courte, D. Lederer, and J.-P. Raskin, "Impact of device shunt loss on DC-80 GHz SPDT in 22 nm FD-SOI," in *Proc. 51st Eur. Solid-State Device Conf. (ESSDERC)*, Grenoble, France, Sep. 2021, pp. 195–198, doi: 10.1109/ESSDERC53440.2021.9631835.

[37] L. Nyssens, M. Rack, D. Lederer, and J.-P. Raskin, "2-stage LNA at 39 GHz in 22 nm FD SOI," in *Proc. Eur. Microw. Week (EuMW)*, Milan, Italy, Sep. 2022.

[38] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, Dec. 1997, doi: 10.1109/16.644646.

[39] C. R. Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 924–932, Apr. 2012, doi: 10.1109/TED.2012.2183598.

[40] M. Rack, F. Allibert, and J.-P. Raskin, "Modeling of semiconductor substrates for RF applications: Part I-Static and dynamic physics of carriers and traps," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4598–4605, Sep. 2021, doi: 10.1109/TED.2021.3096777.

[41] M. Rack, F. Allibert, and J.-P. Raskin, "Modeling of semiconductor substrates for RF applications: Part II–Parameter impact on harmonic distortion," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4606–4613, Sep. 2021, doi: 10.1109/TED.2021.3096781.

[42] M. Rack, L. Nyssens, and J.-P. Raskin, "Low-loss Si-substrates enhanced using buried PN junctions for RF applications," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 690–693, May 2019, doi: 10.1109/LED.2019.2908259.

[43] M. Moulin *et al.*, "High performance silicon-based substrate using buried PN junctions towards RF applications," in *Proc. 7th Joint Int. EuroSOI Workshop Int. Conf. Ultimate Integr. Silicon (EuroSOI-ULIS)*, Caen, France, Sep. 2021, pp. 1–4, doi: 10.1109/EuroSOI-ULIS53016.2021.9560171.

[44] M. Rack, L. Nyssens, and J.-P. Raskin, "Silicon-substrate enhancement technique enabling high quality integrated RF passives," in *Proc. IEEE Int. Microw. Symp. (IMS)*, Boston, MA, USA, Jun. 2019, pp. 1295–1298, doi: 10.1109/MWSYM.2019.8701095.