Received 26 January 2022; revised 11 March 2022; accepted 31 March 2022. Date of publication 12 April 2022; date of current version 22 April 2022.
The review of this article was arranged by Editor P. Pavan.

Digital Object Identifier 10.1109/JEDS.2022.3166708

Performance Enhancement of Asymmetrical Double Gate Junctionless CMOS Inverter With 3-nm Critical Feature Size Using Charge Sheet

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ABSTRACT In this paper, after calibrating the models and parameters used in the simulations based on experimental data, by using the opposite doping in the channel and between the gates in an asymmetric double-gate junctionless (JL) transistor with the 3nm gate length, a charge sheet (CS) was created. The results showed that, due to creating CS in the middle of the channel, the horizontal electric field was increased, thus more major carriers were depleted from the middle of the channel. With the analysis of the I_{DS}-V_{GS} diagrams at different temperatures, it was concluded that in the CS JL MOSFET, while the ON-state current is very close to compared that in the JL MOSFET (same structure without CS), the drain leakage current has decreased by around 10^3. Furthermore, the I_{DS}-V_{DS} diagram showed that the drain current in the CS JL MOSFET was much less affected by the drain voltage compared to that in the JL MOSFET. Also in AC analysis and at 1MHz frequency, by using CS the parasitic capacitances were reduced. Due to the improvement obtained in the presence of the charge sheet, the proposed structure was used in designing an inverter. The results showed that in the presence of the charge sheet, logical high input range, and logical low input range were increased, and also, noise margin low (NM_L) and noise margin high (NM_H) were improved.

INDEX TERMS Junctionless transistor, MOSFET, CMOS, inverter, charge sheet, DC analysis, AC analysis.

I. INTRODUCTION

Considering that the industry seeks to miniaturization of CMOS transistors, research has increased on the design of transistors that reduce leakage current and have a significant switching speed in small dimensions [1]. The purpose of the fabrication of transistors with small dimensions is to be used in low-power digital circuits [2]–[3]. Therefore, two factors are very important in the design of a reliable transistor. The first factor is that the gate is capable of controlling the channel and drain current, and the second factor is that the transistor has a low drain leakage current in different temperature conditions [4]–[5]. On the other hand, with the downsizing of the physical gate length in the conventional transistors and due to the opposite doping of the channel with respect to the doping of the source and drain regions, the charge sharing and doping gradient phenomena occurred in the dimensions under 22 nodes, which led to a weakening of transistor performance [6]. In the recent decade, junctionless transistors have been introduced as a suitable alternative device to conventional transistors [7]–[8], and due to the easy fabrication process, better I_{ON}/I_{OFF} ratio, better frequency responses, and smallest parasitic capacitances have been highly regarded [9]–[10]. Initially, two features were considered for designing the structure of junctionless transistors. The first was that the source, drain, and channel regions were doped with the same type of doping, and the second was that the drain current flowed in the accumulation mode [11]–[13]. A lot of research has been done to improve these types of transistors. Choi *et al.* [14] examined the threshold voltage variation relative to channel width variation by constructing a junctionless transistor with 50nm gate length. Baruah and Paily [15] evaluated the Analog performance of junctionless transistor with 40nm gate using a High-k Spacer. Moon *et al.* [16] investigated

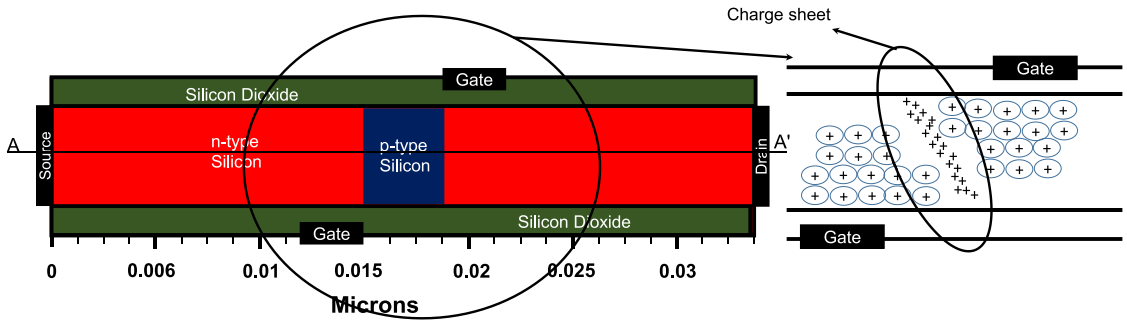

FIGURE 1. **The cross-section schematic view of an n-type asymmetrical double-gate junctionless MOSFET with a 3 nm physical gate length that uses reverse channel doping (p-type) to create the charge sheet.**

the performance of double gate junctionless transistor with 30 nm gate length on bulk in both doped and doping-less modes. Gundapaneni *et al.* [17] electrically increased the effective channel length in a junctionless transistor with 20 nm gate length in the off state by using a high k spacer. Barraud *et al.* [18] succeeded in fabricating transistors with a gate length of less than 13 nm. Studies on gate length reduction and channel length reduction on junctionless transistors continued until Migita *et al.* [19] and succeeded in designing and manufacturing a 3nm gate length.

The results showed that in a junctionless transistor with a scaled gate length (under 10 nm) when no voltage is applied to the gate, a drain current is established in the channel. The reason for this is that the electric field resulting from the difference between the gate work function and the semiconductor work function is not strong enough to deplete the majority of the carriers in the OFF state. In this paper, a novel structure based on the charge sheet (CS) was proposed for an asymmetrical double gate junctionless (JL) with a 3nm gate length. The results showed that in the proposed structure, the OFF-state current and the I_{ON}/I_{OFF} ratio have improved significantly. Studies also showed that CS JL performed much better in AC analysis rather than JL structure. Thus, using the proposed transistor, a NOT gate was designed, which significantly improved its performance.

II. SIMULATION METHODOLOGY AND RESULTS

Fig. 1 shows a cross-section schematic view of an n-type asymmetrical double-gate junctionless transistor with a 3nm physical gate length that uses reverse channel doping (p-type) to create the charge sheet. All simulations were carried out by numerical ATLAS Silvaco simulator [20]. Channel doping was considered 10^{19} (cm^{-3}) and also the channel thickness and gate oxide thickness were considered as 8 nm and 1 nm, respectively. Due to this amount of doping, the CCSMOB model was used to consider scattering effects and the CVT model was used to consider mobility degradation. Also, the FLDMOB model was used to consider the mobility dependence on the lateral electric field, and the SRH model was used to consider the recombination effects and lifetime of minority carriers. On the other hand, due to the very small dimensions of the transistor, the BQP model was used to consider quantum effects.

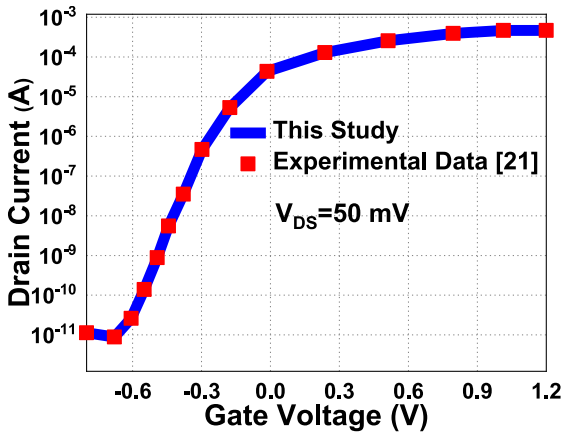

FIGURE 2. **Validation of the transfer characteristics curve obtained from simulation of JL structure with an experimental data in [21].**

As shown in Fig. 1, the electrons are depleted from the areas below the gate when the transistor is in the OFF state and only positive ions remain inside the channel. On the other hand, these positive ions cause the repels of the positive charges doped into the middle of the channel, which produces a sheet full of positive charges in the middle of the channel that these charges in this paper called charge sheet. Table 1 shows the essential parameters used in the simulations.

The models and parameters used in the simulations were calibrated by reproducing the experimental data in [21]. Fig. 2 confirms that models and appropriate parameters have been used.

A. DC ANALYSIS

Fig. 3(a) shows the log scale of the electrons and holes concentration in the OFF state along the AA' cutline. In this figure, as it is evident from the red line with circular symbols, in the JL structure without charge sheet, the electron concentration in the OFF state reaches 10^{16} (cm^{-3}), which means that the channel in the OFF state has a significant number of electrons and if an unintended voltage is applied

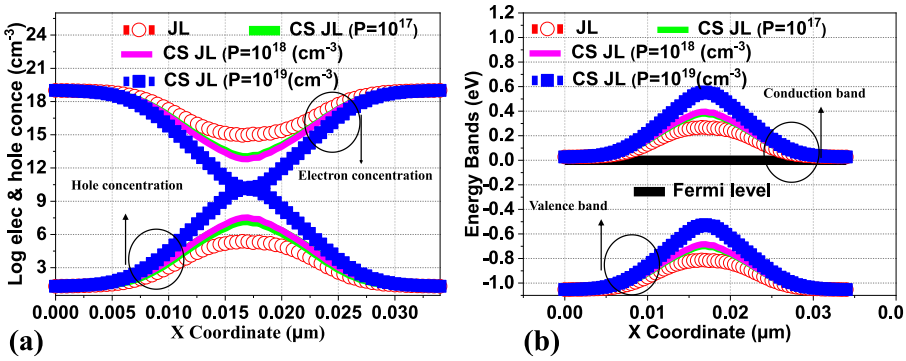

FIGURE 3. a) Log scale of electron and hole concentration for the JL and CS JL structures in the OFF state, and b) The equilibrium energy bands the JL and CS JL structures.

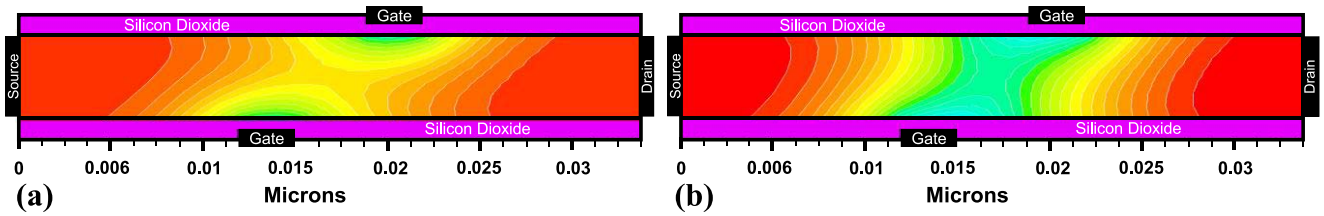

FIGURE 4. Graphical schematics cross section of the electron concentration in the OFF state for a) The JL structure, and b) The CS JL structure.

TABLE 1. Parameters used for the device simulation.

Parameters	Specifications
Electron affinity of silicon dioxide	0.9 (eV)
Electron affinity of silicon	4.18 (eV)
Energy band gap of silicon dioxide	8.99 (eV)
Energy band gap of silicon	1.07 (eV)
Relative permittivity of silicon dioxide	3.9 (eV)
Relative permittivity of silicon	11.9 (eV)
n-type doping concentration	10^{19} - 10^{18} - 10^{17} (cm^{-3})
p-type doping concentration	10^{19} - 10^{18} (cm^{-3})
Silicon dioxide thickness	1 (nm)
Silicon body thickness	8 (nm)
Gate work function	5.2 (eV)
gate length	3 (nm)

to the drain, regardless of the gate voltage, drain current is established in the channel and the transistor turns on. The blue line with square symbols shows the log scale diagram of the electrons and holes concentration for the CS JL structure. When CS was applied in the area between the two gates and inside the channel, it was observed that the concentration of electrons decreased to 10^{11} and the concentration of holes increased by 10^{12} (cm^{-3}). In this situation, the number of electrons depleted in the channel increases, and in the OFF state, the channel closes completely. Therefore, turning on the transistor and passing current is fully controlled by the gate.

The energy levels along the AA' cut line are shown in Fig. 3(b). According to the behavior of electrons and holes, it is observed that the conduction band in the CS JL structure is closer to the Fermi level than that in the JL structure. This means that the accumulation of holes in the OFF state in the middle of the channel and the proposed structure has increased. Fig. 4(a) and (b) show a graphical schematic cross-section of the electrons concentration for the JL structure and the CS JL structure, respectively. In these figures, it is clear that in the proposed structure and the OFF state, more electrons are depleted from the middle of the channel and the transistor is in the absolute OFF.

Fig. 5 shows the drain current versus gate voltage for different temperatures at 273K, 300K, 315K, and 350K for the JL structure and the CS JL structure in terms of drain voltages of 50mV, 100mV, 200mV, 300mV, 400mV, and 500mV. As shown in this figure, at all temperatures, and different voltages, the proposed structure has a much lower drain leakage current than that in the JL structure. On the other hand, it can be seen that the ON-state current in CS JL is very close to the JL current.

For a more accurate evaluation, the I_{OFF} and I_{ON}/I_{OFF} parameters were extracted from Fig. 5 and shown in Fig. 6, respectively. As shown in Fig. 6(a), the drain leakage current in the proposed structure has been improved by 10^3. Examining Fig. 6(b), it can also be seen that the I_{ON} /I_{OFF} ratio has increased in the CS JL structure by 10^3. Therefore, it can be concluded that the proposed structure has a very low drain leakage current and a very high switching speed.

The performance evaluation of the transistor is very important considering the curve of the output characteristic on a very small scale. Because in small dimensions, the dependence of the drain current on the drain voltage increases. Fig. 7 shows the output characteristic of the CS JL structure and the JL structure. Fig. 7(a) shows that by applying a voltage of 250 mV to the gate when the channel is slightly open, the drain current is almost zero until it is applied to the

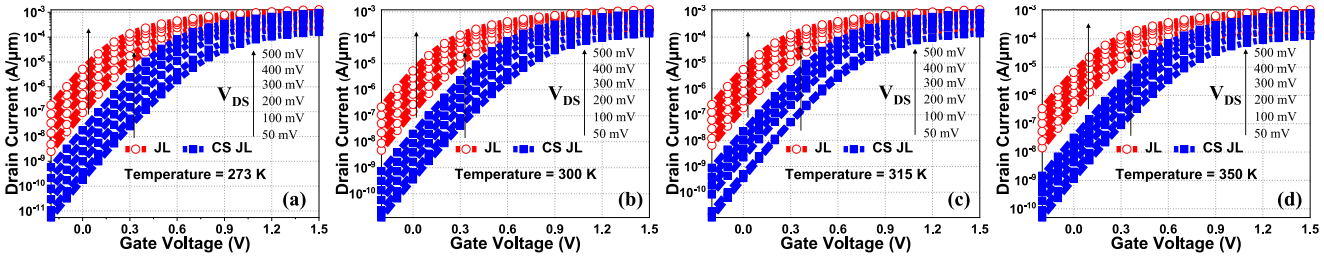

FIGURE 5. The drain current versus the gate voltage in terms of the drain voltages of 50mV, 100mV, 200mV, 300mV, 400mV, and 500mV for (a) the temperature at 273 K, (b) the temperature at 300 K, (c) the temperature at 315 K, and (d) the temperature at 350 K.

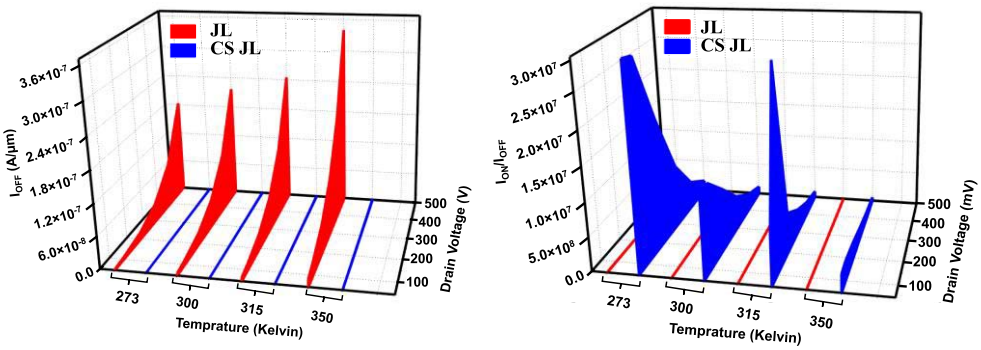

FIGURE 6. (a) Drain leakage current (OFF current) for JL and CS JL structures, and (b) I_{ON}/I_{OFF} ratio for JL and CS JL structures.

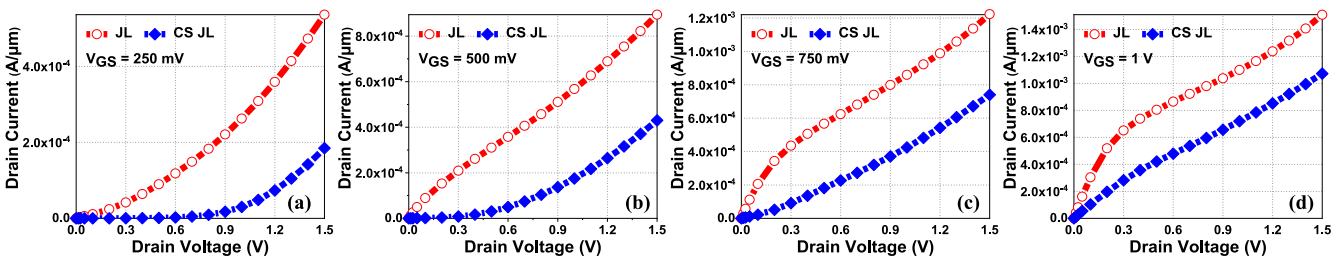

FIGURE 7. Drain current versus the drain voltage for, a) the gate voltages of 250 mV, (b) the gate voltages of 500 mV, (c) the gate voltages of 750 mV, and (d) the gate voltages of 1 V.

0.9V drain. On the other hand, it can be seen that when the channel is open and a voltage of 1 V and 1.5 V is applied to the gate, the amount of drain current is approximately 2% less than the current in the JL structure. Hence, it can be concluded that in the CS JL structure, if an inadvertent voltage is applied to the gate and the channel is in the half-depletion state, the drain current will be affected to a much lesser extent by the drain voltage.

B. AC ANALYSIS

Fig. 8(a) and (b) show the gate-drain capacitance and the gate-source capacitance in terms of gate voltage variation, respectively. In the obtained results and at a frequency of 1MHz, the gate-drain capacitance was 16 fF for the CS JL structure when the transistor was ON and 17.5 fF for the JL structure. Also in the same conditions, the gate-source capacitance was obtained for the CS JL structure of 15.5 fF and the JL structure of 16.5 fF.

According to equation (1), it can be concluded that the reduction of parasitic capacitances in the CS JL structure has increased the cut-off frequency.

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})} \tag{1}$$

$$f_{max} = \sqrt{\frac{f_T}{2\pi R_g C_{GD}}} \tag{2}$$

Moreover, according to equation (2), it can be concluded that maximum oscillation frequency (fmax) has improved.

III. CMOS INVERTER

An inverter can be made with an NMOS transistor or a PMOS transistor, but it is better to use both to reduce power consumption. Fig. 9 shows a schematic view of the CMOS inverter or NOT gate. In this study, two junctionless transistors, n-type and p-type, were designed based on the charge sheet and used in the inverter in Fig. 9. The channel doping

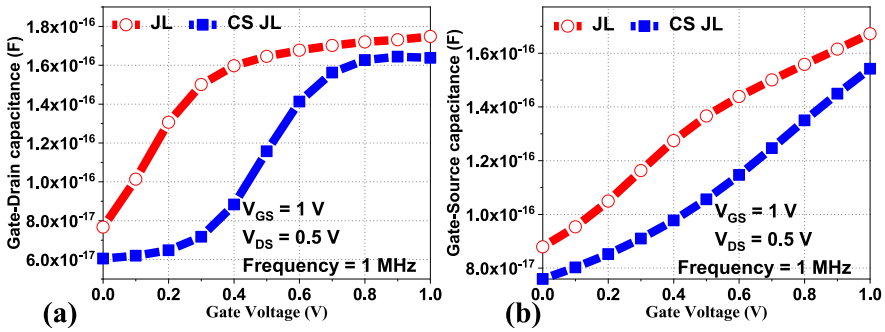

FIGURE 8. (a) Gate-Drain capacitance, and (b) Gate-Source capacitance, versus gate voltage for the CS JL structure compared to the JL structure.

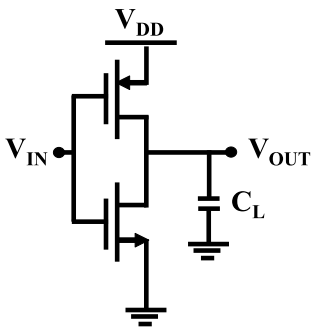

FIGURE 9. Schematic of the CMOS inverter circuit composed of n-type and p-type transistors.

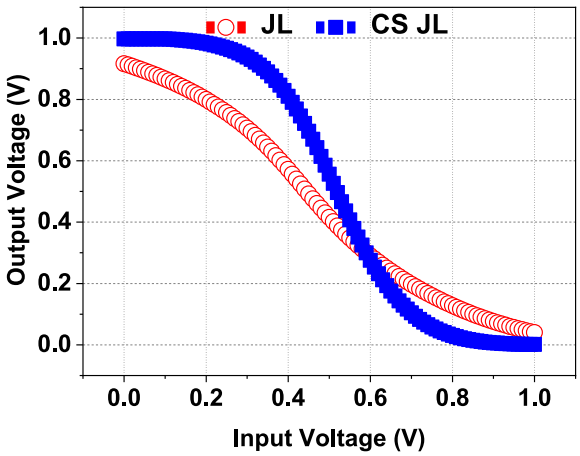

FIGURE 10. Voltage transfer characteristics for the JL CMOS inverter and CS JL CMOS inverter.

TABLE 2. Noise-margin measures.

Parameters	JL structure	CS JL structure
VOH min (V)	0.73764	0.92127
VOL max (V)	0.26947	0.09296
VIH min (V)	0.62	0.71
VIL max (V)	0.27	0.32
NMH (V)	0.11764	0.21127
NML (V)	0.00053	0.22704
VM (V)	0.47	0.52

and gate work function of the p-type transistor was considered 10^{18} (cm^{-3}) and 4.35 (eV), respectively. Opposite doping (10^{19} (cm^{-3}) n-type) was also used to create a charge sheet in this transistor. In the circuit shown in Fig. 9, V_{DD} is the drain voltage, V_{IN} is the input voltage, and C_L is the load capacitor. C_L was found in this circuit as the sum of $C_{GDn} + C_{GSn} + C_{GDp} + C_{GSp}$. Fig. 10 shows the voltage transfer characteristics (VTC) when applying 1V to V_{DD} and 1V to V_{IN}. As shown in this figure, when the charge sheet is not used (for the JL structure), the output voltage does not have a suitable switch due to the input voltage. Whereas, when the charge sheet is used, the output voltage has been able to be currently in the opposite position to the input voltage and change the level. According to Fig. 10 and Fig. 11, various data such as the high and low nominal voltages can be obtained, which are shown in Table 2.

As shown in Table 2, the minimum output voltage of the driving device for logic high ($V_{OH\,min}$) for the CS JL structure and the JL structure were obtained in order 0.92127 V and 0.73764 V, respectively. In the same conditions, the maximum output voltage of the driving device for logic low ($V_{OL\,max}$) for the CS JL structure and the JL structure were obtained in order 0.09296 V and 0.26947 V, respectively. Also, the switching threshold voltage for the JL and CS JL structures were obtained in order 0.47 V and 0.52 V, respectively. On the other hand, for CS JL and JL structures, the minimum input high voltage of a logic gate ($V_{IH\,min}$) was obtained 0.71 V and 0.62 V, and the maximum input low voltage ($V_{IL\,max}$) was obtained 0.32 V and 0.27 V, respectively.

Fig. 11 shows the graphically authorized and unauthorized voltages for the CS JL and JL structures to obtain the 0 and 1 logics.

Based on Fig. 11, noise margin low (NM_L) and noise margin high (NM_H) can be specified. According to this figure, NM_L and NM_H are obtained from the following equations.

$$NM_H = V_{OH} - V_{IH} \tag{3}$$

$$NM_L = V_{IL} - V_{OL} \tag{4}$$

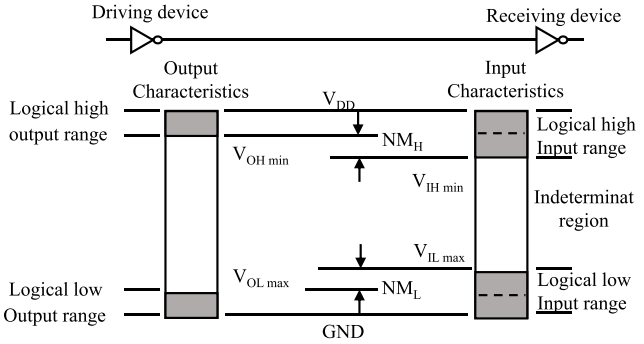

FIGURE 11. Block diagram of Noise margin.

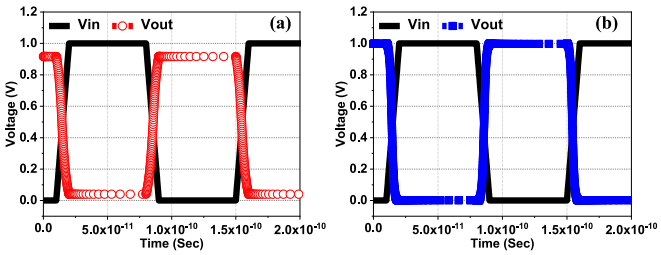

FIGURE 12. Transient analysis of inverter circuit for (a) JL CMOS inverter (b) CS JL CMOS inverter.

TABLE 3. Propagation delays.

Parameters	JL structure	CS JL structure
tPHL (ps)	3.41E-13	8.33E-13
tPLH (ps)	4.61E-13	9.28E-13
tP	4.01E-13	8.81E-13

According to equations (3) and (4), NM_H was obtained for the CS JL and JL structures, 0.21127 and 0.11764, and NM_L were obtained 0.22704 and 0.00053 respectively.

According to these results, it is obvious that in the CS JL structure, higher input voltage amplitude can be applied so that the output voltage does not collapse.

Fig. 12 illustrates the transient response for JL and CS JL structures. As shown in this figure, in the inverter with JL structure, the level of output voltage amplitude is less than the input voltage amplitude. This is because, when applying the negative voltage to the gate, there is no positive charge in the channel to respond to these negative charges, while in the inverter with CS JL structure, the amplitude of the output voltage is equal to the amplitude of the input voltage.

Table 3 shows the propagation delays. Considering that in the JL structure the output voltage amplitude cannot accurately follow the amplitude of the input voltage, it is observed that due to the smaller amplitude in this structure High-to-Low propagation delay (t_{PHL}) and Low-to-High propagation delay (t_{PHL}) are lower than that in the CS JL structure. On the other hand, considering that in the CS JL structure the output voltage amplitude correctly follows the input voltage amplitude, it can be seen that t_{PHL} and t_{PHL} in this structure have very little difference with t_{PHL} and t_{PHL} in the JL structure.

Average propagation delays are obtained from the following equation.

$$t_P = \frac{t_{PHL} + t_{PLH}}{2}. \tag{5}$$

IV. CONCLUSION

In this paper, an asymmetrical double gate junctionless with a gate length of 3nm was investigated and evaluated in the presence of a charge sheet (CS). The DC analysis showed that when CS was used, the leakage current was reduced by 10^3 at temperatures of 273K, 300K, 315K, and 350K compared to the structure without CS. the results also showed that in the same conditions and at the above-mentioned temperatures, the I_{ON}/I_{OFF} ratio in the CS structure has increased compared to the JL structure. On the other hand, in AC analysis, it was found that parasitic capacitances have been improved in the proposed structure at a frequency of 1MHz. The results of behavioral analysis of the inverter showed that the minimum output voltage of the driving device for high logic, the maximum output voltage of the driving device for low logic, switching threshold voltage, the minimum high voltage input of a logic gate, the maximum input Low voltage has improved in the presence of CS. Also, by calculating noise margin low (NM_L) and noise margin high (NM_H), it was found that the proposed structure has better logical high input and logical low input ranges.

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