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Four-Terminal Ferroelectric Schottky Barrier Field Effect Transistors as Artificial Synapses for Neuromorphic Applications

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ABSTRACT In this paper, artificial synapses based on four terminal ferroelectric Schottky barrier field effect transistors (FE-SBFETs) are experimentally demonstrated. The ferroelectric polarization switching dynamics gradually modulate the Schottky barriers, thus programming the device conductance by applying negative or postive pulses to imitate the excitation and inhibition behaviors of the biological synapse. The excitatory post-synaptic current can be modulated by the back-gate bias, enabling the reconfiguration of the weight profile with high speed of 20 ns and low energy (< 1 fJ/spike) consumption. Besides, the tunable long term potentiation and depression show high endurance and very small cycle-to-cycle variations. Based on the good linearity, high symmetricity and large dynamic range of the synaptic weight updates, a high recognition accuracy (92.6%) is achieved for handwritten digits by multilayer perceptron artificial neural networks. These findings demonstrate FE-SBFET has high potential as an ideal synaptic component for the future intelligent neuromorphic network.

INDEX TERMS Ferroelectric polarization, FE-SBFET, HZO, neuromorphic, artificial synapse.

I. INTRODUCTION

Artificial neuromorphic system (ANS) has emerged as an alluring technology in the post-Moore era due to its high efficiency ability to complete cognitive tasks [1], [2]. An ANS using conventional CMOS technology requires numerous transistors to implement basic neuron functions, thus causing high cost and extra high power consumptions [3]–[5]. Non-volatile memories (NVM), like resistive random access memory (ReRAM) [6] and phase change memory (PCM) [7] based devices are very interesting candidates for neuron devices. However, the high variability, poor stability and high operation voltage are challenges for these devices [8], [9].

HfO_2 based ferroelectric materials have attracted a lot of attention due to their CMOS compatibility and scalability [4], [10]. Ferroelectric FETs (FeFETs) which use HfO_2 based ferroelectric layer as the gate oxide show very promising neuron functions with high performance, and low power consumption [11], [12]. Compared with traditional FeFETs, the metal source/drain Schottky barrier (SB) MOSFET (SBFET) structure is very attractive to maintain the HfO_2 based ferroelectric properties due to its relatively low temperature processing which requires neither ion implantation nor thermal activation of source/drain contacts at high temperatures [13]–[17].

In our previous work [18], we reported a 3-terminal synapse based on ferroelectric SBFETs (FE-SBFETs), where homo-synaptic plasticity of artificial synapses was demonstrated. In this work, a 4-terminal synapse based on the FE-SBFET with a back gate is presented [19]. Emphasis is put on the impact of the back gate which acts as a modulatory neuron to tune the synapse functionalities generated by the top gate. Thus hetero-synaptic plasticity of the

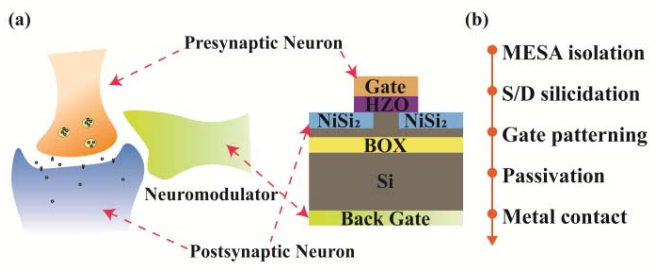

FIGURE 1. (a) Schematic showing a 4-terminal FE-SBFET synapse, where the top gate and drain are used as the pre- and post- synaptic terminals. The back gate is the neuromodulator. (b) Key fabrication process flow for the FE-SBFET.

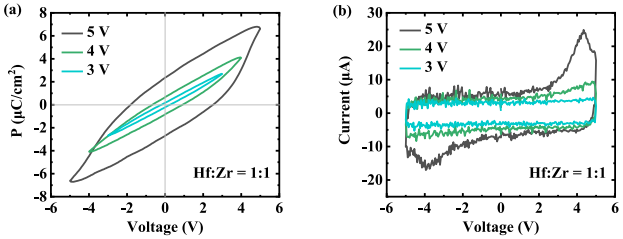

FIGURE 2. (a) P-V characteristics of a 10 nm thick HZO layer measured with a TiN/HZO/$NiSi_2$ MFM capacitor. (b) Corresponding transient currents for this MFM capacitor.

synapse can be achieved. The SB at source/drain and the channel potential are modulated by the ferroelectric polarization and the back gate, thus changing the carrier injection through the SB and the channel conductance of the device. The fabricated FE-SBFETs employing uniform single crystalline $NiSi_2$ SB contacts on silicon on insulator (SOI) and ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film exhibit tunable excitatory post-synaptic current (EPSC) with high switching speed and low power consumption, paired-pulse facilitation (PPF), high symmetric conductance for long term potentiation and depression characteristics (LTP/LTD). Due to the good linearity, high symmetricity and ON/OFF ratio, a high pattern recognition accuracy of 92.6% is achieved based on the simulation of a 3-layer multilayer perceptron (MLP) artificial neural network.

II. DEVICE FABRICATION

The device structure is schematically shown in Fig. 1(a), where the top gate and drain are used as the pre- and post-synaptic terminals while the back gate acts as a neuromodulator. The synapse utilizes ferroelectric partial polarization switching dynamics in thin HZO films while the neuromodulator bias gradually modulates the SB of the $NiSi_2$ to Si contacts and the channel conductance. The partial polarization switching of the ferroelectric by a negative voltage pulse on the top gate induces additional holes at $NiSi_2$/Si interface, causing SB thinning at the valence band. An increase of the number of pulses will strength the domain polarization, resulting in thinner SB and consequently more holes are injected through the SB. Therefore, gate voltage pulses can gradually program the conductance of the device. The neuromodulator bias is used to modulate the carrier density in the Si channel, realizing hetero-synaptic plasticity which can solve the positive feed-back loop problem in conventional homo-synapses [20], [21].

Devices were fabricated on an SOI substrate with a boron-doped ($\sim 10^{16}$ B/cm^{-3}) 55nm thick top Si layer and a 145 nm thick buried SiO_2 layer (BOX). As shown in Fig. 1(b), after mesa definition single crystalline $NiSi_2$ layers were formed at source/drain regions using conventional self-aligned silicidation process at 800°C in forming gas atmosphere with a 3 nm Ni thin film [22]. After removal of the excess Ni, a 10 nm thick HZO layer and a 40 nm thick TiN layer were deposited by ALD and sputtering, respectively, forming the gate stack. Tetrakis (ethylmethylamino) hafnium (TEMAHf), tetrakis (ethylmethylamino) zirconium (TEMAZr) are employed as precursors and water vapor as co-reactant for ALD deposition of HZO layers at 300°C. Then a rapid thermal annealing at 500°C in N_2 was performed to crystallize the HZO into the ferroelectric phase. The gate was defined by optical lithography and reactive ion etching. Meanwhile, metal-ferroelectric-metal (MFM) ferroelectric capacitors with TiN/HZO/$NiSi_2$ stack were also fabricated to characterize the ferroelectric properties of the HZO layer. The top gate of the device has 6 μm overlaps with the source/drain $NiSi_2$ contacts which provides larger SB contact area modulated by the ferroelectric polarization. As we showed in our previous paper [18] interfacial SiO_2 layers with a thickness of 1.7 nm were formed between the $NiSi_2$ and HZO, as well as between the Si channel and HZO layer. The fabricated device has a channel length of 10 μm between the two $NiSi_2$ layers. After deposition of a PECVD SiO_2 layer for passivation device contacts were metallized with Al after via opening. Finally, an Al layer was deposited on the back side of the substrate to be used as the back gate.

III. RESULTS AND DISCUSSION

A. I-V CHARACTERISTICS OF FE-SBFETS

The ferroelectricity of HZO is characterized using a TiN/10 nm HZO/$NiSi_2$ MFM capacitor. Fig. 2(a) and (b) show the typical polarization–voltage (P-V) ferroelectric hysteresis loops and corresponding transient currents of the MFM capacitor, respectively. The remanent polarization gradually increases by increasing the applied voltage, which means the polarization of the HZO ferroelectric layer can be effectively exploited by controlling the applied voltage. The polarization of the HZO layer depends strongly on the orthorhombic phases in the layer, which can be enhanced by the stress presented in the TiN layer during annealing [23]. As discussed in our previous paper [18], the stress-free $NiSi_2$ bottom electrode shows less reinforcement to form the orthorhombic phase in the HZO layer, thus causing weaker polarization in the TiN/HZO/$NiSi_2$ capacitor. This can be further enhanced by optimization of the top TiN layer thickness and annealing process.

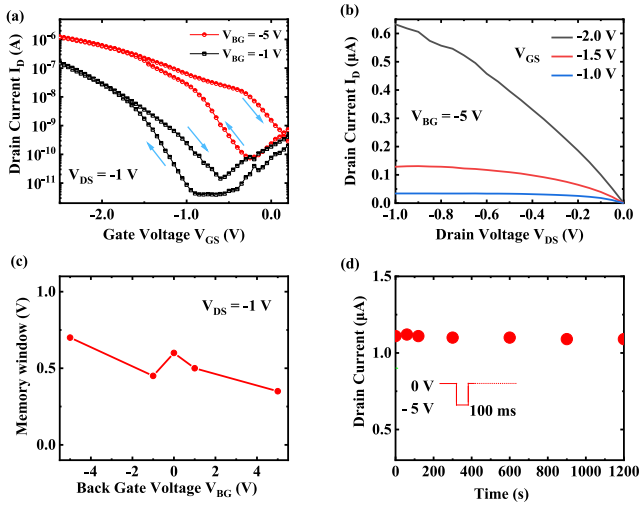

FIGURE 3. **(a) I_D-V_{GS} transfer characteristics at $V_{BG} = -5$ V, -1 V and $V_{DS} = -1$ V for an FE-SBFET, showing a clockwise hysteresis for p-FET and ambipolar switching behavior. (b) I_D-V_{DS} output curves of the corresponding device with varying V_{GS} from -1.0 to -2.0 V. (c) Memory window of the corresponding device with varying V_{BG} from -5 to 5 V. (d) Retention time by measuring the drain current at $V_{DS} = -1$ V of a FE-SBFET device after a gate pulse with an amplitude of -5 V with 100 ms pulse width, showing a long retention time.**

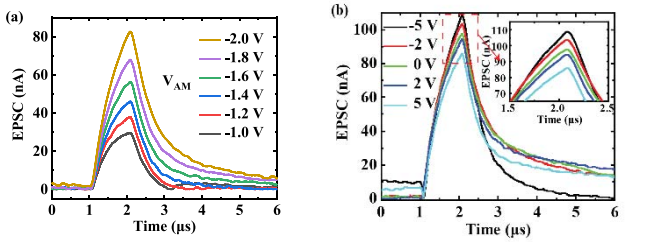

FIGURE 4. **(a) EPSC generated by the gate spike with an identical duration time (1 μs) and various potentiating amplitudes V_{AM} ranging from -1 to -2 V measured at $V_{DS} = -0.15$ V and $V_{BG} = -5$ V. (b) Dependence of EPSC on the neuromodulator voltage V_{BG}, showing synaptic modulations. The inset in Fig. 4(b) is the zoom of the EPSC peaks, showing clearly the modulation of V_{BG}.**

The drain current (I_D) versus gate voltage (V_{GS}) transfer characteristics of a 4-terminal FE-SBFET are presented in Fig. 3(a) with dual sweeping of V_{GS} in forward and reverse directions at a drain voltage $V_{DS} = -1$ V and a back gate voltages $V_{BG} = -1.0$ and -5.0 V, respectively, showing a clearly clockwise hysteresis for the p-FET branch and the typical SB-MOSFET ambipolar behavior. Because of the p-type SOI layer and the higher Schottky barrier of $NiSi_2$ to electrons the n-FET branch shows a much higher threshold voltage and lower currents. Therefore, in this paper we mainly focus on the p-FET branch. However, the ambipolarity could contribute high off-currents. The ambipolarity could be suppressed by moderate doping of the SOI layer or using fully depleted (FD) SOI with ultra-thin body and BOX, where the improved electrostatic control can make the barrier thinner, and thus the onset voltage between p- and n-FET branch is larger. Comparison the I_D-V_{GS} characteristics at $V_{BG} = -1.0$ V and -5.0 V indicates that a higher negative V_{BG} increases both I_D and the memory window due to more electrostatic charges (here holes) introduced by higher negative back gate. The device shows an ON/OFF current ratio of 1×10^4 and a memory window of 0.7 V at $V_{BG} = -5$ V. The output characteristics I_{DS}-V_{DS} for the corresponding FE-SBFET are shown in Fig. 3(b) with V_{GS} sweeping from -1.0 to -2.0 V. Compared to the results shown in [18] without back gate, a $V_{BG} = -5$ V suppresses the super-linear behavior in the I_D-V_{DS} characteristics because more electrostatic charges are created by the back-gate and thus reduces the effective SB at source/drain. As shown in Fig. 3(c), the memory window of the FE-SBFET slightly decreases with increasing V_{BG} from -5 to 5 V. Fig. 3(d) shows the retention behavior by measuring the drain current of the FE-SBFET device at $V_{DS} = 1$ V after applying a gate pulse of -5 V/100 ms, demonstrating a long retention time. The FE-SBFETs presented in this paper benefits from much easier process to avoid high thermal budget which could degrade the ferroelectric layer and the ferroelectric/Si channel interface. One of the drawbacks of our device compared with the FDSOI FeFET as reported in [24] is the lower ON/OFF current ratio and the smaller memory window due to the ambipolar switching and the weaker controllability of both the top and back gates. FE-SBFETs on FDSOI substrates are under processing.

B. SYNAPSE CHARACTERISTICS

To exploit synaptic functionalities, the top gate and drain terminals act as connections of the pre- and post- synaptic neurons, respectively. The back gate is used as the neuromodulator. Postsynaptic currents triggered by presynaptic spikes from the top gate terminal correspond to EPSC, which can measure the synaptic strength. The EPSC response of an FE-SBFET based synapse is characterized by measuring the transient drain currents at a fixed $V_{DS} = -0.15$ V, $V_{BG} = -5$ V for a voltage pulse stimulus on the top gate as shown in Fig. 4(a), which is generated by a single presynaptic spike with different pulse amplitudes V_{AM} ranging from -1.0 to -2.0 V and a pulse width = 1 μs. The back-gate tunable channel carrier density resembles the information transmission in biological synapses. By applying an external stimulus of back gate voltage, the synapse weight is tuned by modulating the connection strength between neurons (the hole density in the device), in other words, the synaptic plasticity. The dependence of EPSC on the neuromodulator voltage V_{BG} is depicted in Fig. 4(b) with V_{BG} varying from -5 to 5 V, showing synaptic weight modulation abilities.

Fig. 5(a) displays the EPSC response recorded at $V_{DS} = -0.15$ V to a gate input spike ($V_{AM} = -2$ V) with various pulse time ranging from 20 ns to 1 μs. A very clear EPSC with large enough signal/noise ratio is achieved even for the 20 ns pulse, demonstrating high speed of the device. The EPSC peak value increases with the increasing spiking pulse width t_{pw} (Fig. 5b). The energy/spike consumption shown

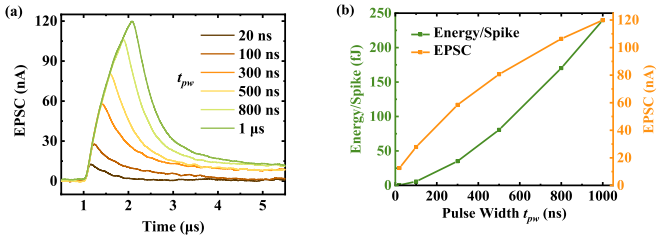

FIGURE 5. **(a) EPSC generated by a gate pulse with an identical amplitude (−2 V) at V_{BG} = −5 V and different pulse width t_{pw} ranging from 20 ns to 1 μs, showing a high switching speed. (b) The EPSC peak value increases with the pulse width. The calculated energy/spike consumption shows a very low value of < 1 fJ at V_{AM} = −2 V, V_{DS} = −0.15 V, V_{BG} = −5 V and pulse duration time 20 ns.**

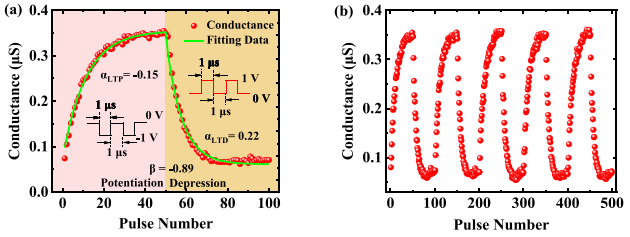

FIGURE 7. **Emulation of biological synaptic behaviors and repetitive channel conductance modulation. (a) Measured synapse conductance at V_{DS} = −0.15 V and V_{BG} = −5 V as a function of identical pulse numbers, showing potentiation and depression characteristics. (b) Exemplary 5 cycles of potentiation and depression after 10k repeated pulse measurements show very small CTC variations.**

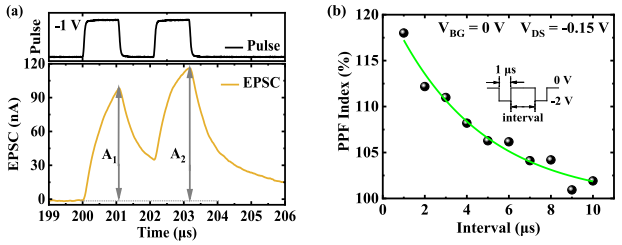

FIGURE 6. **(a) EPSC responses triggered by a pair of input pulses (−1 V, 1 μs) with a time interval of 1 μs at V_{AM} = −1 V, V_{DS} = −0.15 V and V_{BG} = 0 V. A_1 and A_2 represent the EPSC generated by the first and second presynaptic spike pulses, respectively. PPF index is calculated from A_1 and A_2. (b) PPF characteristics for an FE-SBFET synapse by measuring the synaptic strength change as a function of the pulse interval, showing a biological synapse behavior with a single exponential decay.**

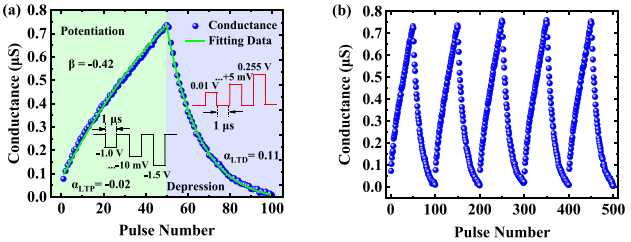

FIGURE 8. **(a) The synapse conductance measured at V_{DS} = −0.15 V with non-identical (increasing amplitude, as shown in the insets) pulses, indicate an improved linearity and better potentiation/depression symmetry compared to the results presented in Fig. 6(a). (b) Similar to Fig. 6 (b), the exemplary 5 cycles of potentiation/depression with non-identical pulses after 10k repeated measurements show also a very small CTC variations (~1%).**

in Fig. 5b is calculated with:

$$E = V_{AM} \times EPSC \times t_{pw}. \tag{1}$$

A low energy consumption of < 1 fJ/spike is obtained at pulse width t_{pw} = 20 ns, demonstrating further high energy efficiency and high speed compared to the state of the art technologies [25].

To examine the short-term synaptic plasticity, PPF was investigated, which is essential to decode the temporary information in a biological system used to measure the synaptic strength change. The PPF index is defined as:

$$PPF\ index = A_2/A_1 \times 100\%. \tag{2}$$

where A_1 and A_2 correspond to the EPSC amplitude generated by the first and second of two neighboring pre-synaptic spikes. Fig. 6(a) shows the PPF characteristics when two successive input pulses (−1 V, 1 μs) were introduced with an interval time of 1 μs, as presented in Fig. 6a. The PPF index is plotted in Fig. 6(b) as a function of the pulse interval from 1 to 10 μs, showing a biological synapse behavior with a single exponential decay by fitting PPF with the following equation:

$$PPF\ index = C_0 + C_1 \times e^{-t/\tau 0}. \tag{3}$$

where C_0 is the background, t the pulse interval time, C_1 (0.22) the initial facilitation magnitude, and τ_0 is the decay time constant (4.25 μs). The PPF index decreases from 118% to 101.9% with increasing the interval time between two presynaptic spikes from 1 to 10 μs.

The continuous and repetitive channel conductance modulation of the aforementioned synaptic transistor with a series pulse is exhibited in Fig. 7, showing the long-term synaptic plasticity. Long-term potentiation and depression (LTP/LTD) characteristics are clearly demonstrated in Fig. 7(a) by plotting the measured conductance of an FE-SBFET synapse as a function of pulse numbers for pulse waveforms with 1 μs width, 1 μs interval and ± 1 V amplitude, where the nonlinearity α_P = −0.15, α_D = 0.22 and asymmetry β = −0.89 are extracted according to [26] by fitting the experimental data with 50 programming states, and the ON/OFF ratio = 6. Fig. 7(b) depicts exemplarily 5 cycles of potentiation/depression after 10k pulse measurements, showing a small cycle-to-cycle (CTC) variation (1%) and a high endurance. Likewise, the measured FE-SBFET synapse channel conductance as a function of non-identical (increasing amplitude) pulse numbers is displayed in Fig. 8(a), showing better linearity and symmetry, where the nonlinearity α_P = −0.02, α_D = 0.11 and asymmetry β = −0.42. It also shows a very high ON/OFF ratio = 97, an extremely small CTC variation and a high endurance (Fig. 8(b)). The corresponding scheme of the applied synaptic spikes is illustrated in the insets of Fig. 7(a) and Fig. 8(a), respectively.

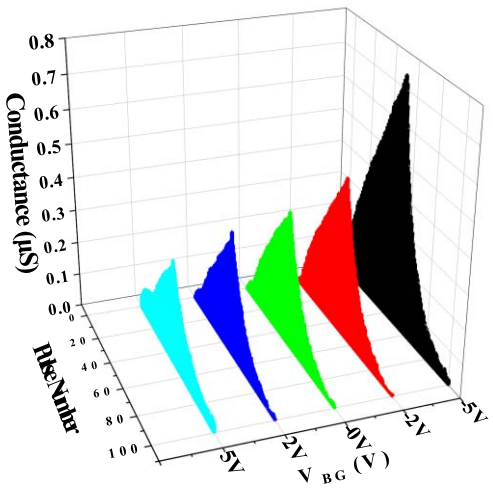

FIGURE 9. Plots of channel conductance as a function of the number of input spikes at various V_{BG} values, showing the modulation of the synaptic weight by V_{BG}.

Fig. 9 presents the device conductance as a function of the number of input spikes at various V_{BG} values, which indicates the synaptic plasticity including LTP and LTD, is further accelerated by applying a negative V_{BG}, corresponding to the consolidation of long-term memory. When V_{BG} changes from -5 to 5 V, the nonlinearity increases from -0.02 / 0.11 to -0.15 / 0.12 and the ON/OFF ratio decreases from 97 to 16. This behavior originates from the effective back-gate electric field across the SOI layer, increasing the holes density in the Si layer meanwhile the conductance of the channel region will also increase and thus a higher dynamic range of the EPSC. So using electrostatic charges, the intrinsic type of synaptic plasticity can be modified easily. We have to mention that the single common back-gate under Si substrate cannot control the device individually. This is the drawback of the back-gate. One of the possible solutions is to employ the shallow trench isolation (STI) technology to isolate device from each other and contact the substrate close to the device from the top.

C. PATTERN RECOGNITION SIMULATION

To explore the further application of Fe-SBFET synapse in pattern recognition, a 3-layer multilayer perceptron (MLP) neural network was designed based on the experiment results of the potentiation and depression to perform supervised learning on the Modified National Institute of Standard and Technology (MNIST) database [27]. As shown in Fig. 10(a), due to dramatic improvement in linearity and asymmetry, the recognition accuracy acquired with non-identical pulses are much higher than the identical pulses at $V_{BG} = -5$ V. For example, the recognition accuracy after 20 epochs corresponds to 61.3% and 90.0% for identical and non-identical pulses, respectively. Furthermore, recognition accuracy of simulation is also controlled by the neuromodulator voltage V_{BG}. The highest learning accuracy of 92.6% is achieved at

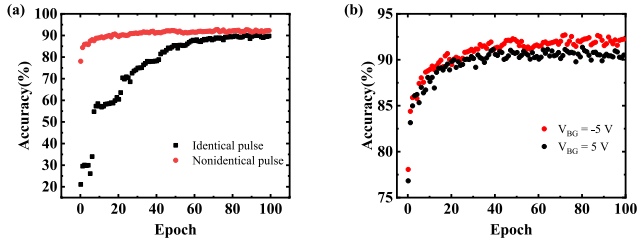

FIGURE 10. Pattern recognition simulation. (a) Recognition accuracy acquired with the identical and non-identical pulses at $V_{BG} = -5$ V. (b) Recognition accuracy of simulation with different V_{BG}. A high learning accuracy of 92.6% is achieved at $V_{BG} = -5$ V with non-identical pulses.

$V_{BG} = -5$ V with non-identical pulses in Fig. 10(b). The network has a training set of 60k images and a testing set of 10k images.

IV. CONCLUSION

We have demonstrated a four terminal ferroelectric Schottky barrier field effect transistors with single crystalline $NiSi_2$ contacts and HZO ferroelectric to mimic synapse properties. The fabricated synapse exhibits synaptic functions tuned by the back-gate bias, including excitatory post-synaptic current and paired-pulse facilitation with high speed (20 ns) and low energy consumption ($<$ 1 fJ/spike). Furthermore, tunable long term potentiation and depression with high endurance, low cycle-to-cycle variations and high endurance have been achieved with lower voltage pulses and small currents. Finally, the artificial neuron network simulation built from FE-SBFET synapse achieves 92.6% recognition accuracy of handwriting digit, which shows a high potential on the implementation of the future intelligent neuromorphic systems.

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