Received 3 March 2022; revised 26 March 2022; accepted 26 March 2022. Date of publication 30 March 2022; date of current version 8 April 2022.
The review of this article was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2022.3163251

Temperature-Dependent Narrow Width Effects of 28-nm CMOS Transistors for Cold Electronics

TING TSAI, HORNG-CHIH LIN (Senior Member, IEEE), AND PEI-WEN LI (Senior Member, IEEE)

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan

CORRESPONDING AUTHOR: P.-W. LI (e-mail: pwli@nycu.edu.tw)

This work was supported by the Ministry of Science and Technology, Taiwan, under Grant 108-2221-E-009-007-MY3 and Grant 109-2221-E-009-022-MY3.

ABSTRACT We reported temperature-dependent narrow width effects on electrical characteristics of 28-nm CMOS transistors measured at temperature of 77 K−300 K. At cryogenic temperatures, P-MOSFETs appear to have stronger temperature-induced threshold voltage (V_{th}) increase and subthreshold swing (SS) reduction than N-MOSFETs, whereas the improvement in drain-induced barrier lowering (DIBL) is more evident in N-MOSFETs. N-MOSFETs show typical reverse narrow effect (RNWEs) in terms of V_{th} roll-off along with SS rise-up with narrowing channel-widths (W_G). In contrast, P-MOSFETs exhibit anomalous RNWE, that is, V_{th} (SS) decreases (increases) with decreasing W_G from 3 μm to 0.6 μm and reversely increases (decreases) with further narrowing to 0.3 μm. RNWEs on N-MOSFETs are clearly suppressed at cryogenic temperatures, whereas P-MOSFETs appear to have enhanced anomalous RNWEs in terms of V_{th} and DIBL variations at 77 K.

INDEX TERMS Cryogenic CMOS, reverse narrow width effect.

I. INTRODUCTION

Cryogenic complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) have attracted extensive attentions for their great promises not only for control and readout circuitry in quantum computing [1]–[6], but also for spacecraft [7], [8], data centers, precision detection [9], memory [10], [11], and high-performance computing (HPC) [12]. This is because the performance of MOSFETs at cryogenic temperatures gains improvements in terms of on-state current (I_{ON}) at constant gate-overdrive, mobility, transconductance (g_m), subthreshold swing (SS), off-state current (I_{OFF}), power dissipation, thermal noise, thermal-assisted leakage, and thermal fluctuations, etc. In particular, HPC has been estimated to have the best performance/power factor improvement at $T = 77$ K -100 K by $>$ 5-fold as compared to room-temperature operation [12], [13]. However, V_{th} increase [14], [15] and unusual electrical characteristics such as current hump [16] may impact the operation of CMOS circuits at deep cryogenic temperatures.

For cryo-CMOS circuitry design, not only temperature-induced variations in key parameters of V_{th}, SS, and V_{th} shift due to drain-induced barrier lowering (DIBL) for transistors with given channel-lengths (L_G) and widths (W_G), but also the deviations in temperature dependency of short-channel effects (SCEs) and narrow-width effects (NWEs) are critical. This is because transistors with different L_G and W_G would be considered in analog ICs, since the performance of analog ICs may not be directly benefit from the smallest feature sizes as much as of digital ICs. Therefore, the discrepancy in temperature-induced V_{th} increase, SS reduction, DIBL variation, and NWEs between N-MOSFETs and P-MOSFETs possibly give rise to additional design concerns for cryo-CMOS circuitry.

Several reports have investigated cryogenic characteristics and modeling of bulk MOSFETs, [14]–[22] FinFETs, [12]–[23], and fully-depleted silicon-on-insulator (SOI) FETs [23]–[27] with L_G ranging from 0.35 μm to 14 nm. However, NWEs on advanced CMOSFETs operating at cryogenic temperatures remain to be addressed. In this paper, we report temperature-dependent electrical characteristics of N-MOSFETs and P-MOSFETs with W_G of 0.3 μm − 3 μm fabricated using a commercial 28-nm bulk CMOS foundry service. Transistors were

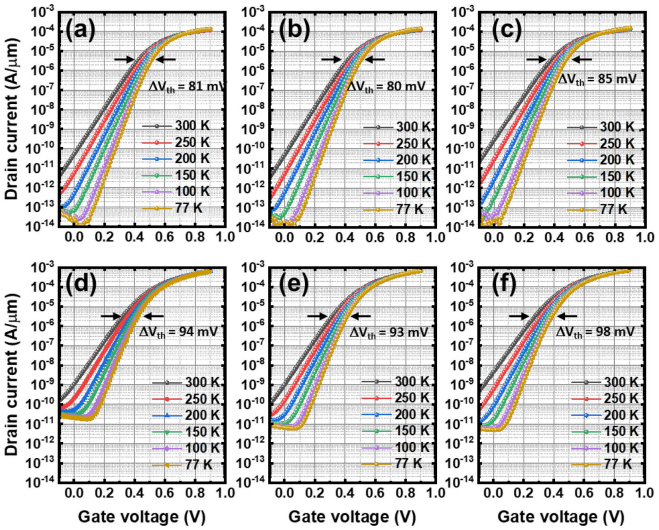

FIGURE 1. Transfer characteristics of N-MOSFETs with W_G/L_G of (a)/(d) 3 μm/28 nm, (b)/(e) 0.6 μm/28 nm, and (c)/(f) 0.3 μm/28 nm measured at $V_D = +0.05$ V/+0.9 V, respectively.

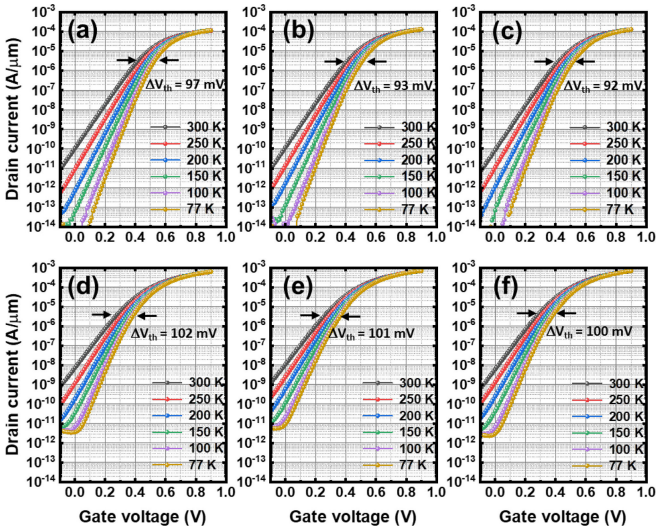

FIGURE 2. Transfer characteristics of P-MOSFETs with W_G/L_G of (a)/(d) 3 μm/28 nm, (b)/(e) 0.6 μm/28 nm, and (c)/(f) 0.3 μm/28 nm measured at $V_D = -0.05$ V/−0.9 V, respectively.

measured at $T = 77$ K − 300 K. Key parameters were extracted from experimentally-measured current-voltage (I-V) characteristics and numerically fitted for accurate modeling.

II. ELECTRICAL MEASUREMENTS

Electrical measurements were conducted in a Lakeshore CPX-VF liquid-nitrogen cooled vacuum-sealed probe station using a semiconductor device analyzer Agilent B1500A equipped with B1517A high-resolution source monitor unit/atto sense and switch unit, improving the measurement resolution to femtoampere range. Transfer characteristics were measured in saturation ($|V_D| = 0.9$ V) and linear ($|V_D| = 0.05$ V) regimes, respectively. Parameters of V_{th} (V_G at which the maximum transconductance ($g_{m,max}$) occurs), SS ($\equiv \partial(\log I_D)/\partial V_G)^{-1}$), DIBL ($\equiv$ (V_{th} ($|V_D| = 0.9$ V) − V_{th} ($|V_D| = 0.05$ V))/ΔV_D), I_{ON} (I_D at $|V_G = 0.9$ V), and I_{OFF} (I_D at $V_G = 0$ V) were extracted from transfer characteristics.

III. RESULTS AND DISCUSSION

A. TEMPERATURE EFFECT

Figs. 1 and 2 show transfer characteristics of N-MOSFETs and P-MOSFETs, respectively, measured at temperature ranging from 77 K to 300 K. It is clearly seen that lowering temperature leads to a systematic increase in V_{th} (Fig. 3) along with a reduction in SS for both N-MOSFETs and P-MOSFETs operating at linear and saturation regimes.

Parameters of V_{th} and SS for P-MOSFETs appear to be more susceptible to operating temperatures than their counterpart N-MOSFETs. Figure 3 show that decreasing temperature from 300 K to 77 K, V_{th}-shift (V_{th} ($T = 77$ K) − V_{th} ($T = 300$ K)) values of 97 mV and 102 mV for 3 μm-wide P-MOSFETs are greater than that of 81 mV and

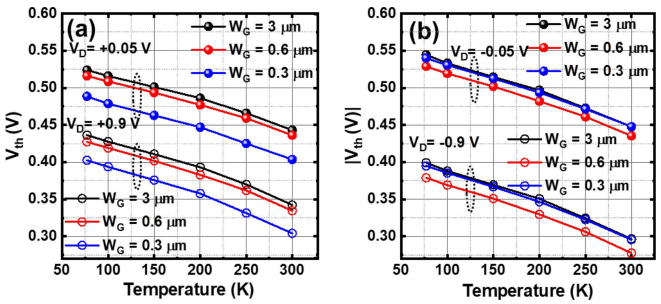

FIGURE 3. Threshold voltage as a function of measurement temperatures for (a) NMOS and (b) PMOS transistors with $W_G = 0.3$ μm − 3 μm.

94 mV for than N-MOSFETs operating at linear and saturation regimes, respectively. Similarly, P-MOSFETs with $W_G = 0.6$ μm and 0.3 μm appear to have stronger temperature-induced V_{th} shift than N-MOSFETs.

Low-temperature operation indeed improves DIBL for both N-MOSFETs and P-MOSFETs as shown in Fig. 4(a) and 4(b), respectively. Notably, the improvement in DIBL (ΔDIBL = DIBL($T = 77$ K) − DIBL($T = 300$ K)) appears to be more evident in N-MOSFETs (−15 mV/V) as compared to that ($\sim$ −8 mV/V) of P-MOSFETs. The reduction in DIBL for PMOSFETs becomes saturated at temperature below 150 K, whereas NMOSFETs have a continuous improvement in DIBL with lowering temperature from 300 K to 77 K.

Fig. 5 shows that at $T = 200$ K−300 K, SS decreases with lowering temperature, following a linear relationship of $SS = n\times$ ln(10)(kT/q) with n being a constant and independent of temperature. It is important to note that at temperatures below 170 K for N-MOSFETs and 200 K for P-MOSFETs, respectively, the SS linearity does not hold anymore. That is, n becomes a function of temperature and gets larger at lower temperatures. Another important

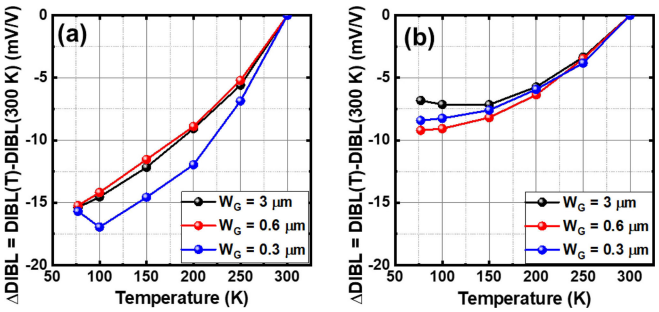

FIGURE 4. DIBL as a function of measurement temperatures for (a) N-MOSFETs and (b) P-MOSFETs.

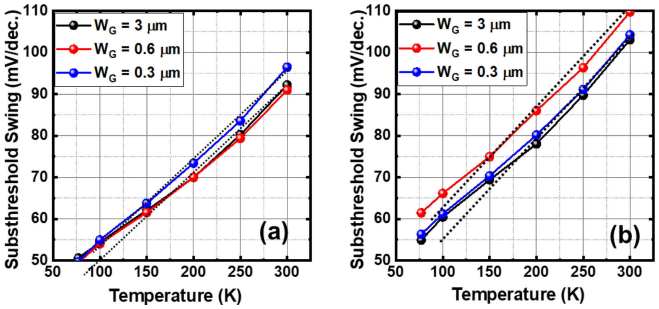

FIGURE 5. Temperature-dependent subthreshold swing for (a) N-MOSFETs and (b) P-MOSFETs with W_G = 0.3 μm − 3 μm biased at V_D = +0.9 V and −0.9 V, respectively.

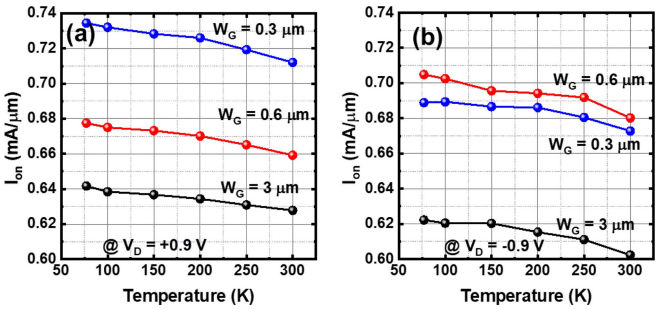

FIGURE 6. Temperature dependency of I_{ON} for N-MOSFETs and P-MOSFETs with W_G of 0.3 μm, 0.6 μm, and 3 μm biased at V_D = +0.9 V and −0.9 V, respectively.

finding of notes is that lowering-temperature induced *SS* improvement is much enhanced for P-MOSFETs in comparison to N-MOSFETs. This is evidenced by the observation that while studied P-MOSFETs operating in the saturation regime have *SS* values of 103−110 mV/dec larger than N-MOSFETs (90−96 mV/dec) at 300 K (Fig. 5(a)), *SS* values of 55−57 mV/dec for 0.6 μm- and 0.3 μm-wide P-MOSFETs (Fig. 5(b)) are getting close to that of 50 mV/dec for N-MOSFETs at 77 K.

While *SS* significantly improves at low temperatures, Fig. 6 shows that there is only a slight increase in I_{ON} by 1.03-fold when lowering temperature from 300 K to 77 K for both N-MOSFETs and P-MOSFETs. This is because a large increase in V_{th} at 77 K reduces the gate overdrive of $V_G - V_{th}$ and thereby, suppresses I_{ON} enhancement. Beckers *et al.* [14]

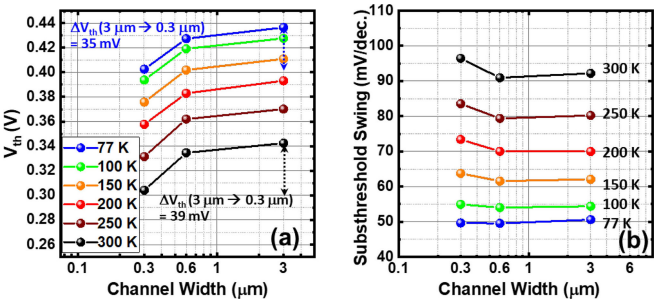

FIGURE 7. Channel width-dependent (a) V_{th} and (b) *SS* for NMOSFETs operating at V_D = +0.9 V and measured at temperature of 77 K − 300 K.

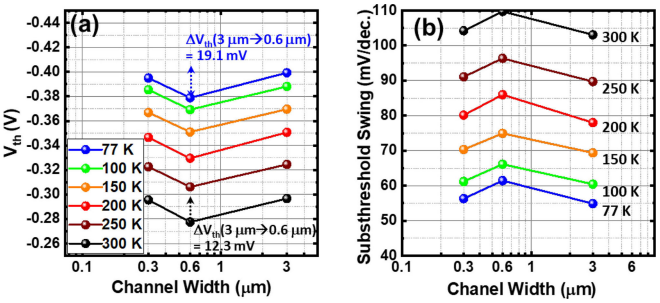

FIGURE 8. Channel width-dependent (a) V_{th} and (b) *SS* for PMOSFETs operating at V_D = −0.9 V and measured at temperature of 77 K − 300 K.

have reported that lowering temperature from 300 K to 77 K even decreases I_{ON} for the short-channel (L_G = 28 nm) N-MOSFETs, while I_{ON} increase indeed is observed for the long devices (L_G = 1 μm) at cryogenic temperatures.

B. CHANNEL-WIDTH EFFECT

N-MOSFETs exhibit typical reverse narrow width effect (RNWE), that is, narrowing W_G from 3 μm to 0.3 μm leads to V_{th} roll-off along with *SS* rise-up as seen in Fig. 7(a) and (b), respectively. The phenomenon of W_G-dependent V_{th} roll-off is commonly observed from N-MOSFETs fabricated using shallow-trench isolation technology. RNWEs have been ascribed to stronger gate controllability to the corner of shallow-trenches or a larger gate fringing-field terminating at the sidewall of the channel, [28] so that the gate charge per unit area needed for the inversion of narrower channels becomes smaller. We discovered that RNWEs for N-MOSFETs appear to be suppressed at cryogenic temperatures. That is, ΔV_{th} (= $V_{th}(W_G$ = 0.3 μm) − $V_{th}(W_G$ = 3 μm)) decreases from −39 mV at 300 K to −35 mV at 77 K (Fig. 7(a)) along with a decrease in ΔSS (= $SS(W_G$ = 0.3 μm) − $SS(W_G$ = 3 μm)) from 5 mV/dec to 0 mV/dec (Fig. 7(b)).

In contrast, P-MOSFETs show anomalous RNWEs [29], that is, V_{th} initially decreases with narrowing W_G from 3 μm to 0.6 μm and then reversely increases with further narrowing W_G to 0.3 μm (Fig. 8(a)). We also observed that among studied P-MOSFETs, 0.6 μm-wide PMOSFETs have the highest *SS* at *T* = 77 K−300 K (Figs. 5(b) and 8(b)). Possible mechanisms for the anomalous increase

TABLE 1. Model parameters.

Parameter	Description
VTH0	Long-channel threshold voltage
KT1	Temperature coefficient for threshold voltage
NFACTOR	Subthreshold-swing factor
TFACTOR	Temperature coefficient of NFACTOR
ETA0	DIBL coefficient in subthreshold region
TETA0	Temperature coefficient of ETA0
CDSCD	Drain-bias sensitivity of CDSC
U0	Low-field mobility
UA	1st-order mobility degradation due to vertical field
UB	2nd-order mobility degradation due to vertical field
UTE	Mobility temperature exponent
UA1	Temperature coefficient for UA
UB1	Temperature coefficient for UB
RDSW	Zero bias LDD resistance per unit width
PRT	Temperature coefficient for RDSW
VSAT	Saturation velocity
AT	Temperature coefficient for VSAT

in $V_{\rm th}$ for P-MOSFETs with $W_{\rm G} = 0.3$ μm have been attributed to (1) the formation of phosphorus and arsenic puddle by an enhancement of phosphorus and arsenic transient enhanced diffusion (TED) due to Si interstitials generated by the deep boron S/D implant processes [29] or (2) boron enhanced diffusion due to the presence of a large quantity of boron [30].

It is clearly seen in Figs. 7(a) and 8(a) that at $T = 300$ K, the amount of $W_{\rm G}$-induced $V_{\rm th}$ variation ($\Delta V_{\rm th,3\ \mu m \to 0.3\ \mu m} \sim 39$ mV) for the studied 0.3 μm – 3 μm-wide N-MOSFETs is larger than that of PMOSFETs ($\Delta V_{\rm th,3\ \mu m \to 0.6 \mu m} \sim 12.3$ mV) by a factor of 3. In contrast to the low temperature-improved RNWEs on N-MOSFETs, anomalous RNWEs on $V_{\rm th}$ variation in PMOSFETs appears to be enhanced at $T = 77$ K as evidenced by 12.3 mV of $\Delta V_{\rm th} = V_{\rm th}(W_{\rm G} = 0.6\ \mu{\rm m}) - V_{\rm th}(W_{\rm G} = 3\ \mu{\rm m})$ at $T = 300$ K and 15.7 mV at 77 K.

IV. MODELING RESULTS

Temperature-dependent transfer characteristics of studied 28-nm CMOSFETs were numerically fitted using MYSTIC Synopsys software. Parameters associated with short-channel and temperature effects listed in Table 1 were included in the numerical fitting for CMOSFETs operation at $T = 77$ K – 300 K. It is a known fact that standard BSIM compact models validate only at temperature ranging from 220 K to 450 K and fails to fit the characteristics of MOSFETs at cryogenic temperatures. In the standard BSIM models, a linear fitting is generally used to describe temperature effects on the critical temperature-dependent parameters of $V_{\rm th}$, *SS*, mobility, and source-drain parasitic resistance ($R_{\rm DSW}$). However, when temperature falls below 220 K, temperature coefficients of *KT1*, *UTE*, and *PRT* are not a constant anymore but varies with temperature, resulting in large fitting errors for simulating characteristics of MOSFETs using the standard BSIM models at cryogenic temperatures. Therefore, the inclusion of the additional temperature-dependent functions for these coefficients is required in order to improve the fitting precision for MOSFETs operation from 77 K to 300 K. For modeling the performance of MOSFETs at cryogenic temperatures, one has to tune key parameters at each temperature point in order to account for the varying device characteristics across the wide temperature range of 77 K–300 K [17], [31].

In BSIM4 model, the threshold voltage at the nominal temperature (*TNOM*) and its temperature dependence are given in Eq. (1) and (2), respectively.

$$\begin{aligned} V_{th} = {} & VTH0 + \left(\mathrm{K}_{1ox} \cdot \sqrt{\Phi_s - V_{bseff}} - K1 \cdot \sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} \\ & - K_{2ox} V_{bseff} + K_{1ox}\left(\sqrt{1+\frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_s} \\ & + \left(K3 + K3B \cdot V_{bseff}\right)\frac{TOXE}{W'_{eff} + W0}\Phi_s \\ & - 0.5 \cdot \left[\frac{DVT0W}{cosh\left(DVT1W\frac{L_{eff}W'_{eff}}{l_{tw}}\right) - 1} \right. \\ & \left. + \frac{DVT0}{cosh\left(DVT1\frac{L_{eff}}{l_t}\right) - 1}\right](V_{bi} - \Phi_s) \\ & - \frac{0.5}{cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right) - 1}\left(ETA0 + ETAB \cdot V_{bseff}\right)V_{ds} \\ & - nv_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot \left(1 + e^{-DVTP1 \cdot V_{ds}}\right)}\right) \\ & - \left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP3}}\right) \cdot \tanh(DVTP4 \cdot V_{ds}) \end{aligned} \tag{1}$$

$$\begin{aligned} V_{th}(T) = {} & V_{th}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{beff}\right) \\ & \times \left(\frac{T}{TNOM} - 1\right). \end{aligned} \tag{2}$$

The primary temperature-dependent parameters considered in Eqs. (1) and (2) are *ETA0* and *KT1*, which are the temperature-dependent DIBL coefficient in the subthreshold region and the temperature coefficient of $V_{\rm th}$, respectively, to be fitted.

Figs. 9(a) and (b) show fitted *KT1*(T) curves for N- and P-MOSFETs with $W_{\rm G} = 0.3{-}3$ μm, respectively. Fitted *KT1* is a negative value and increases with lowering temperature. For N-MOSFETs, the fitted *KT1*(T) curve for the case of $W_{\rm G} = 0.3$ μm is below the curves for that of $W_{\rm G} = 0.6$ μm and 3 μm (Fig. 9(a)). On the contrary, the fitted *KT1*(T) curve for PMOSFETs with $W_{\rm G} = 0.3$ μm lands well above others (Fig. 9(b)). In general, the fitted *KT1*(T) curves of P-MOSFETs lands below that of N-MOSFETs, suggesting that $V_{\rm th}$ of P-MOSFETs has a stronger temperature dependency (Fig. 9(b)).

TABLE 2. Fitted coefficients of $KT1_0$, $KT1_1$, and $KT1_2$ for $KT1$ (T) of NMOSFETs and PMOSFETs.

	NMOSFETs			PMOSFETs		
	W = 3 μm	W = 0.6 μm	W = 0.3 μm	W = 3 μm	W = 0.6 μm	W = 0.3 μm
$KT1_0$	-1.12E-1	-1.06E-1	-1.06E-1	-1.15E-1	-1.23E-1	-1.13E-1
$KT1_1$	7.02E-5	2.24E-5	-4.65E-5	-1.60E-4	1.64E-5	-1.17E-4
$KT1_2$	-7.25E-7	-6.15E-7	-3.83E-7	4.47E-8	-4.89E-7	1.21E-9

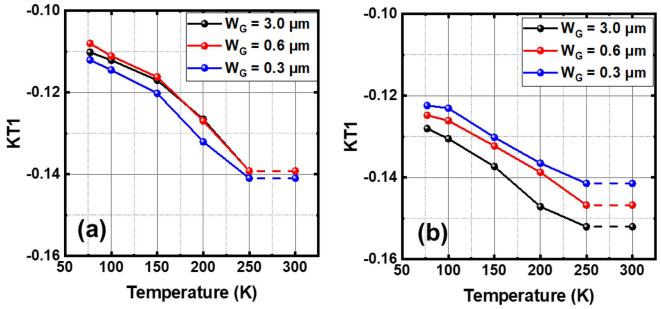

FIGURE 9. Fitted temperature-dependent $KT1$ for (a) N- and (b) P-MOSFETs with $W_G = 0.3\ \mu m - 3\ \mu m$.

It is clearly seen in Fig. 9 that as temperature is lower than 250 K, $KT1$ deviates from the suggested constant value of $KT1$ ($T = 300 - 250$K) of the process design kit (PDK) provided by the foundry. This is because standard BSIM model only validates at the temperature range of 220 K–400K. For 28 nm CMOSFETs, fitted $KT1$ curves appear to be a function of temperature and channel width, following a relationship of $KT1(T) = KT1_0 + KT1_1 \times T + KT1_2 \times T^2$. The fitted values for $KT1_0$, $KT1_1$, and $KT1_2$ for NMOSFETs and PMOSFETs are listed in Table 1. An interesting finding of notes is that the temperature-dependency of $KT1$ for NMOSFETs appear to be stronger than that of PMOSFETs, whereas the impact of channel-width effects on the temperature coefficient of threshold voltage for PMOSFETs is obviously significant than on that for NMOSFETs.

Fitted $KT1$ curves well explain experimentally-observed temperature dependency of V_{th}, as evidenced by a good agreement of experimentally-measured and numerically-simulated V_{th} shift for N- and P-MOSFETs at $|V_D| = 0.05$ V and 0.9 V in Fig. 10.

Intuitively SS improves (decreases) with lowering temperature due to reduced thermionic emission, following an empirical equation of $n\times$ ln(10) (kT/q). However, previous reports have pointed out the fact that below a critical temperature, SS deviates from the Boltzmann limit and saturates. [24], [32]–[34]. In this work, we used the subthreshold-swing factor (*NFACTOR:* a parameter to compensate errors in calculating depletion-capacitance) and its temperature coefficient (*TNFACTOR*) to describe the temperature dependency of $n(T)$ for modeling SS. n and *NFACTOR* are described in Eqs. (3) and (4), respectively.

$$n = 1 + NFACTOR\frac{C_{dep}}{C_{oxe}} + \frac{Cdsc\_Term + CIT}{C_{oxe}} \tag{3}$$

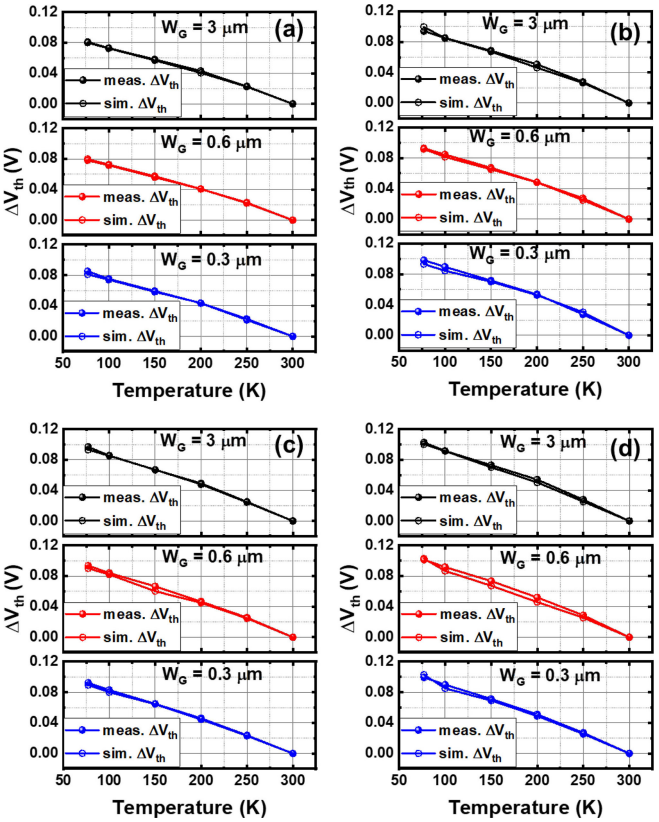

FIGURE 10. Temperature-dependent measured and simulated values for V_{th} shift for NMOSFETs at (a) $V_D = +0.5$ V, (b) +0.9 V and PMOSFETs at (c) $V_D = -0.5$ V, (d) −0.9 V with $W_G = 0.3\ \mu m - 3\ \mu m$.

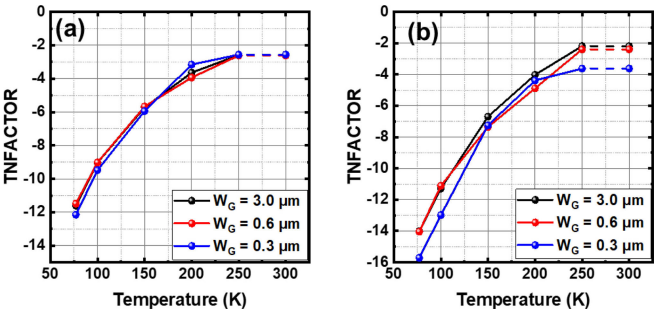

FIGURE 11. *TNFACTOR* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

$$NFACTOR(T) = NFACTOR(TNOM) + TNFACTOR\left(\frac{T}{TNOM} - 1\right) \tag{4}$$

Figs. 11 and 12 show that fitted curves of $TNFACTOR(T)$ and $NFACTOR(T)$ for P-MOSFETs appear to have stronger temperature dependency than that for NMOSFETs, in particular, when temperature is below 150 K.

Lowering operating temperature is beneficial for improving carrier mobility due to reduced phonon scattering. Eq. (5) describes the temperature dependency of low-field mobility

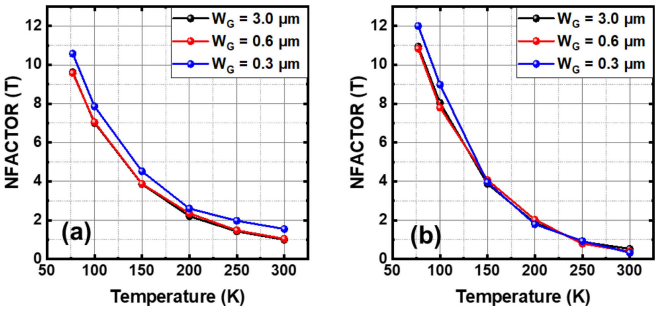

FIGURE 12. Temperature-dependent *NFACTOR* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

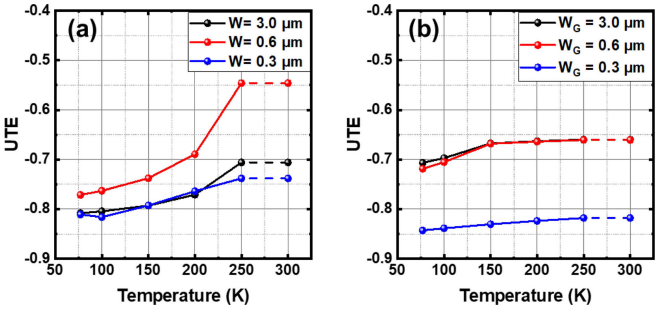

FIGURE 13. *UTE* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

in BSIM models.

$$U0(T) = U0(TNOM)\left(\frac{T}{TNOM}\right)^{UTE}. \quad (5)$$

Extracted mobility temperature exponent, *UTE*, curves for N-MOSFETs and P-MOSFETs are shown in Fig. 13. It is clearly seen in Fig. 13(a) that the values of *UTE*(T) for 0.3 μm-wide N-MOSFETs vary from −0.74 to -0.82, whereas 3 μm-wide N-MOSFETs have *UTE* values ranging from −0.55 – −0.77. These fitted values of *UTE* suggest that the low-field electron mobility in N-MOSFETs with narrow width of 0.3 μm is predominated by phonon scattering ($\mu_L \propto T^{-1.5}$), whereas combined effects of Coulomb scattering ($\mu_L \propto T^{+1.5}$) and phonon scattering influence electron mobility for NMOSFETs with 3 μm and 0.6 μm wide-channels. Another interesting finding from our experimental and simulation results is that all studied 0.3 μm–3 μm-wide P-MOSFETs have fitted *UTE*(T) values ranging from −0.66 – −0.84, indicating that low-field hole mobility is influenced by both Coulomb scattering and phonon scattering. Figs. 14(a) and (b) show a drastic increase in low-field electron- and hole-mobility when measurement temperature is lower than 150 K and 200 K, respectively, where phonon scattering becomes dominant.

RDSW is a parameter to describe source/drain parasitic resistance, consisting of contact resistance, diffusion resistance between the contact and the gate edge, and crowding resistance at the gate edge. *RDSW* does not proportionally scale with the channel length and gives more impacts on the drive current of short-channel MOSFETs because *RDSW*

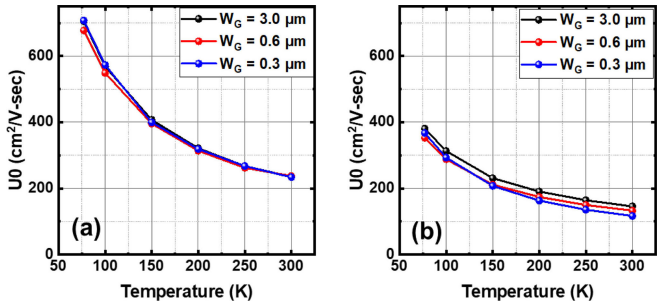

FIGURE 14. Temperature-dependent *U0* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

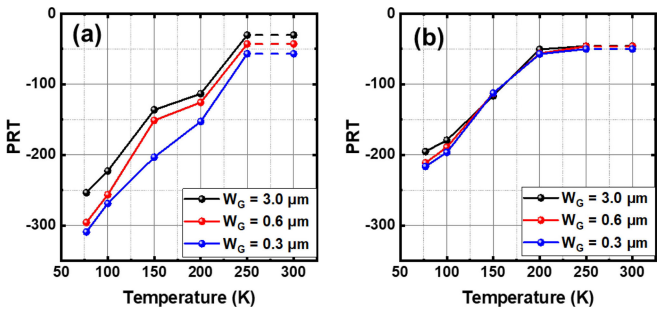

FIGURE 15. *PRT* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

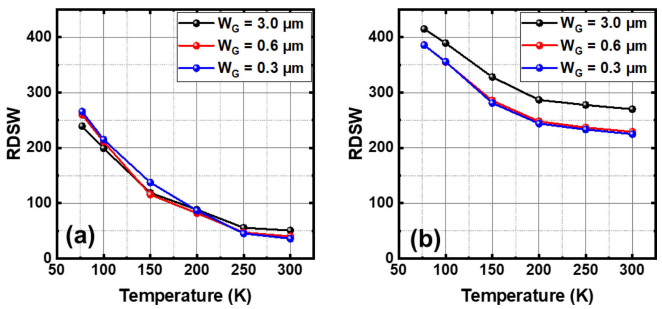

FIGURE 16. Temperature-dependent *RDSW* for (a) NMOS and (b) PMOS transistors with $W_G = 0.3\ \mu m - 3\ \mu m$.

becomes comparable to the conducting channel resistance. The temperature dependence of *RDSW* in BSIM model is given in Eq. (6)

$$RDSW(T) = RDSW(TNOM) + PRT\left(\frac{T}{TNOM} - 1\right). \quad (6)$$

Extracted *PRT*(T) curves of *RDSW* for N-MOSFETs and P-MOSFETs are shown in Fig. 15. *PRT*(T) curves of PMOSFETs generally lands over the curves of N-MOSFET, whereas *PRT*(T) of N-MOSFETs appears to have a stronger temperature dependency than P-MOSFETs. Our simulated *PRT*(T) results suggest that As dopants are more susceptible to incomplete ionization than BF_2 dopants at temperature below 200 K. It is clearly seen in Fig. 16 that *RDSW*(T) curves of N-MOSFETs are much lower than that of P-MOSFETs by a factor of 5 at T = 250 K–300 K,

and the difference in $RDSW(T)$ gets smaller between N-MOSFETs and P-MOSFETs at T below 200 K because a drastic increase in *RDSW* for NMOSFETs.

Intuitively one may expect a decrease in *RDSW* by lowering temperature. However, previous report [31] has already showed that experimentally-measured *RDSW* values of $L_G = 0.35$ μm N-MOSFETs and P-MOSFETs increase with lowering temperatures from 300 K to 77 K. Concurrent with the increase in *RDSW* at low temperatures, the offset of the channel length (ΔL), which is defined as the difference between L_{mask} and L_{eff} (the effective channel length), decreases from a positive value to a negative value due to an overextension of the effective gate length. A negative ΔL value at low temperatures suggestes that potential barriers appear at the gate edges in the overlapping gate-to-source and gate-to-drain regions. The potential barriers augment parasitic resistance. Besides, Luo *et al.* [35] have also reported that compared to the case at 300 K, larger *RDSW* at 77 K is predominantly induced by incomplete ionization effects occurring to lightly-doped (LDD) regions near source/drain for 0.18 μm NMOSFETs. This is because that incomplete ionization at cryogenic temperature is enhanced particularly in LDD regions due to higher activation energies required for lower doping levels [36] as compared to that for heavily-doped S/D, resulting in a large series resistance in the LDD regions.

V. CONCLUSION

We presented the cryogenic study of 28-nm CMOSFETs from 300 K to 77 K. Temperature dependencies of V_{th}, DIBL, I_{ON}, and *SS* for CMOSFETs with $W_G = 0.3$ μm − 3 μm were experimentally measured and numerically fitted. We observed that P-MOSFETs appear to have a stronger temperature dependency in terms of V_{th} increase and *SS* reduction than their counterpart N-MOSFETs. In contrast, DIBL improvement by lowering temperature is more significant in N-MOSFETs. RNWEs on N-MOSFETs in terms of V_{th} roll-off and *SS* rise-up are suppressed at cryogenic temperatures, whereas P-MOSFETs appear to have mild temperature dependence of anomalous RNWE in terms of V_{th} and DIBL variations. Based on our experimentally-measured cryogenic characteristics of CMOSFETs, we have advanced the BSIM modeling for better design of cryogenic CMOS circuitry.

ACKNOWLEDGMENT

The authors would express their sincere gratitude to MediaTek Inc. for providing the 28 nm-CMOSFET testkey samples studied in this work. The authors thank Synopsys for the technical support of transistor model parameter extraction.

REFERENCES

[1] B. Patra *et al.*, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

[2] J.-S. Park *et al.*, "13.1 A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22nm FFL FinFET Technology," in *Proc. IEEE ISSCC*, 2021, pp. 208–210, doi: 10.1109/ISSCC42613.2021.9365762.

[3] E. Charbon *et al.*, "Cryo-CMOS for quantum computing," in *IEDM Tech. Dig.*, 2016, pp. 1–4, doi: 10.1109/IEDM.2016.7838410.

[4] D. J. Reilly, "Engineering the quantum-classical interface of solid-state qubits," *NPJ Quantum Inf.*, vol. 1, Oct. 2015, Art. no. 15011, doi: 10.1038/npjqi.2015.11.

[5] S. R. Ekanayake, T. Lehmann, A. S. Dzurak, R. G. Clark, and A. Brawley, "Characterization of SOS-CMOS FETs at low temperatures for the design of integrated circuits for quantum bit control and readout," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 539–547, Feb. 2010, doi: 10.1109/TED.2009.2037381.

[6] J. M. Hornibrook *et al.*, "Cryogenic control architecture for large-scale quantum computing," *Phys. Rev. Appl.*, vol. 3, Feb. 2015, Art. no. 24010, doi: 10.1103/PhysRevApplied.3.024010.

[7] V. Revéret *et al.*, "CESAR: Cryogenic electronics for space applications," *J. Low Temp. Phys.*, vol. 176, nos. 3–4, pp. 446–452, 2014, doi: 10.1007/s10909-013-1021-4.

[8] P. Merken, T. Souverijns, J. Putzeys, Y. Creten, and C. V. Hoof, "Flight qualification and circuit development of sensor front-end electronics for PACS/Hershel at liquid helium temperature," *J. Microelectron. Electron. Packag.*, vol. 4, no. 4, pp. 130–135, 2007, doi: 10.4071/1551-4897-4.4.130.

[9] B. Okcan, P. Merken, G. Gielen, and C. van Hoof, "A cryogenic analog to digital converter operating from 300 K down to 4.4 K," *Rev. Sci. Instrum.*, vol. 81, no. 2, Feb. 2010, Art. no. 24702, doi: 10.1063/1.3309825.

[10] W. H. Henkels *et al.*, "A 4-Mb low-temperature DRAM," *IEEE J. Solid-State Circuits*, vol. 26, no. 11, pp. 1519–1529, Nov. 1991, doi: 10.1109/4.98967.

[11] S. Skorobogotov, "Low temperature data remanence in static RAM," Dept. Comput. Lab., Univ. Cambridge, Cambridge, U.K., Rep. UCAM-CL-TR-536, 2002.

[12] H. L. Chiang *et al.*, "Cold CMOS as a power-performance-reliability booster for advanced FinFETs," in *IEEE VLSI Tech. Dig.*, 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265065.

[13] D. M. Carlson, D. C. Sullivan, R. E. Bach, and D. R. Resnick, "The ETA 10 liquid-nitrogen-cooled supercomputer system," *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1404–1413, Aug. 1989, doi: 10.1109/16.30952.

[14] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing," in *Proc. 47th Eur. Solid-State Dev. Res. Conf. (ESSDERC)*, 2017, pp. 62–65, doi: 10.1109/ESSDERC.2017.8066592.

[15] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOSFET threshold voltage model," in *Proc. 49th Eur. Solid-State Dev. Res. Conf. (ESSDERC)*, 2019, pp. 94–97, doi: 10.1109/ESSDERC.2019.8901806.

[16] A. Mercha, J. M. Rafi, E. Sirnoen, E. Augendre, and C. Claeys, "Parasitic conduction in a 0.13 μm CMOS technology at low temperature," in *Proc. IEEE 5th Workshop Low Temp. Electron. (WOLTE)*, 2002, pp. 61–64, doi: 10.1109/WOLTE.2002.1022451.

[17] R. Saligram, W. Chakraborty, N. Cao, Y. Cao, S. Datta, and A. Raychowdhury, "Power performance analysis of digital standard cells for 28 nm bulk CMOS at cryogenic temperature using BSIM models," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 7, no. 2, pp. 193–200, Dec. 2021, doi: 10.1109/JXCDC.2021.3131100.

[18] J. Ning, M. Schormans, and A. Demosthenous, "Towards an improved model for 65-nm CMOS at cryogenic temperatures," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5, doi: 10.1109/ISCAS45731.2020.9180666.

[19] T. Lu, Y. Zhang, Y. Zhang, J. Xu, G. Guo, and C. Luo, "Cryogenic modeling of MOSFET device based on BSIM and EKV models," 2021, *arXiv:2104.08467*.

[20] A. Kabaoğlu and M. B. Yelten, "A cryogenic modeling methodology of MOSFET I-V characteristics in BSIM3," in *Proc. IEEE 14th Int. Conf. Synth. Model. Anal. Simul. Methods Appl. Circuit Des. (SMACD)*, 2017, pp. 1–4, doi: 10.1109/SMACD.2017.7981578.

[21] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1007–1018, 2018, doi: 10.1109/JEDS.2018.2817458.

[22] W. Chakraborty, K. Ni, J. Smoth, A. Raychowdhury, and S. Datta, "An empirically validated virtual source FET model for deeply scaled cool CMOS," in *IEDM Tech. Dig.*, Dec. 2019, pp. 1–4.

[23] G. Pahwa, P. Kushwaha, A. Dasgupta, S. Salahuddin, and C. Hu, "Compact modeling of temperature effects in FDSOI and FinFET devices down to cryogenic temperatures," *IEEE Trans. Electron Dev.*, vol. 68, no. 9, pp. 4223–4230, Sep. 2021, doi: 10.1109/TED.2021.3097971.

[24] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 106–115, Sep. 2019, doi: 10.1016/j.sse.2019.03.033.

[25] W. Chakraborty *et al.*, "Characterization and modeling of 22 nm FDSOI cryogenic RF CMOS," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 7, no. 2, pp. 184–192, Dec. 2021, doi: 10.1109/JXCDC.2021.3131144.

[26] S. Bonen *et al.*, "Cryogenic characterization of 22-nm FDSOI CMOS technology for quantum computing ICs," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 127–130, Jan. 2019, doi: 10.1109/LED.2018.2880303.

[27] F. S. Di Santa Maria, C. Theodorou, X. Mescot, F. Balestra, G. Ghibaudo, and M. Cassé, "Low temperature behavior of FD-SOI MOSFETs from micro- to nano-meter channel lengths," in *Proc. IEEE 14th Workshop Low Temp. Electron. (WOLTE)*, 2021, pp. 1–4, doi: 10.1109/WOLTE49037.2021.9555451.

[28] L. A. Akers, "The inverse-narrow-width effect," *IEEE Electron Device Lett.*, vol. 7, no. 7, pp. 419–421, Jul. 1986, doi: 10.1109/EDL.1986.26422.

[29] W. S. Lau *et al.*, "Anomalous narrow width effect in NMOS and PMOS surface channel transistors using shallow trench isolation," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, 2005, pp. 773–776, doi: 10.1109/EDSSC.2005.1635391.

[30] A. Agarwal, H.-J. Gossmann, D. J. Eaglesham, S. B. Herner, A. T. Fiory, and T. E. Haynes, "Boron-enhanced diffusion of boron from ultralow-energy ion implantation," *Appl. Phys. Lett.*, vol. 74, p. 2435, Apr. 1999, doi: 10.1063/1.123872.

[31] H. Zhao and X. Liu, "Modeling of a standard 0.35 μm CMOS technology operating from 77 K to 300 K," *Cryogenics*, vol. 59, pp. 49–59, Jan./Feb. 2014, doi: 10.1016/j.cryogenics.2013.10.003.

[32] A. Beckers, F. Jazaeri, and C. Enz, "Theoretical limit of low temperature subthreshold swing in field-effect transistors," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 276–279, Feb. 2020, doi: 10.1109/LED.2019.2963379.

[33] H. Bohuslavskyi *et al.*, "Cryogenic subthreshold swing saturation in FD-SOI MOSFETs described with band broadening," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 784–787, May 2019, doi: 10.1109/LED.2019.2903111.

[34] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018, doi: 10.1109/TED.2018.2854701.

[35] C. Luo, Z. Li, T.-T. Lu, J. Xu, and G.-P. Guo, "MOSFET characterization and modeling at cryogenic temperatures," *Cryogenics*, vol. 98, pp. 12–17, Mar. 2019, doi: 10.1016/j.cryogenics.2018.12.009.

[36] A. Akturk, J. Allnutt, Z. Dilli, N. Goldsman, and M. Peckerar, "Device modeling at cryogenic temperatures: Effects of incomplete ionization," *IEEE Trans. Electron Devices.*, vol. 54, no. 11, pp. 2984–2990, Nov. 2007, doi: 10.1109/TED.2007.906966.