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BEOL Process Effects on ePCM Reliability

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ABSTRACT The effect of back-end of line (BEOL) process on cell performance and reliability of Phase-Change Memory embedded in a 28nm FD-SOI platform (ePCM) is discussed. The microscopic evolution of the Ge-rich GST alloy during process is the focus of the first part of the paper. A new metric for quantification of active material modifications is introduced to better follow its evolution with process sequence. Ge clustering has been shown to occur during the fabrication, impacting the pristine resistance and the after forming cell performance. Two different BEOL processes are then benchmarked in terms of key performance. An optimized process is identified, and an extensive electrical characterization of array performance and reliability is done on the full 16MB chip. The optimized BEOL process results in a memory cell fully compatible with the requirements for demanding automotive applications.

INDEX TERMS ePCM, reliability, BEOL, 28nm FDSOI, embedded memory, emerging memory, Ge-rich GST, GST.

I. INTRODUCTION

The demand for semiconductor microchips in automotive markets is increasing year by year driven by the amount of intelligence needed to optimize engine performance, improve driving assistance, and enable more and more powerful entertainment on-board systems. Together with the increased intelligence, a strong growth in the demand for memory is also happening. In this scenario, high-density, high-performance memory arrays, embedded in advanced CMOS platforms, are becoming of great interest. Among the non-volatile memories, ePCM [1] is attracting interest for its very good performance and because it can be easily embedded with minimal impact on CMOS logic transistors. The interactions between the BEOL process and ePCM are the focus of this paper. Fig. 1 on the left reports the BJT-selected array diagram in which the bit-lines run vertically, connected to the emitter of a pnp bipolar transistor through the storage element. The word-lines are instead realized by connecting the bases of the bipolars. The collector is common grounded. Fig. 1 on the right shows the 16 MB test chip floorplan as integrated in the 28nm FD-SOI CMOS platform [1].

The cell is realized with the wall approach of Fig. 2, where the cross-section along the word-line (on the left) and along the bit-line (on the right) are reported [2]. Ge-rich GST [3] has been employed as active phase-change material to satisfy the stringent automotive requirements. ePCM is integrated after the front-end CMOS fabrication, according to the complex BEOL integration process flow of Fig. 3. 7 thin metals and 4 thick metals are used to drive the signals inside the embedded chip.

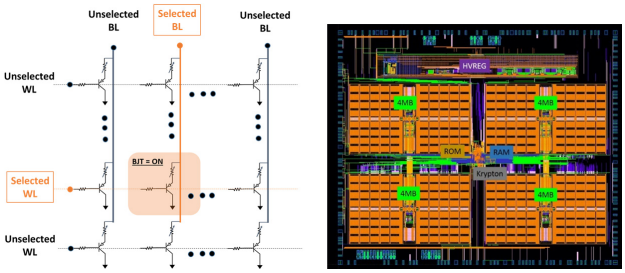

FIGURE 1. On the left: the BJT-selected array is organized by WLs connecting the BJT bases, and BLs connecting cell top electrodes. Collector is common grounded for the full array. On the right: layout of 16 MB test chip.

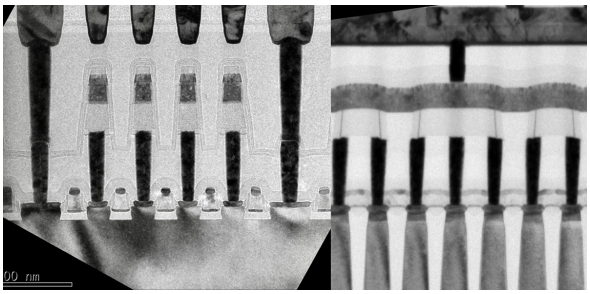

FIGURE 2. ePCM cell cross-section in 28nm FDSOI CMOS platform. X-section showing the BJT 4 emitter structure string [1], Y-section show the continuous BL with the via0 strapping in M1.

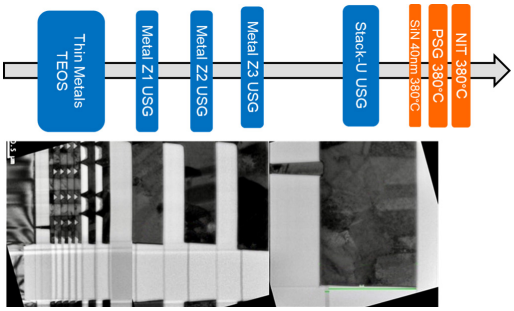

FIGURE 3. Back end of line cross-section and related process scheme. The actual BEOL process employs 7 thin metals and 4 thicker metals.

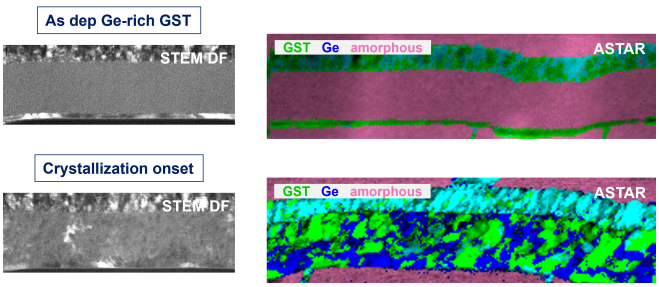

FIGURE 4. Crystallization study of Ge-rich GST during process. When crystallization occurs due to process thermal budget, GST crystallize first pushing out Ge excess.

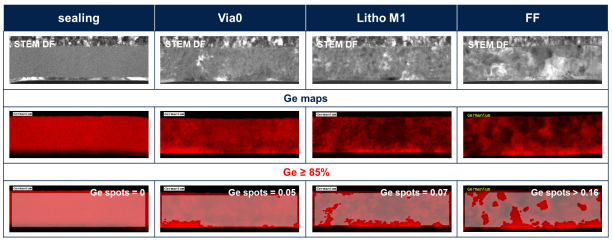

FIGURE 5. Ge segregation of Ge-rich material during process steps at EELS analysis. At Via0 fabrication, Ge clustering starts to be visible. On the bottom row: quantification of Ge clustering during process: reported values are the counts of EELS spots with Ge ≥ 85%, normalized to the map size.

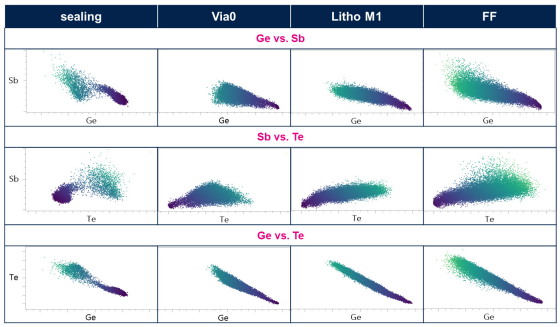

FIGURE 6. Chemical plots of main elements (Ge, Sb, Te) during process steps of EELS data. At Vias0 fabrication, crystallization onset is observable with distribution collapse.

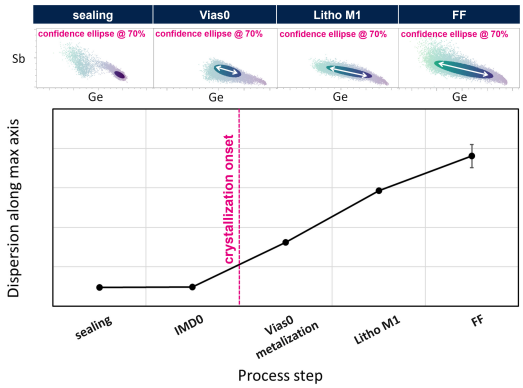

FIGURE 7. On the top: illustrative confidence ellipses @ 70% and their elongation along maximum axis (white arrows when present) for each process step. On the bottom: dispersion along maximum axis metrics in function of process steps. Crystallization onset is highlighted and linear increasing trend for crystallization.

To study the impact of the BEOL process on ePCM, figures from Fig. 4 to Fig. 7 show the active material evolution during different process steps of the integration flow through TEM and EELS analyses, as previously reported by Redaelli *et al.* in [4]. Ge segregation in the Ge-rich GST is highlighted by ASTAR technique [5] (Fig. 4) during the crystallization of the as-deposited amorphous alloy. Clustering of Ge is visually put in evidence in Fig. 5, while a quantification is reported on the bottom row, where it is clear the impact of the first metallization steps. Ge segregation is strictly linked to alloy crystallization, being Ge expulsion and clustering necessary for the crystallization onset [6]. This joined phenomenon can be further studied

by analyzing chemical plots of main alloy elements (Ge, Sb, Te) for each step of the process (in Fig. 6, where color code from violet to light green is proportional to Ge content): passing from as-deposited to end-of-process material, elemental distributions first collapse in an unique population at crystallization onset, mixing Ge-rich and underlayer parts of the active stack, then increase their spread along a preferential direction, corresponding to the axis of Ge increasing/Te decreasing.

In fact, these two directions are strongly correlated (as evidenced by the Ge vs. Te plots) being the three main elements forced to be normalized. Thus, only one plot is needed for the physical description: in the following, Ge vs. Sb plot has been considered. Dispersion increasing along Ge axis with process steps is the chemical consequence of the more and more pronounced Ge expulsion with alloy crystallization: this directional spread indicates the presence of grains with different Ge content, varying for its expulsion degree from each crystal. Stronger is the expulsion wider is the spread, according to Ge clustering reported in Fig. 5. Moreover, a statistical-based method has been elaborated to quantify the observed evolution of chemical dispersion with process steps [7].

The new methodology exploits the definition of Mahalanobis distance (d_M), a generalized version of Euclidean distance that considers intrinsic dispersion and variance of data. Using d_M it is possible to define a *confidence ellipse* for the chemical distribution under study and to extrapolate related parameters to quantify its center point or extension [7]. In particular, the elongation of the maximum axis of the ellipse results connected to the dispersion previously mentioned, giving an effective quantification of the crystallization process of the alloy. The results are reported in Fig. 7: dispersion along maximum axis of confidence ellipses @ 90% are reported in the bottom panel, while an illustrative representation is proposed in the top panel (see white arrows on ellipses @ 70%).

As reported in the figure, this new metrics is capable to show the behavior of alloy crystallization through process steps, highlighting critical points like crystallization onset or quantifying speed of the phenomenon. The trend of extracted metrics is also compatible with observed Ge clustering, which is in turn a forming mechanism (Fig. 8), as extensively studied from Baldo *et al.* [8]. Given a total amount of segregated germanium (as reported with blue and red pictures on the left), differences in the virgin and post-forming median resistance are obtained (as reported on the right with same color code). The post forming cell behavior is thus the result of the forming pulse and the obtained distribution of elements after process integration [8]. This effect must be thus carefully considered.

II. ELECTRICAL CHARACTERIZATION

In this respect, we compare two different BEOL processes, named process A and the optimized process B. Differences in the BEOL between the two processes include optimization

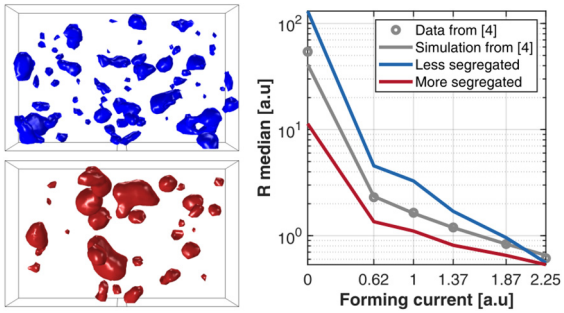

FIGURE 8. On the right: median of resistance obtained with the model reported in [5] for the two different Ge clustering cases on the left (small vs big Ge cluster at a fixed total segregated Ge).

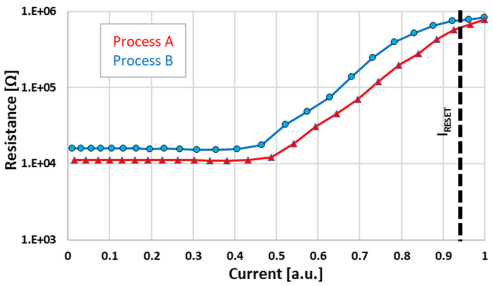

FIGURE 9. Programming curve comparison of process A and B. Process B is the less segregated, reflecting in a higher SET resistance and lower Ireset. Delay between program and read is 100μs.

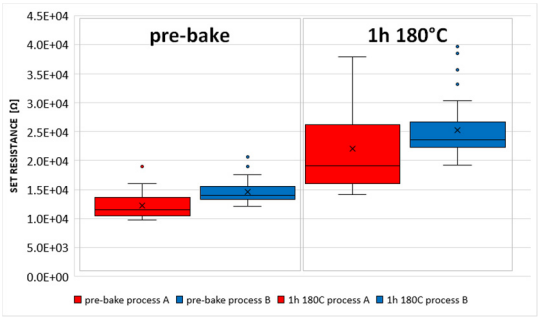

FIGURE 10. SET resistance box plots schematically showing SET drift phenomenon. Pre-bake and 1h @ 180°C conditions are compared. Box plots are acquired over 40 cells on wafer. Symbol "x" states for mean value.

of thermal process steps [9]. Fig. 9 compares the SET-to-RESET programming curves on the median of 40 cells on the wafer. A small effect can be seen in terms of SET resistance and programming curve. Process B features a higher SET resistance due to an average higher Ge concentration in the less segregated end-of-process alloy, consistently with the simulation in Fig. 8 on the right. Fig. 10 schematically shows SET drift phenomenon in the two processes: in the pre-bake condition, resistance mismatch between process A and B, already seen in Fig. 9, is visible and such difference does not change also after 1h @ 180°C of annealing. Thus, SET drift slope is the same in the two processes and no impact on the phenomenon due to Ge concentration in the material is observable, according to previous studies [10]. In

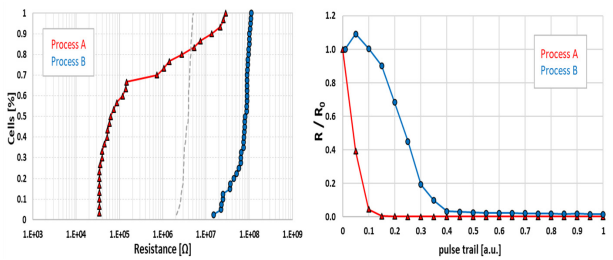

FIGURE 11. On the left: Retention distribution after 230C, 1h retention monitor. Distribution read out is performed after 1s from program, leading to a higher reset resistance drift with respect to the reset resistance value reported in Fig. 9. Process B show better retention performance. On the right: Quenching time experiment shows slower crystallization for process B, consistently with retention data.

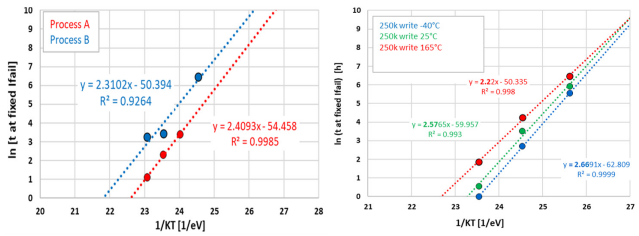

FIGURE 12. On the left: Process A and B crystallization Arrhenius comparison, with process B featuring better retention. On the right: Arrhenius plots for Process B at the end of life at different cycling temperatures.

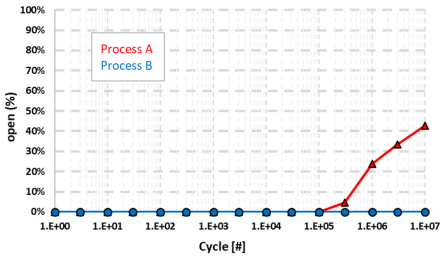

FIGURE 13. Endurance benchmark between the two processes. Process B shows two orders of magnitude improvement in the endurance. Endurance experiments have been carried out with worst case reset condition (higher amplitude).

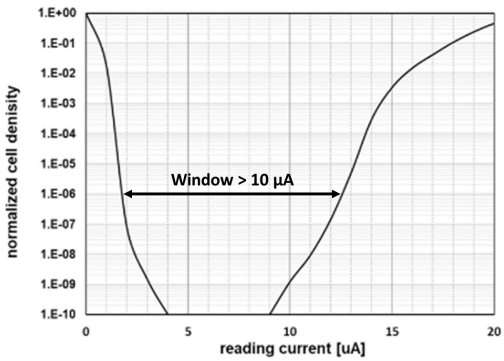

FIGURE 14. SET and RESET distributions of the optimized process. 10 uA window can be detected at BER = 10^{-6}.

fact, SET drift is ascribed to amorphous residuals between grains of crystalline state, not influenced, at a first order, by average Ge content in the alloy. Moreover, the impact of higher segregation of process A is still visible in terms of phenomenon variability, as highlighted in the figure by box plots after annealing.

The benchmark in terms of the crystallization behavior is instead reported in Figs. 11 and 12. Fig. 11 on the left reports the retention monitor (RESET resistance after 1h at 230C bake, corresponding to more than 1 year at 150C): grey dashed line is the pre-bake RESET resistance distribution while red and blue lines are the after-bake distributions of process A and process B respectively. Consistently with the higher Ge content in process B, the blue line shows only drift and no crystallization. Quenching-time experiments are reported in Fig. 11 on the right: in this case also process B shows a slow crystallization material with respect to process A, consistently with the retention monitor discussed before. Also, the Arrhenius plots in Fig. 12 further supports a modification in the amorphous crystallization response, consistent with a change in the active material, induced by process segregation and forming [8]. Note that the activation energy of process B is similar to process A but the Arrhenius pre-factor is much improved (shift up in the Arrhenius plot of Fig. 12 on the left). Furthermore, cycling at different temperatures (Fig. 12 on the right) does not change that much the activation energy that always remains above 2.2 eV.

The other impacted parameter is the cycling performance as reported in Fig. 13, where the main failure mode is the open circuit. Process B can guarantee intrinsically more than 10^7 programming cycles, 2 orders of magnitude better than process A, that intrinsically show a relevant open defect density already at 100K cycles. This is further evidence that supports a change in the active material.

III. OPTIMIZED PROCESS

Fig. 14 reports pre-cycling SET and RESET distributions collected cumulating 80 units of 16 MB arrays of Fig. 1, with the optimized process, named process B. Clean distributions have been demonstrated for both SET and RESET without evidence of outliers. Considering a bit-error rate (BER) of 10^{-6}, needed by ECC (Error Correction Code) to guarantee 1 ppm chip loss on field, more than 10 uA window is demonstrated.

Fig. 15 shows the open failure rate as a function of cycle count for four different cycling temperatures, from −40 °C to 150 °C. An open bit is defined when the current driven by a cell put into the SET state is lower than 2 uA. It is worth noticing that the open occurrence remains below $3x10^{-7}$ up to 250K writes (a write is a single program operation, either SET or RESET). At 500K writes defectivity is anyway lower than 1 ppm, that is the ECC correction capability.

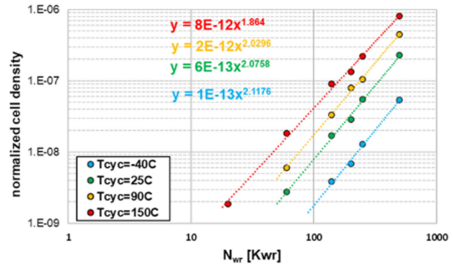

FIGURE 15. Open occurrence vs cycle counts for different environment temperatures. In all the cases BER is less than 10^{-6}.

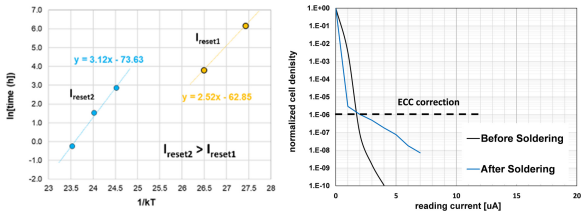

FIGURE 16. On the left: Statistical Ea evaluation extracted at 10^{-7} BER level. The crystallization activation energy is as a function of RESET pulse amplitude: higher the pulse, higher Ea. On the right: RESET distribution pre and after three soldering profiles.

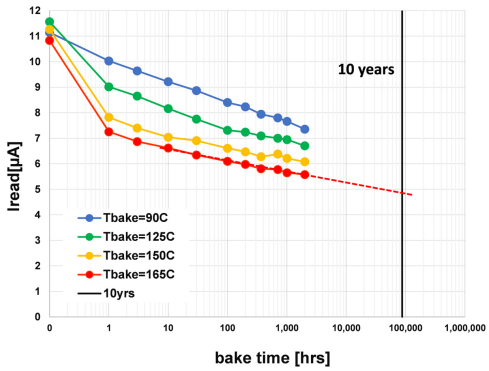

FIGURE 17. SET drift characterization: Iread cut at BER = 10^{-7} after different bakes. For T bake=165C, the read SET current remains higher than 5 uA for 10 years.

Fig. 16 on the left shows the crystallization Arrhenius plot at 10^{-7} defectivity level for two different RESET current amplitudes. The extracted activation energy of crystallization of 3.12 eV, is higher than the values in Fig. 12 for the analytical cell at the same RESET condition, due to better quenching during the RESET pulse in the array (faster falling edge). It is worth noticing that the crystallization activation energy and the Arrhenius pre-factor are a function of the amplitude of the RESET pulse, opening the path for further algorithm optimization.

Fig. 16 on the right shows the RESET distribution before and after three soldering profiles as per JEDEC specification, showing roughly 2 uA current level at ECC correction capability criterion (BER = 10^{-6}).

The extrapolation of SET drift for SET tails is shown in Fig. 17 for different bake temperatures up to 165C.

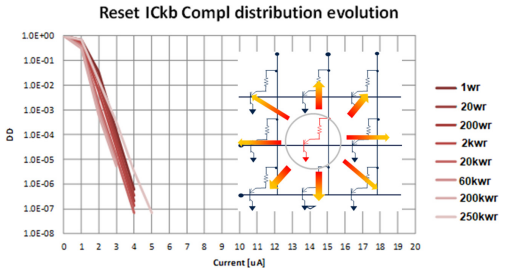

FIGURE 18. Thermal disturb experiment: victim distributions as a function of programming cycles of the aggressors. No tail appearance visible up to 250Kwrites.

BER = 10^{-7} has been chosen to get some additional margin with respect to ECC correction limit in the drift extrapolation. A worst-case end-of-life (10 years) tail current of 5uA can be estimated in the case of higher bake temperature as highlighted by the red dashed projected line.

Thermal disturb was reported as a possible issue for PCM below 45nm with $Ge_2Sb_2Te_5$ [11]. Thermal disturb concerns heat transfer from a cycled aggressor cell (central cell in the figure inset) to neighbor cells previously put in the amorphous state, with possible data loss due to premature crystallization. Following the same methodology as in [11], we found no effect of aggressor cycling on neighbor cells, thus no thermal disturb (no significant RESET distribution shift), by performing dedicated checkerboard experiments up to 250K writes (Fig. 18). Such excellent thermal behavior can be ascribed to a much better RESET retention capability of Ge-rich GST with respect to $Ge_2Sb_2Te_5$ used in the first stand-alone memory applications.

IV. CONCLUSION

In this work the role of BEOL process on ePCM performance has been investigated. A clear evolution of the microscopic alloy structure due to BEOL process has been highlighted through physical analysis, also thanks to the introduction of a novel methodology for compositional analysis. An improved BEOL process has been identified able to intrinsically enhance cell performance. An extensive reliability characterization has been discussed for the optimized process, including SET and RESET retention, soldering compliance, endurance and thermal disturb. The proposed analysis shows intrinsic robustness of the technology for the automotive segment.

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